An Establishment of Neutral Voltage Modulation Strategy for Multilevel Cascaded Inverters under Unbalanced DC Systems

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Abstract: It explains a pulse width modulation process to achieve a balanced line to line output voltages and to maximize the index of modulation in the way of linear modulation range where the output voltage can linearly maintain in the multilevel cascaded inverter (MLCI) operating at unbalanced dc-link conditions. In this process of MLSI, the linear modulation range is reduced, and a perfect output voltage imbalance may come as voltage reference increases. In the proposed method, too large of dc link imbalance avoids the balancing of the output voltages. This limitation has also discussed both simulations and experiments or projects for a seven-level phase-shifted modified MLCI for electric vehicle traction motor drive show that the proposed method can balance line to line output voltages as well as to increase the linear modulation range to peak under the unbalanced dc link conditions.

Index Terms—Harmonic injection, multilevel cascaded inverters (MLCIs), neutral voltage modulation (NVM), phase-shifted (PS) modulation, space vector pulse width modulation (PWM) (SVPWM).

I. INTRODUCTION

Multilevel inverters allow the synthesis of the sinusoidal output voltage from no of steps of voltages. For this reason, multilevel inverters have low di/DT characteristics and usually have low harmonics in the output voltage and current. The switching of very high voltage can be got by stacking multilevel inverter modules. Because of these advantages, multilevel inverters have been applied in different applications fields among different topologies for multilevel inverters; the multilevel cascaded inverter structure is one of the outstanding regional anatomies because of its simple construction for modularization and fault-tolerant capacity. Therefore MLCI is in the application of many things, such as dynamic voltage restores, static synchronous compensator, high voltage energy storage device. In MLCI applications, a modulations strategy to generate gating signals is very crucial to get high-performance control. Respect to this issue many studies have been done, and they are roughly categorized into multilevel selective harmonic deleting pulses width modulation, multilevel carrier-based PWM, & multilevel space vector PWM methods, generally a carrier-based PWM or SVPWM is preferred in some high-power static power converting applications. The series SVPWM method has been studied to cover the overmodulation range in a multilevel inverter.

On the other hand, MLCIs needs to be separated dc links, therefore, if there are one or more faults acquaint in the dc links in each phase as if the voltage orders of the dc links are inadequate, the output voltage of MLCI can be unbalanced without proper payment. To know this issue, some experiments have adequately been acquitted. It is demonstrated that the uncommitted modulation index is reduced under faulty considerations on switch modules in multilevel inverters and recompense algorithms are given for phase-disposition PWM & phase-shifted PWM cases. A neutral voltage shifting cases technique has been an introduction to balancing the state of change in the MLCI based battery energy storage system. A duty cycle modification technique has been proposed to correct an output voltage asymmetry caused by single-phase power fluctuations. Acknowledgment has shown that a zero sequence component helps to obtain the maximum balanced output voltage in a fault condition.

In this page, a carried-based PWM strategy to balance line to line output voltage and to maximize the lines modulation range where the output voltage in each phase is not linear. Accordingly, the linear modification range is deceased, and a significant output voltage imbalance may occur as output voltage references increased compared to the existing technique proposed schemes is very simple to follow and compensation the output voltage imbalance in real time. And rises to maximum the voltage utilization of the dc links. Therefore, if this technique is applied to applications such as EV traction drive systems, the dynamic characteristics can be more improved.

II. MULTILEVEL INVERTERS

In response to the developing demand for high power inverter units, multilevel inverters have been appealing growing attending from academia as well as the industry in the Holocene Decade. between the best-known topologies are the H-bridge

cascade inverter, the capacitor fastening inverter (imbricated cells), and the diode clamping inverter. As described in the literature, the H-bridge cascade inverter has been used in many practical instances for broadcasting amplifier [4], plasma [3], industrial drive [6] as well as STATCOM [7] applications etc. The main restriction of the H-bridge cascade inverter contain in the planning of an isolated power supply for each H-bridge cell When real power transfer is needed. For STATCOM application,

where the isolated amounts are not commanded, the power pulsation at twice output frequency happening with the dc link of apiece H-bridge cell necessitates oversizing Of the dc link capacitors. The capacitor clamping inverter, while the three-level scheme of which was printed in the early 1980's [8], had been seldom discussed until the introduction of the ―imbricated cells‖ [9].

The individual clamping capacitor demands only to fluent the switching frequency ripple voltage and the commanded capacity for each clamping capacitor is hence small. However, as the number of levels enhances, such problems as thermal designing, low-inductance contriving, as well as insulation designing of the system will become decisive Medium voltage drives using four-level capacitor clamping

An inverter has lately been available on the market. The diode fastening inverter, as shown in Fig. 4.1, published by different researchers in the early 90's can be deemed as the extension of the neutral-point-clamped (NPC) inverter Introduced in the early 80 's. Unlike the NPC inverter which has been extensively employed today in industrial drives, tractions as well as FACTS systems, the diode clamping The inverter is right under investigation. In addition to the dc link unbalance problem identified in the other issues with the diode clamping inverter.

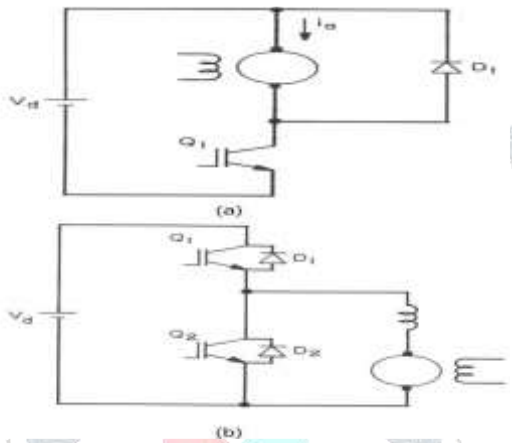

Fig.1 (a) topology of converter

In the hitch mode, as just discussed, the device Q1 hacks the supply voltage and D2 freewheels. In the boost courses, Q2 and D1 are alive. If Q2 is on, the anticipate emf of the motor inclines to builds up the current in the armature inductance, which then courses to the line when Q2 is off. Thus, the machine perambulatory in the generative mode when the motor's mechanical energy is changed into electrical power and fed back to the source. In this mode, Vd is higher than the load counter emf. Small variable-speed permanent magnet (PM) Dc motor drives with dc-dc converters are widely employed in the industry. Separately, buck and boost converters are also commonly used in switching mode power supplies (SMPS). In SMPS, extra filters are typically added to smooth the load harmonics.

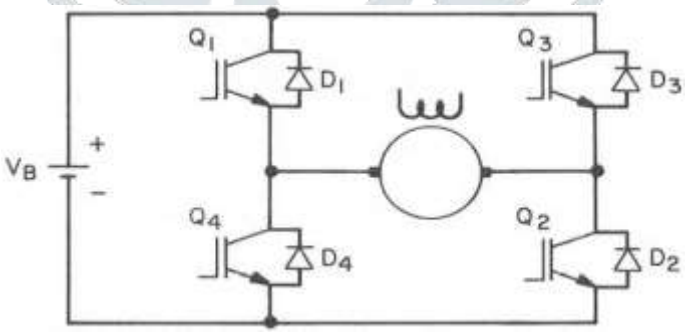

Fig. 2 inverter using an H-bridge topology

III. Existing Topology

This chapter briefly discusses the pulse-width-modulation strategy to accomplish balanced line-to-line output voltages and to increase the modulation index in the additive modulation range where the output voltage can be linearly aligned in the multilevel cascaded inverter (MLCI) controlling under unbalanced dc-link conditions. During the whole range of modulation index from 0 to 1 with less %THD which complies with IEEE 519-1992 harmonic guidelines and also with less switching losses. Commercially existing topologies of multilevel inverters and modulation strategy for the control of multilevel inverters are concisely reviewed. This chapter also awards the documentary of research, research methodology.

Nowadays, power requirements of advanced industries have attained to megawatt level. In detail, high-power medium voltage drives demands power in the megawatt range and is commonly connected to the medium voltage network. It is hard to compare a single power semiconductor switch at once to medium voltage grid (2.3kV, 3.3kV, 4.16kV or 6.9 kV). For this reasons, the

multilevel inverter has regressed as a cost-effective solution for high voltage and high power coverings including power quality and motor campaign problems [26]. As a cost-effective solution, multilevel converter not only reaches more eminent voltage and current ratings, but also alters the use of low power application in renewable energy sources.

These converters are desirable for high voltage and high power coverings due to their power to synthesize higher voltages with a confined maximum device rating, less harmonic distortion, bringing about of smaller common-mode voltage (CM), less electromagnetic sympathy (EMC) problems and attain higher voltage with a bounded maximum device rating.

At present, multilevel inverters are extensively exploited in respective applications such as HVDC transmission [27] distribution generation systems[28], intermediate voltage motor drives[29], Flexible AC Transmission System (FACTS).

IV. PROPOSED PV-STORAGE SYSTEM ARCHITECTURE

This paper is coordinated as follows in section II the voltage vector space for the one by three configuration MLCI is analyzed for a conceptual study. The given modulation scheme is addressed in section III. In sections IV & V, the simulations and experimental results on the two by three MLCI are conferred. Part VI concludes the entire description

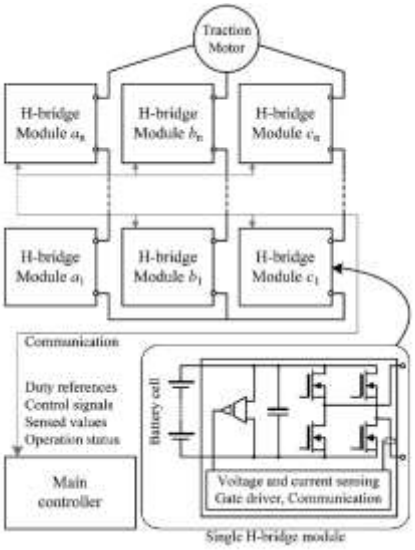

Fig.3 A configuration of mlci for ev traction motor drive

Fig 1 shows the EV traction motor drive system that trades within this paper. In this system, the various power equipment rating is quickly followed by configuration the different number of single H-bridge modules according to a required specification such as neighbor EV, full-size sedan, etc… h.ere all H-bridge having voltage & current sensing circuitries, gate drives and communication interface among module itself and the main controller. Also, battery cells can also be kept in the H-bridge module the unipolar modulation method is given to two switching legs in the H-bridge module.

Therefore the effective switching frequency fsw in a phase is, Fsw=2N×fc----------1

When N and FC represent the No of H-bridge modules in every aspect and the carrier frequency of PWM, fig-2 shows the carrier for each module, the duty cycles in unipolar modulation, and the output voltage when N=2.

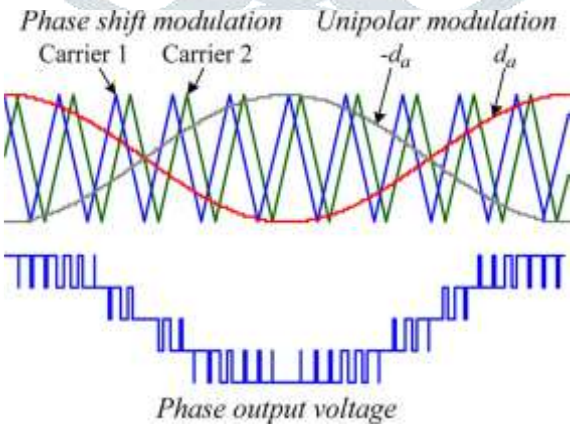

Fig.4. Unipolar and phase shift modulation for single H-bridge module.

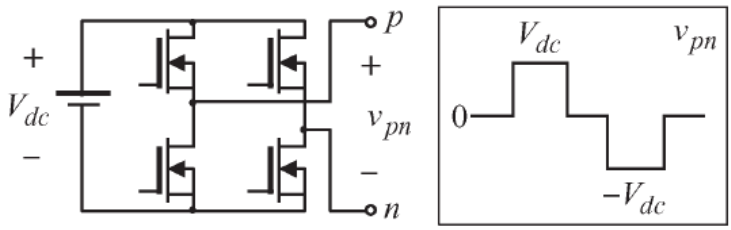

Fig. 5 Output voltage of a single H-bridge module.

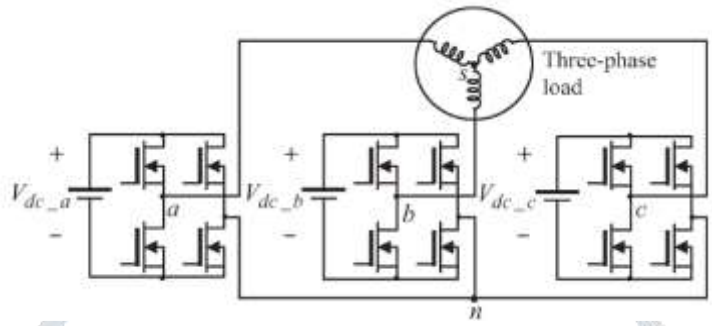

Fig. 6. One-by-three configuration MLCI.

.When the dc link voltage of a single H-bridge module is Vdc, the output Vpn has three states that are Vdc,0, and –Vdc where switching function can be known as Sp and p is exchanged by a, b or c. It represents the phases. The simple one by three configurations MLCI is shown in fig 4

$$v_{pn} = S_p V_{\mathrm{dc}}$$

$$S_p \in \{-1, 0, 1\}_{p=a,b,\mathrm{or},c}$$

The central concept for voltage vector space analysis finds from this standard topology & then it is enlarged to more levels. Here the neutral points are two that is s and n in the MLCI. Here, the voltage amongst the output point of each phase & the neutral point n is defined as the pole voltage Van, Vbn & Van can be known as the pole voltage and the voltages Vas, Vbs, VCs are phase voltages by this concept, Vsn is the voltage between the two neutral points

$$v_{sn} = -v_{as} + v_{an} = -v_{bs} + v_{bn} = -v_{cs} + v_{cn}.$$

By this rule that the sum of all phase voltages becomes zero because the load does not have a neutral line, Vin is written as

$$v_{sn} = \frac{1}{3}(v_{an} + v_{bn} + v_{cn}).$$

By we are substituting 4 in 3 each phases voltage represents as follows by using the relationship defined in 2

$$v_{as} = \frac{2}{3}S_a V_{\mathrm{dc\_}a} - \frac{1}{3}S_b V_{\mathrm{dc\_}b} - \frac{1}{3}S_c V_{\mathrm{dc\_}c}$$

$$v_{bs} = -\frac{1}{3}S_a V_{\mathrm{dc\_}a} + \frac{2}{3}S_b V_{\mathrm{dc\_}b} - \frac{1}{3}S_c V_{\mathrm{dc\_}c}$$

$$v_{cs} = -\frac{1}{3}S_a V_{\mathrm{dc\_}a} - \frac{1}{3}S_b V_{\mathrm{dc\_}b} + \frac{2}{3}S_c V_{\mathrm{dc\_}c}. \qquad (5)$$

If the three dc links value are equilibrated so that Vdc a, Vdc b, Vdc.c have the same amount Vdc the voltage vector space in the α-β axis are defined in fig 5(a).

The switching values of -1 can be cleared by the underbars.

A character of the hexagon in fig 5 a is shown in fig 5 b the vector V010, and V111 are aimed at the same reference axis, phase b here the constitutes of those vectors are different for v010, the vector can be synthesized without the other two phases assistance, however, V111 cant be produced without other vectors according to the vector which doesn't require other two phases assistances to be defined as the independent vectors the dependent vectors are the vectors which depend on different stages.

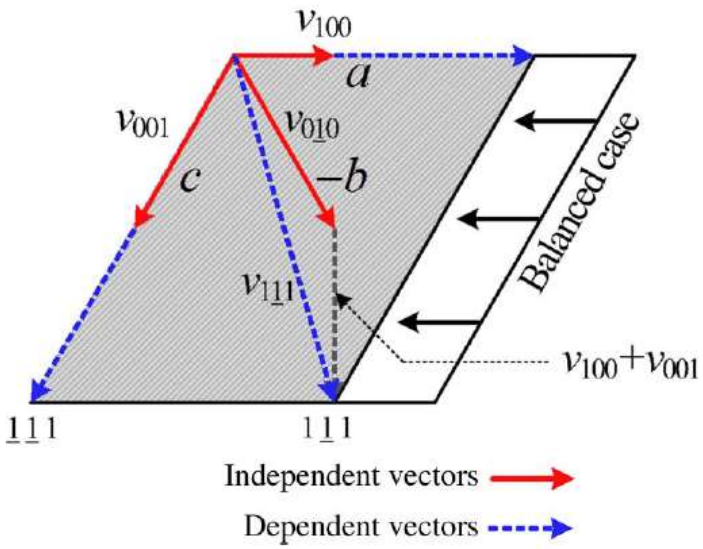

Fig. 7. Voltage vector space in an unbalanced dc-link condition.

The independent vectors can be easily applied in a switching period unlike three ph half bridge inverters because the dc links in each of the three phases are separated in the given system. It should be noted that the maximum voltage is decided by the dependent vectors in the entire voltage vector space. Now, let we assume the case when a three ph load is supplied by unequal dc links fig 6 shown an extremely unbalanced example where Vdc-a is half of the others.

As a result, the V100's magnitude is abbreviated here phase angle of V111, which is the sum of V010, V100, V001. Is no longer equal with the edge of the independent vectors are decreased, the uncommitted voltage vector space is also diminished, and the angles of the dependent vectors are no longer multiples of 60 using this formula, the voltage vector spaces in two different cases are compared in fig 7 a Vdc-a has a less value than the others in fig 7b the three different voltages had by all 3dc links. It can be seen in fig 7 the hexagons original shape is destroyed in both cases this means that the trajectory of the max output voltage vector in the α-β coordinates is also killed according to the shape of the hexagon.

In another way, the magnitude of the maximum modulation index in the linear modulation range in a given hexagon related to the radius of the inner circle which is inscribed in the hexagon as the hexagon distorts, the limit is changed and its linear modulation range is also altered here vph-max is known as maximum amplitude of the phase voltage.

Where Vdc-max, Vdc-mid, and Vdc-min are maxed, medium and minimum voltages.

$$V_{\mathrm{ph\_max}} = \frac{V_{\mathrm{dc\_mid}} + V_{\mathrm{dc\_min}}}{\sqrt{3}}.$$

It should be noted that Vph-max is the maximum synthesize voltage in the linear modulation range in the MLCI undergoing unbalanced dc link conditions.

From 7 it can be recognized that Vph-max is determined by Vdc-mid and Vdc-min if all dc links are well balanced so that Vdc-mid and Vdc-min have identical values, seven is again written as

$$V_{\mathrm{ph\_max}} = \frac{2}{\sqrt{3}} V_{\mathrm{dc}}.$$

This is exactly double the maximum synthesizable voltage in the linear modulation range of a traditional 3-ph half-bridge inverter. The inverter in fig 4 is considered as a three ph full-bridge inverter which is fed by independent dc links. To expand the proposed approach to the multistage MLCI using PS modulation, the total dc-link voltage per phase is represented as

III. PROPOSED MODULATION TECHNIQUE

In section II, the maximum synthesizable voltage in the linear modulation ranged was evaluated under the unbalanced dc links in this section; a method is proposed to realize the enormous modulation index in the linear modulation range these conditions.

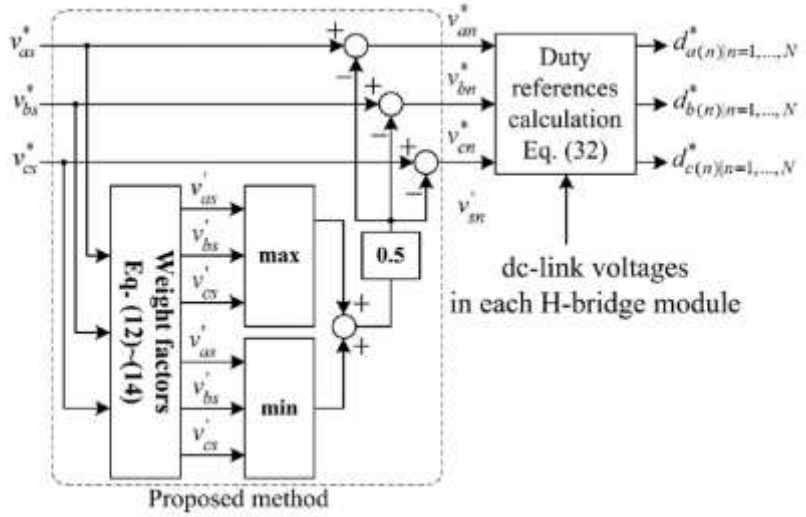

Fig. 8. Implementation of the NVM method.

IV. A TRADITIONAL OFFSET VOLTAGE INJECTION METHOD

The offset voltage injection scheme is a popular technique in three-phase half-bridge inverter applications. The theory beside this is that an offset voltage is incorporate with phase voltage reference to implement various PWM scheme in carrier-based PWM by using that fact that line to line voltage is applied to a 3-ph load 43 44 for ex the offset voltage Vin is injected to the phase voltage reference Vas, Vbs and VCs is injected to the implement carrier-based SVPWM as in

$$v_{sn}^{*} = \frac{v_{\max}^{*} + v_{\min}^{*}}{2} \qquad v_{\max}^{*} = \max\left(v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\right)$$
$$v_{\min}^{*} = \min\left(v_{as}^{*}, v_{bs}^{*}, v_{cs}^{*}\right).$$

If the dc in an MLCI are demented & the traditional offset voltage injection methods are applied the 3-ph output voltages may become distorted as the phase voltage reference approaches Vph-max. this is since the traditional methods are not considering unbalance dc link conditions. hence, even if a phase can synthesize an output voltage address in the linear modulation range, the NVM technique is proposed in this paper. Fig 8 shows the concept of the proposed NVM technique here, a neutral voltage between the two neutral points n and s in fig 4. Is modulated to compensate the output voltage asymmetry caused by unbalanced dc link conditions to do this, the constant weight Kw is defined as,

$$K_w = \frac{V_{\text{dc\_mid}} + V_{\text{dc\_min}}}{2}.$$

By using equ 12, the weight factors are calculated as

$$K_{w\_a} = \frac{K_w}{V_{\text{dc}\_a}} \qquad K_{w\_b} = \frac{K_w}{V_{\text{dc}\_b}} \qquad K_{w\_c} = \frac{K_w}{V_{\text{dc}\_c}} \qquad (13)$$

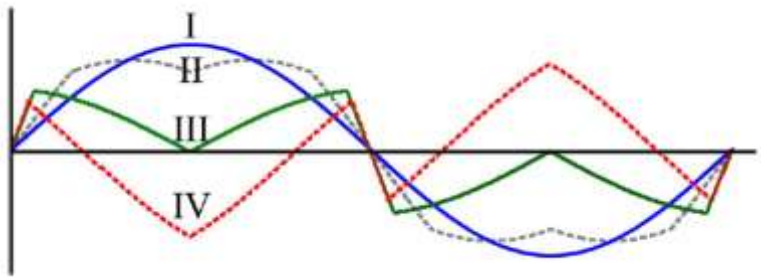

Fig. 9. Comparison of modulated waveforms. (I) Without $v*$ *sn*. (II) Traditional carrier-based SVPWM. (III) Proposed NVM with *V*dc_*a* = 0.275 *V*dc, *V*dc_*b* = *V*dc, and *V*dc_*c* = *V*dc. (IV) Proposed NVM with *V*dc_*a* = 0.2 *V*dc, *V*dc_*b* = *V*dc, and *V*dc_*c* = *V*dc.

Where Kw-a, kw-b, kw-c represent the weight factors for phases a, b, c respectively. Next, the weight factors are manifolded by the phase voltage reference, and new reference Vas', Vbs' and VCs' are found as

$$v'_{as} = K_{w\_a} v^*_{as} \qquad v'_{bs} = K_{w\_b} v^*_{bs} \qquad v'_{cs} = K_{w\_c} v^*_{cs}. \qquad (14)$$

$$v'_{\max} = \max\left(v'_{as}, v'_{bs}, v'_{cs}\right) \qquad v'_{\min} = \min\left(v'_{as}, v'_{bs}, v'_{cs}\right)$$

$$v'_{sn} = \frac{v'_{\max} + v'_{\min}}{2} \qquad \begin{bmatrix} v^*_{an} \\ v^*_{bn} \\ v^*_{cn} \end{bmatrix} = \begin{bmatrix} v^*_{as} - v'_{sn} \\ v^*_{bs} - v'_{sn} \\ v^*_{cs} - v'_{sn} \end{bmatrix}. \qquad (15$$

From 15 and 19, it can be recognized that it Vas', whose dc link voltage is less than the others is corresponding to Vmax or Vmin, the absolute value of Vsn is greater than Van in 10. On the other hand Van, Vbn, Vcn called as pole voltage references. These are calculated by subtracting Vsn from the original phase voltage references Vas, Vbs and VCs as in 15 which are not considering

$$\begin{bmatrix} v^*_{ab} \\ v^*_{bc} \\ v^*_{ca} \end{bmatrix} = \begin{bmatrix} v^*_{an} - v^*_{bn} \\ v^*_{bn} - v^*_{cn} \\ v^*_{cn} - v^*_{an} \end{bmatrix} == \begin{bmatrix} v^*_{as} - v'_{sn} - v^*_{bs} + v'_{sn} \\ v^*_{bs} - v'_{sn} - v^*_{cs} + v'_{sn} \\ v^*_{cs} - v'_{sn} - v^*_{as} + v'_{sn} \end{bmatrix}$$

$$= \begin{bmatrix} v^*_{as} - v^*_{bs} \\ v^*_{bs} - v^*_{cs} \\ v^*_{cs} - v^*_{as} \end{bmatrix}. \qquad ($$

$$V_{\mathrm{dc\_}a} < V_{\mathrm{dc\_}b} < V_{\mathrm{dc\_}c}.$$

$$K_{w\_a} > K_{w\_b} > K_{w\_c} \qquad K_{w\_a} > 1$$

$$K_{w\_b}, K_{w\_c} < 1.$$

$$|v'_{as}| > |v^*_{as}| \qquad |v'_{bs}| < |v^*_{bs}| \qquad |v'_{cs}| < |v^*_{cs}|.$$

Vsn but Vsc on the contrary if VCs is Vmax then the final pole voltage references are bigger than the original pole voltage references by using this principle or formula, the applied method decreases the portion of the phase whose dc link voltage is smaller than the others and increases the utilization of the phase in which the dc link voltage is greater than those of the other phases. From this process, of estimation, the applied method enables the peak synthesizable modulation index in the linear modulation range under this unbalanced dc link conditions to be achieved. In practice to this, if all of the dc link voltages are super balanced so that Vdc-a, and Vdc-care equal to Vdc.

$$V_{\mathrm{dc\_mid}} = V_{\mathrm{dc\_min}} = V_{\mathrm{dc}}.$$

$$K_w = \frac{V_{\mathrm{dc\_mid}} + V_{\mathrm{dc\_min}}}{2} = V_{\mathrm{dc}}$$

$$K_{w\_a} = K_{w\_b} = K_{w\_c} = 1$$

$$v'_{as} = v^*_{as} \qquad v'_{bs} = v^*_{bs} \qquad v'_{cs} = v^*_{cs}.$$

C.CONSTRAINTS OF PROPOSED METHOD

In this section, the limitation of unbalanced dc links can be while still being compensation by the applied process is evaluated.

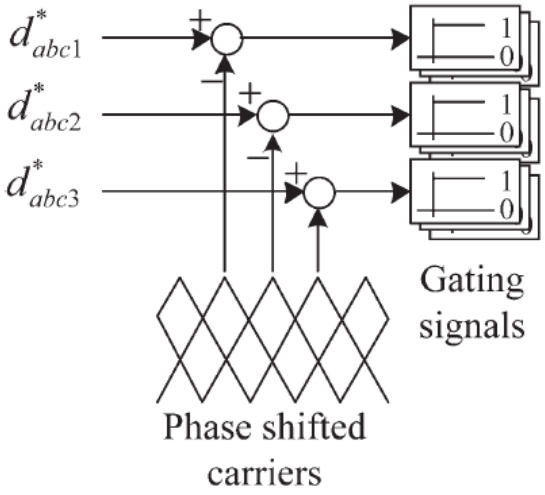

Fig. 10. Comparison of the duty references and the carriers.

IV. RESULTS AND DISCUSSION

The results of traditional sinusoidal are shown in case 1 and 2 and carrier-based supreme, while case III and IV illustrate the waveforms of the proposed method with different ratios of dc link voltages. The basic idea to examine the limitation of the proposed method is to evaluate what conditions bring the different polarities between the original voltage reference and the modified voltage reference by using the proposed method in fig 9, the vertices at π/2 and 3π/2 rad almost come in contact with, but not cross the zero point. However, the directions of the vertices are opposite the original phase voltage

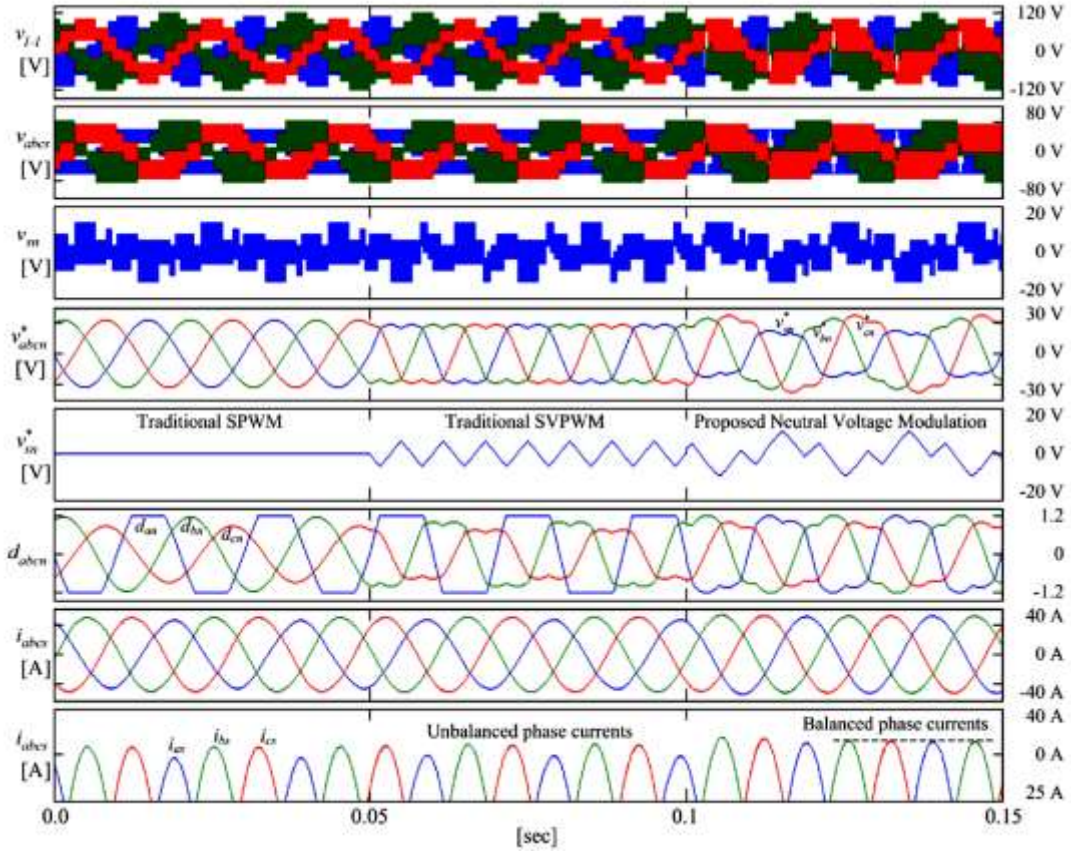

Fig. 11. Simulation result of traditional SPWM, traditional SVPWM, and the proposed method.

CONCLUSION

The NVM proficiency for MLCIs under unbalanced dc-link Conditions have been in this paper. To canvass the maximum limit synthetic voltage of MLCIs, the voltage vector has been enquired using the changing function. From the analysis, the maximum additive modulation range was derived. The NVM proficiency is employed to achieve the maximum modulation index

in the linear intonation range beneath an unbalanced dc-link consideration as well as to balance the Output phase voltages. Equalized to the old methods, the proposed proficiency is easily carried out and ameliorates the output voltage quality under unbalanced dc-link conditions. Both simulations based on the IPM motor drive application verify the effectiveness of the method.

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