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Design and Analysis of 45nm 8T SRAM

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Abstract : A rather more serious effect caused by high leakage current in memory element is an important constrain for the functionality failing of the SRAM cell. Due to the presence of leakage current occurs the data retention fault, when the memory cell loses its previously stored value owing the leakage current. There are two types of RAMs. These are Static RAM (SRAM) and Dynamic RAM (DRAM). SRAM design with different number of transistors but DRAM transistor design with single transistor. SRAMs are classified based on the number of transistors used in this design i.e 6T, 7T and 8T SRAMs. During the write operation into 6T SRAM cell has a limitation i.e. poor write stability and during the read operation into 7T SRAM cell has a limitation i.e. poor read stability. Many SRAM cells have been proposed for improving stability of read and write operation. The basic idea for improving the read and write stability is to separate the bit line pins from storing nodes. The read as well as write operations of SRAM have great stability if circuit is designed by using 8 transistors.

IndexTerms **- SRAM, 6T SRAM, 8T SRAM, Read Stability, Write ability**

I. INTRODUCTION

The structure of 8 transistors SRAM which is shown in below Figure 1 used for design of proposed 8T SRAM. The single ended 8 transistors SRAM design having high stability in read operation. It also utilizes a single bit line as well as the two separate word lines Write Word Line (WWL) and Read Write Line (RWL) for write and read operation. The SRAM design has two cross coupled inverters. The left inverter has 3 transistors P2, N1, N3 while the right inverter has 2 transistors P1 and N2.

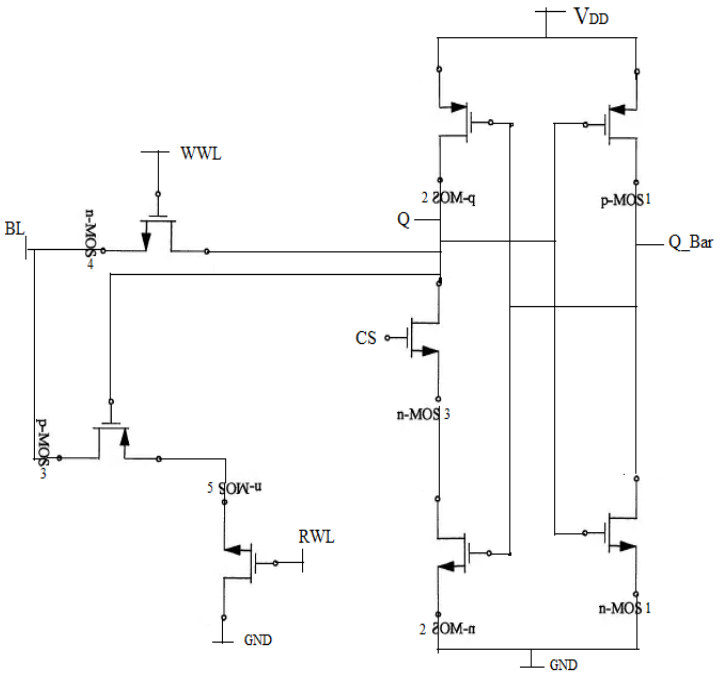

Fig. 1. Schematic of 8T SRAM cell.

II. PROPOSED 8T SRAM

The proposed design uses an extra transistor of CS for cutting off the feedback in cross coupled inverters. In this SRAM cell the read and write operation are controlled by separate word lines, which enhance the write ability and read stability of the cell. The Write Word-Line WWL is used for transferring data from single bit-line BL to Q. Later, the inverted information is stored at QBAR. When Read Word Line RWL is activated, the bit line BL is used for transferring the data from the memory cell as the output during read operation.

2.1 Write Operation

For write operation, the bit line is charged to VDD, and writes word line is pulled high. During write operation, the CS is maintained at 0V, for retaining the stored content at node Q. During write '0' the bit line is maintained at ground and signal CS at VDD, so that the charge is stored at node Q and can easily be inverted from 1 to 0.

2.2 Read Operations

Before initiating the read operation, the BL is precharged to VDD while WWL and RWL are set as 0V and VDD. In the SRAM cell, the storing node Q is connected directly to the PMOS (P_3) transistor. During read 1 operation P_3 transistor gets turn off due to stored 1 at Q, RWL is activated. The precharged BL does not get discharged due to turn off state of P_3 transistor, and 1 is read by sense amplifier.

2.3 Hold Operations

During hold operation, both the word lines WWL and RWL are off. The bit line is charged at VDD and CS is maintained at VDD. The existing design has more power dissipation.

III. DESIGN OF 8T SRAM

The design of SRAM with 6 Transistors, first launched the Generic Process Design Kit with Specific Size (GPDK_Specific Size) technology. Then created the Electronic Design Automation-Process Design Kit-GPDK_Specific Size. Next one path created from CDS library. Then open the terminal window by right clicking. Create new file and design a circuit by using drag and drop method. The flow diagram of 6T SRAM design is shown in Figure 2.

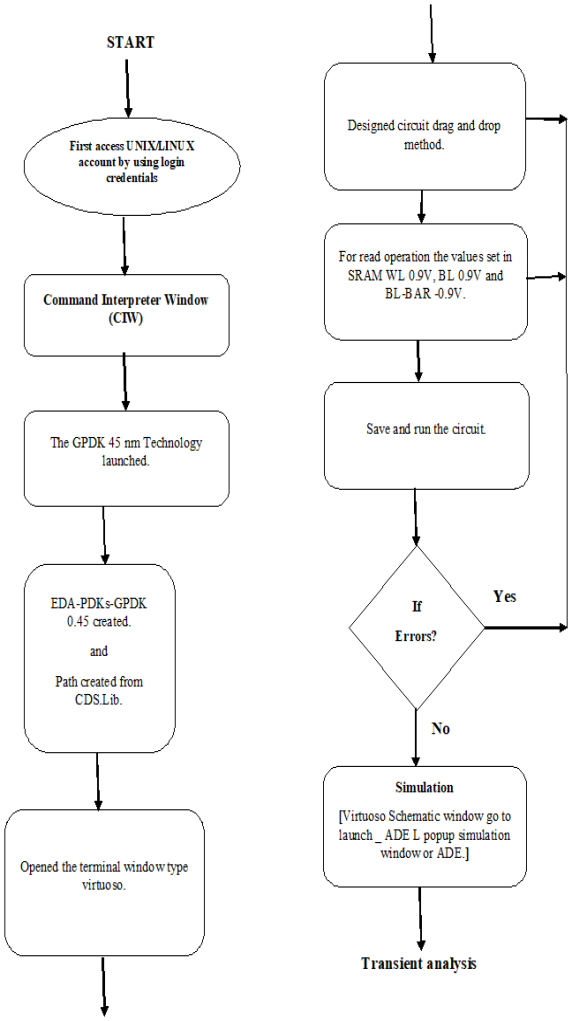

Fig. 1. Flow Chart of design of the 6T SRAM.

IV. RESULTS

For measuring static power consumption bit sequences inserted properly at bit line pins BL and BL_bar. The static power analysis of SRAM design with 8 Transistors in three nanometric technologies are described with following graphs. The Read

operation and Write operation in each memory cell performed as: write '0' [When data is either '0' or '1'], write '1' [When data is either '0' or '1'], Read '0', Read '1'.

To improve the stability of Read and Write operations in SRAM design used extra access transistors. Due to using extra transistors in design of SRAM improves the leakage current while performing Read and Write operations. In this proposed SRAM design improved the Read and Write stability by using extra access transistors but increases leakage power. The performance of 8T SRAM during read and write operation given in below table 1.

Table 1 Table Type Styles

Circuits	Area (nm2)	Power (W)	Current (A)	Delay (nS)
8T-SRAM – Read	43200	8.374n	9.0305n	0.201
8T-SRAM - write	43200	27.947u	31.052u	0.3088

V. CONSLUSION

For improving both Read and Write stability of the basic 6T SRAM cell included an extra access transistors to 6T SRAM circuit. Designed SRAM with 8 Transistors in 45nm technology. The increasing transistor count in SRAM design provided better Read and Write stability, but increased area, static power, leakage current and delay.

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