IMPLEMENTATION OF 64-BIT MAC UNIT USING VEDIC MATHS AND REVERSIBLE LOGIC GATES

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Abstract: In this paper 64 bit Multiply and Accumulate Unit (MAC) is implemented by using Vedic Multiplier and Reversible Logic Gates. A Vedic multiplier is composed by utilizing the algorithm called Urdhava Triyagbhayam sutra. The reversible logic gates are used to design the adder and they are major prerequisite for the developing field of Quantum processing. The more performance and lesser silicon area are obtained by using the Vedic multiplier by reducing the partial products .The less power is obtained by using the reversible logic. The HDL-Verilog code is used for the MAC design. The simulation and synthesis is done in Xilinx 14.1 ISE design suite.

IndexTerms **- Urdhwa Tiryabhyam Sutra, Kogge Stone Adder, Vedic Multiplier, MAC unit.**

1. INTRODUCTION

The Multiply and Accumulate unit is a hardware unit that performs the basic arithmetic operations like addition, subtraction and also calculus operations. The Mac takes the multiplier and multiplicand as its input and it consists of three blocks. The Mac output and one adder input will join and it forms the multiplication unit, another input of the adder, multiplier unit are joined by accumulate register. Microprocessor, Logic unit and DSP are main applications of the MAC unit. The designs obtained by MAC are non linear in nature they are discrete cosine or FFT. The entire speed of addition operation and multiplication operation of the system decides performance and whole speed. Long multiplication process creates critical delay and propagation delay exhibits to the parallel addition in the adder. The multiplier is more significant and its operation is very fast for this reason multipliers plays very important role in designing of the digital processors.

2. MAC ARCHITECTURE

MAC unit is a hardware unit that performs computation of two numbers and its operation is represented as follows

$$X \leftarrow X+(Y*Z) \quad \ldots\ldots\ldots\ldots (1)$$

MAC unit calculates the product of 2 binary numbers and join that result to an accumulator unit. It consists of three blocks namely multiplier, adder and accumulator as shown in the figure 1. Combinational logics are used to implement the multiplier and adder is followed by the multiplier which is used to add or join the 2 binary numbers and finally stores the result in accumulator stage. For each clock pulse the output of accumulator is fed to the adder input at that time output of the multiplier is added to the accumulator stage. More number of logic are required for combinational multiplier but it calculates the product very rapidly compare to shifting and adding method. Digital signal processors are the first processors which are planned by Mac units.

2.1 vedic multiplier-urdhwa tiryabhyam sutra

This algorithm is otherwise called vertical and transversely algorithm. In this algorithm partial products computation takes only one step hence it doesn't require the shift operation .The important goal of this algorithm is save time and total power. This technique is time, region and force efficient. The Urdhva-Tiryakbyham algorithm is used for the larger multiplication operations; it offers better performance contrast to further algorithms.

Generalized Algorithm for Urdhva-Tiryakbyham sutra

Let us take two N binary bit numbers A and B are inputs where n=1, 2, 3 …N. where A =$a_{n\ldots\ldots\ldots\ldots}a_1,a_2$, a_3 and B= $b_{n\ldots\ldots\ldots}b1,b_2,b_3$.The output is represented as S of (n+n) bits where S= $s_{(n+n)\ldots\ldots\ldots\ldots}s_1,s_2,s_3$.The algorithm consists of three steps are given below.

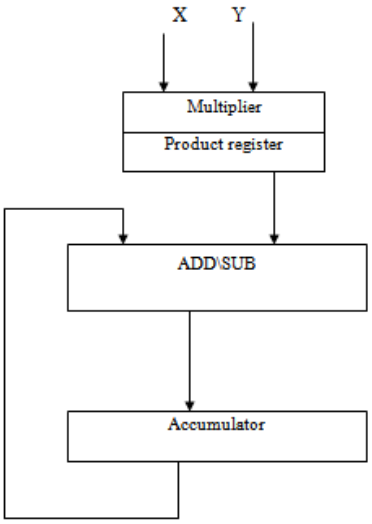
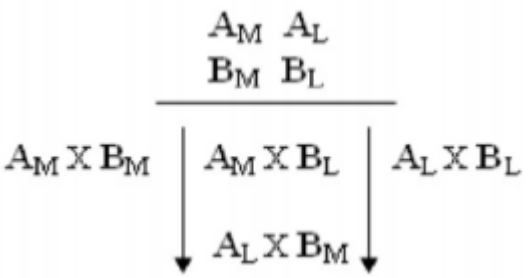


Fig 1: Design of MAC unit

Step 1: The multiplicand A and multiplier B divide into 2 equal parts. One part is represented as [N to N/2+1] bit and another is represented as [N/2 t0 1] bit respectively. First bit points MSB and last bit points LSB.

Step 2: A is written as A_M and A_L.B is written as B_M and B_L.

Step 3: The general format is given as below



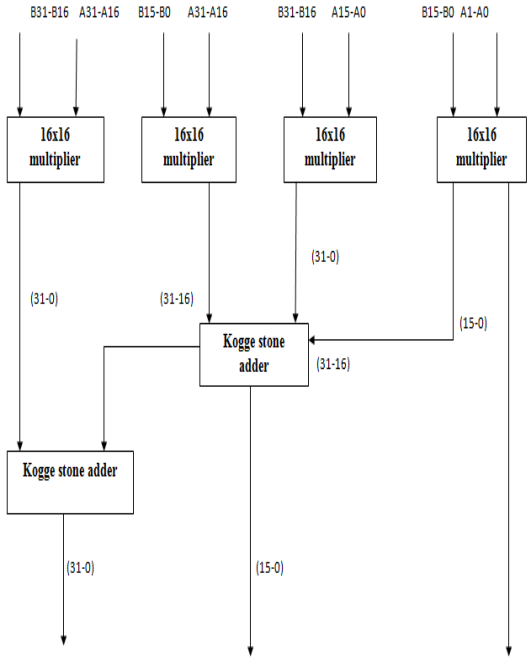


Fig 2:32*32 MAC unit with Kogge stone adder

3. KOGGE STONE ADDER

KSA is a collateral prefix invert adder and it's one of the speediest adders hence it's widely used in industry. The Kogge stone has minimum argumentation depth, maximum fork count, and negligible fan out. While a high fork number infers a bigger zone, the low rationale profundity and negligible fan-out permit quicker execution. KSA consists of three different parts as shown in the below fig3.

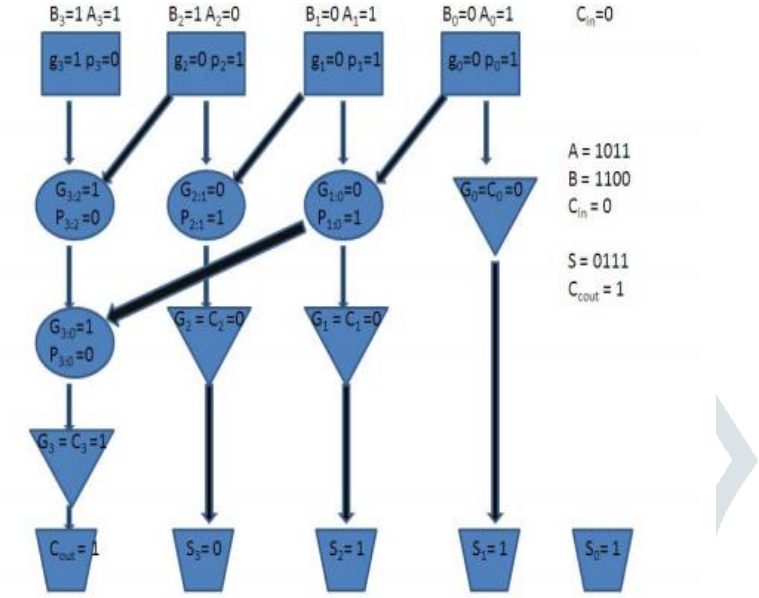


Fig 3: Different working blocks of Kogge stone adder

4. RESULTS

In this section implemented result for MAC unit using Kogge stone adder and multiplier is displayed in fig 4 and RTL view of the MAC unit is displayed in fig5.

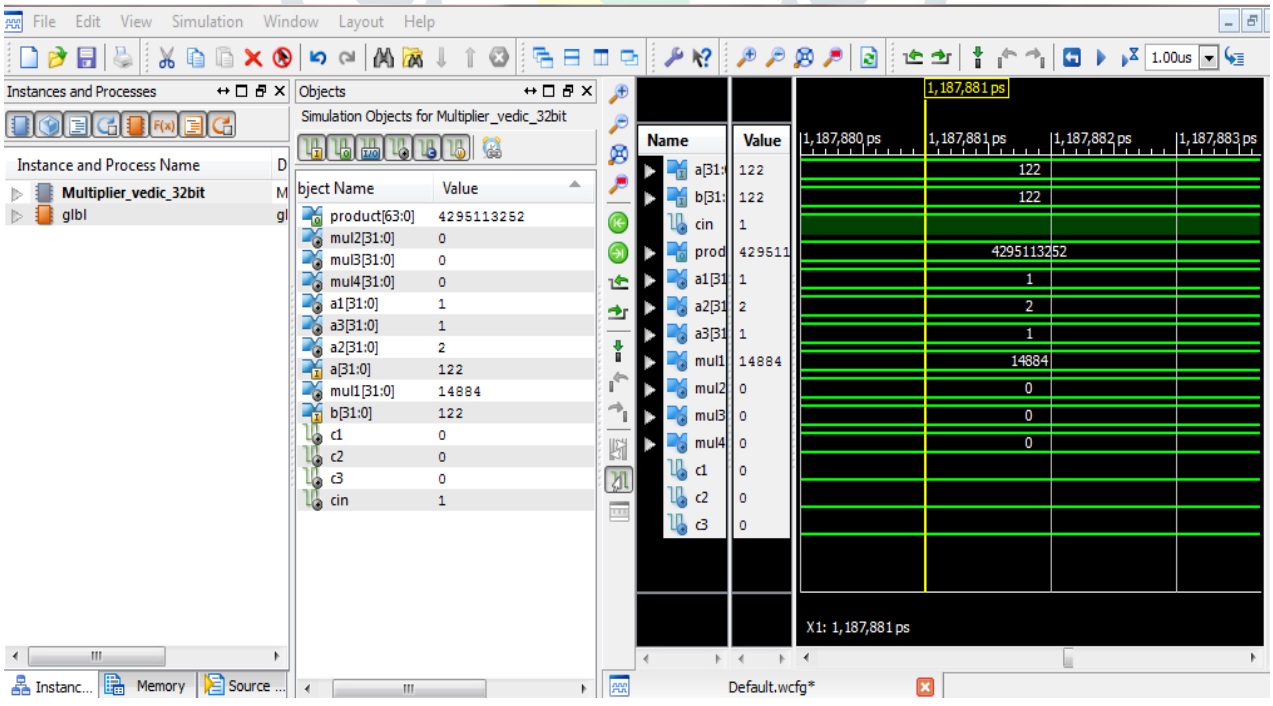


Fig 4: Simulation results of 32*32 MAC Unit

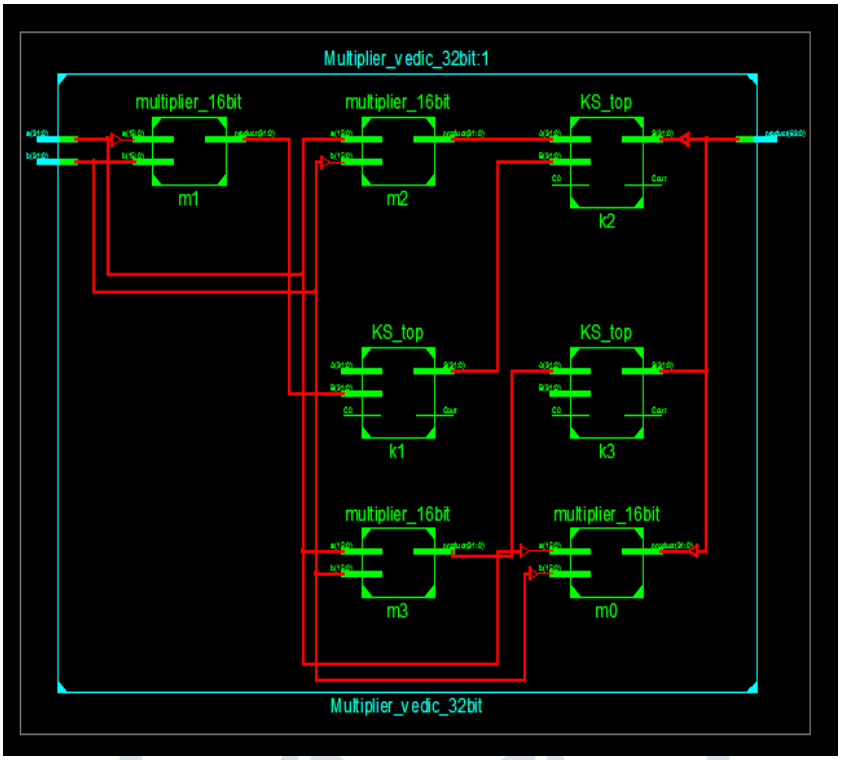


Fig 5: MAC with Kogge stone adder RTL view

5. CONCLUSION

From this project we can conclude that the outcome obtained by Vedic multiplier with 64 bit and reversible barrier is very great. The work exhibited depends on 64 bit MAC unit with multipliers.MAC is a essential building for multiplication operations and its amalgation for all units, hence Uradhva-Tiryakbhayam with 64 bit invert rationale and multiply and accumulate unit is best in all views are velocity, zone, many sided quality.MAC unit is basic basement for different designs and other perspectives. Consolidating the Vedic maths and reversible rationale will prompt new and proficient accomplishments in creating different fields of Mathematics and science.

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