Performance Analysis of ZETA Topology Based Electronic Ballast Over SEPIC Topology for Fluorescent Lamps

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Abstract-This paper presents a low THD based electronic ballast which consists of a ac-dc converter with power factor correction at the input stage, buck-boost ZETA topology, and a high frequency dc-ac inverter at the output side. The electronic ballast is based on a high frequency waver signal, which shapes the input current in a sinusoidal form and produces the output current with low THD. The simulation of high power factor (PF) electronic ballast for a fluorescent lamp are carried out with constant dc link voltage and analyzed with the performance of the existing SEPIC topology. A half bridge series resonant parallel loaded type of inverter is used in the power conversion stage to supply constant current to the lamp. The power quality measures such as total harmonic distortion (THD), power factor (PF) and crest factor (CF) are measured to verify the expected and satisfactory performance of the proposed topology.

Index Terms - Power factor, Crest factor, Total harmonic distortion, Constant lamp power, High switching frequency

I.INTRODUCTION

Lighting plays an important role in all the aspects (industrial, commercial, domestic convenience, etc). Besides various types of Lamps, Fluorescent Lamp is commonly used for its efficiency and low power consumption. The conversion of electric power into light is more effectively carried out in a fluorescent lamp through a ballast. The cost of fluorescent lamp is higher than the cost of incandescent lamp, but energy saving is achieved through fluorescent lamps.
The lamp ballast has two main functions:

- To provide a initial thrust and
- To limit the current flowing through the lamp in its acceptable range.

There are two types of ballasts: inductive ballasts and electronic ballasts. The electronic ballasts are more efficient than inductive ballasts. Inductive ballasts have to be operated in conjunction with starters for lamp ignition. Electronic ballast operates at high frequencies from 20kHz to 50kHz hence it does not need any separate starter to provide initial ignition. These Electronic ballasts uses electronics circuitry to optimize the performance of the lamp. Electronic ballasts for fluorescent lamps becoming more common due to its superior performances. A typical Fluorescent lamp drive consists of a various power conversion stages is shown in Figure. 1, which should provide satisfactory lamp operation, desirable power factor and efficiency of the energy drained from grid. The electromagnetic interference (EMI) filter is attached with the input stage to eliminate the harmonic components generated by the high frequency switching of the PF correction (PFC) stage, otherwise, high-frequency harmonics can decrease the system PF and cause interference problems with other equipment.

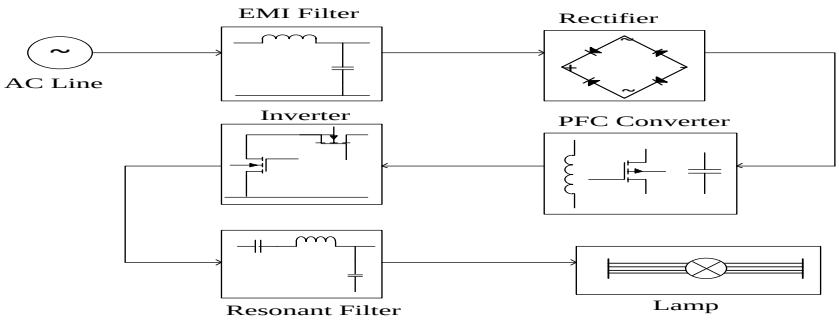

Figure.1 Typical Electronic Ballast

The requirements for this first conversion stage will depend on the selected power converter and design methodology. This circuit typically employs a half-bridge inverter to generate the square waveform which is applied to the resonant load and sets the lamp operating frequency .For analyzing the performance of both proposed and existing topologies Total Harmonic Distortion ,Crest Factor (1.7 for fluorescent lamps) and power factor have been measured.

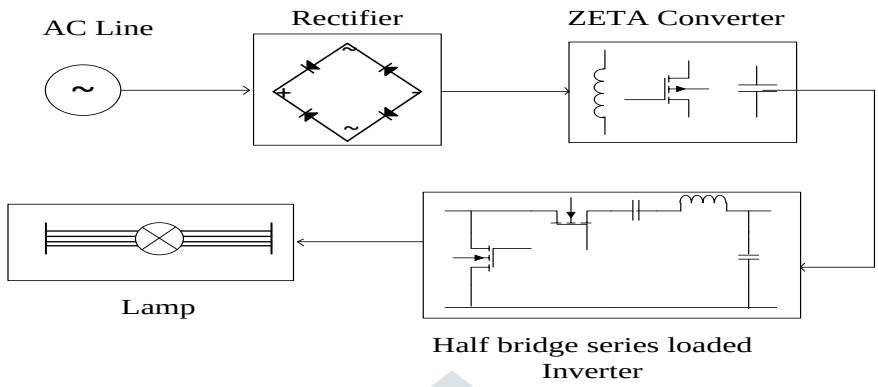

Figure .2 Block Diagram of Proposed system

In the proposed method ZETA converter is used in the PFC stage and in the power control stage,the half bridge parallel loaded inverter is used. The inductor connected in the input stage is used to reduce the ripples in the input current,in turn enhances the power factor at the input stage. The half bridge inverter maintains the lamp operate in the lamp frequency. Figure. 3 shows the circuit diagram of the proposed system of electronic ballast.The ac-dc converter makes the input ac current to follow the ac mains voltage in order to achieve the nearly unity power factor at input stage and the dc-ac inverter gives the enough voltage to ignite the lamp henceforth provides constant lamp current at high frequency to maintain proper illumination.

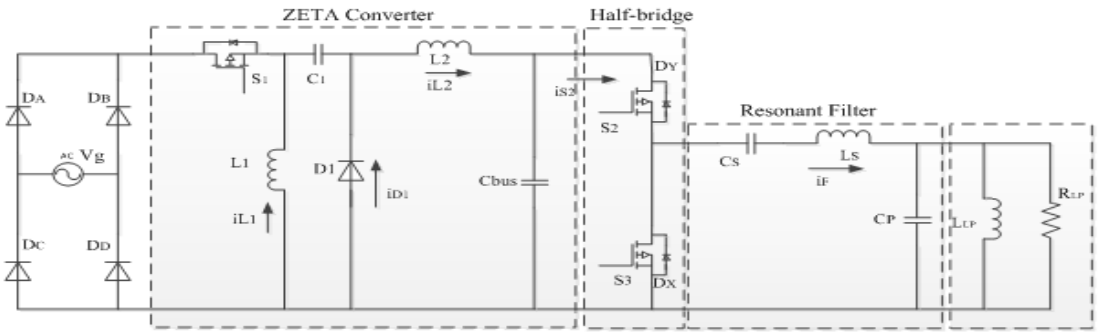

Figure.3 Circuit diagram of ZETA topology based electronic ballast

In the proposed electronic ballast, the selection of proper converter is made based upon the following considerations.

1) An energy storage element should be present between a PFC ac-dc converter and a lamp-driving dc-ac inverter in order to prevent the lamp current to be directly controlled by the ac mains voltage. For this purpose, a capacitor is preferred over an inductor due to its low loss, cost and size.
2) A voltage fed inverter is used as a lamp-driving dc-ac converter to save filter components.
3) Low ac mains voltage should be stepped-up to produce a high voltage to initiate lamp ignition without using a boost-up transformer.
4) The DC link voltage should be maintained constant with respect to a wide variation of input ac mains voltage.

As per the considerations made above, a ZETA topology is chosen as the PFC converter and a half bridge series resonant inverter is used to drive the lamp. Fig. 3 shows the proposed electronic ballast derived from CCM controlled ZETA converter and half bridge series resonant parallel loaded inverter (SRPLI).The power switches MI and M2 are alternately turned on and off at a 40 kHz frequency. The switching frequency of the resonant inverter is maintained more than the resonance frequency of the load circuit to achieve the ZVS (Zero Voltage Switching), which reduces the high frequency switching losses.

II. ZETA TOPOLOGY

ZETA converter, consists of an output capacitor, C_2; coupled inductors L_1 and L_2; an AC coupling capacitor, C_1;a power PMOSFET,Q; and a diode, D. To understand the voltages at the various circuit nodes, it is important to analyze the circuit at DC when both switches are off and not switching. Capacitor C_1 will be in parallel with C_2, so $C_1$is charged to the output voltage,

V_{OUT}, during steady-state CCM. Fig 2 shows the volt ages across L_1 and L_2 during CCM operation. When Q is off, the voltage across L_2 must be V_{OUT} since it is in parallel with C_2. Since C_2 is charged to V_{OUT}, the voltage across Q when Q is off is V_{IN}+ V_{OUT}; therefore the voltage across L_1 is $-V_{OUT}$ relative to the drain of Q. When Q is on, capacitor C_1, charged to V_{OUT}, is connected in series with L_2; so the voltage across L_2 is $+V_{IN}$, and diode D sees V_{IN}+ V_{OUT}. The currents flowing through various circuit components are shown in Fig 3. When Q is on, energy from the input supply is being stored in L_1, L_2, and C_1. L_2 also provides I_{OUT}. When Q turns off, L_1's current continues to flow from current provided by C_1, and L_2 again provides I_{OUT}.

III. SRPLI - PC STAGE

The SRPLI is normally referred as the symmetric half-bridge and uses one of the resonant tank capacitors (C_b in the Fig 4) to block the dc voltage level of the square wave generated by the bridge. This means that capacitor C_b will exhibit a dc level equal to half the dc input voltage superimposed on its normal alternating voltage. A transformer can also be used in this inverter to step the input voltage up or down to the required level for each application. In this case the use of the series capacitor C_b prevents any dc current from circulating through the primary winding, thus avoiding transformer saturation. This topology is often used by ballast manufacturers to supply fluorescent lamps, especially in the self-oscillating version, which allows drastic reductions in cost. When supplying hot cathode fluorescent lamps, the parallel capacitor C_p is normally placed across two electrodes, in order to provide a preheating current for the electrodes and achieve soft ignition.

IV . DESIGN SPECIFICATIONS

L_r,C_b and C_p are the resonant circuit parameters and R_{lamp} is the steady state resistance of the fluorescent lamp. The purpose of C_b (blocking capacitor) is to block the dc component otherwise they can distort the lamp current. Likewise each parameter has been choosed for their satisfactory performance. The formulas for calculating the parameters are given in [1].

Table 1. Design Specifications

Parameters	Specifications
Input RMS voltage ,Frequency	220 V,50 Hz
Switching frequency, Duty cycle	40 kHz, 0.57
Output power, Efficiency, ripple current	60 W,85%,15%
PFC stage output voltage	110-120 V
Lamp Parameters	
R_{lamp}	400Ω
L_{lamp}	630µH
ZETA converter parameters	
L_1, L_2	3.2mH, 194 µH
C_1, C_{bus}	12 nF, 33 µF
Resonant elements	
L_r	2.68 mH
C_b	95 nF
C_p	6.6 nF

V.SIMULATION AND RESULTS

Simulink model of SEPICTopology based Electronic ballast is shown in Figure 4.

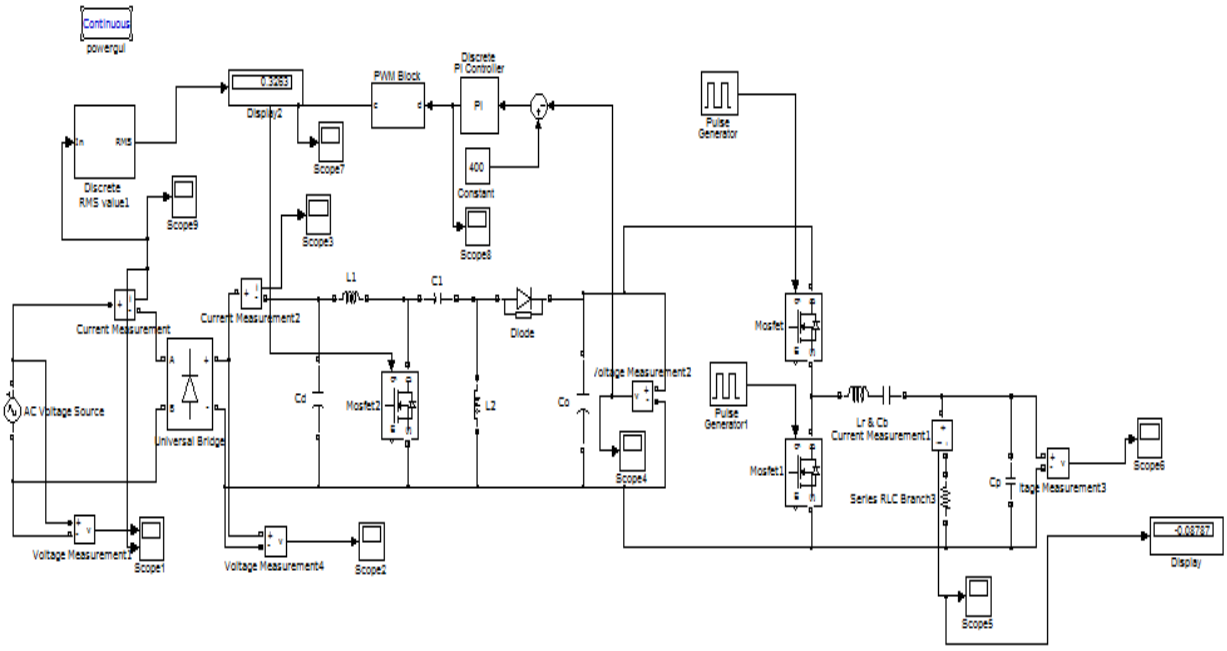

Figure 4 SEPIC topology based Electronic Ballast

OUTPUT WAVEFORMS

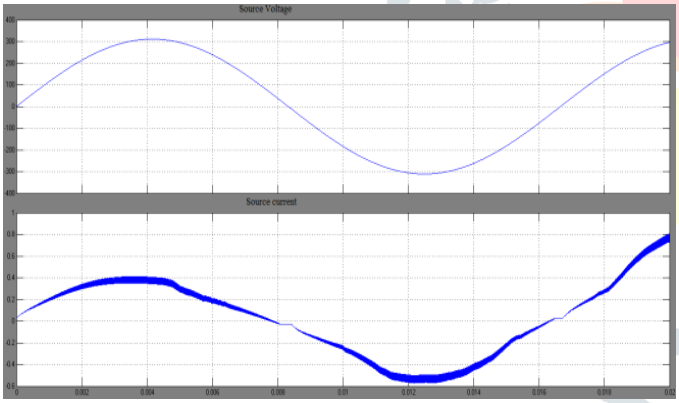

Figure.5 Waveform of Source current and voltage

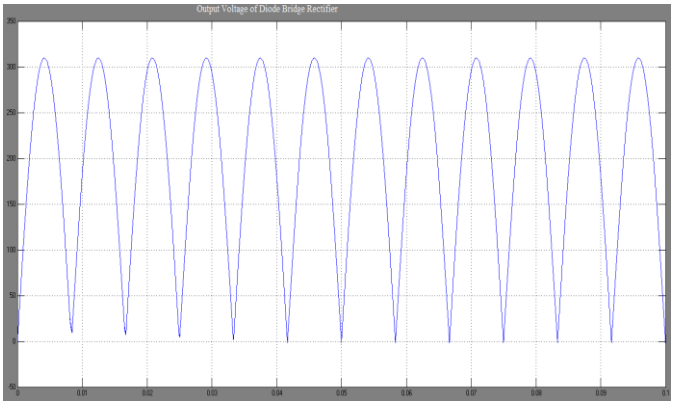

Figure.6 Output voltage Diode Bridge Rectifier

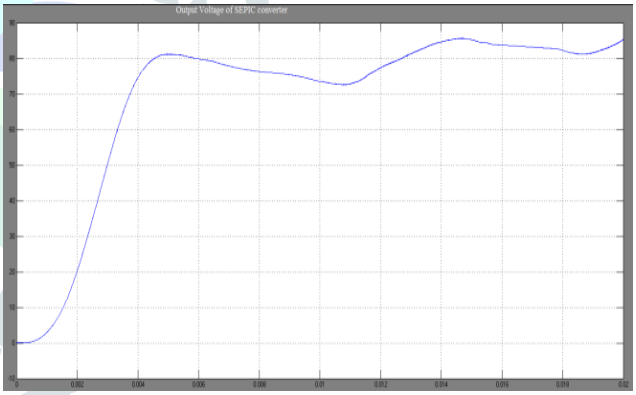

Figure.7 Output voltage of SEPIC converter

THD Analysis of SEPIC PFC based Electronic ballast

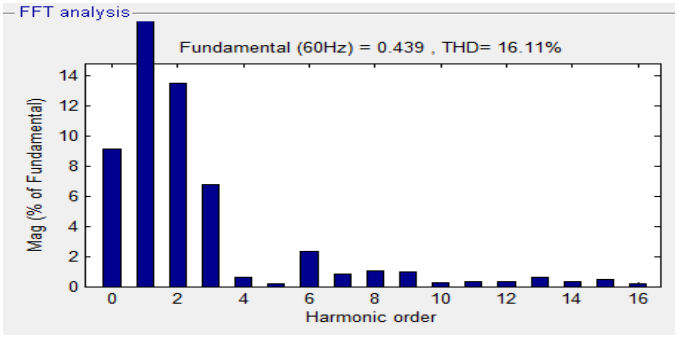

Figure.8 THD analysis of Input Current

The simulation diagram of proposed ZETA topology based electronic ballast is shown in Figure 9.

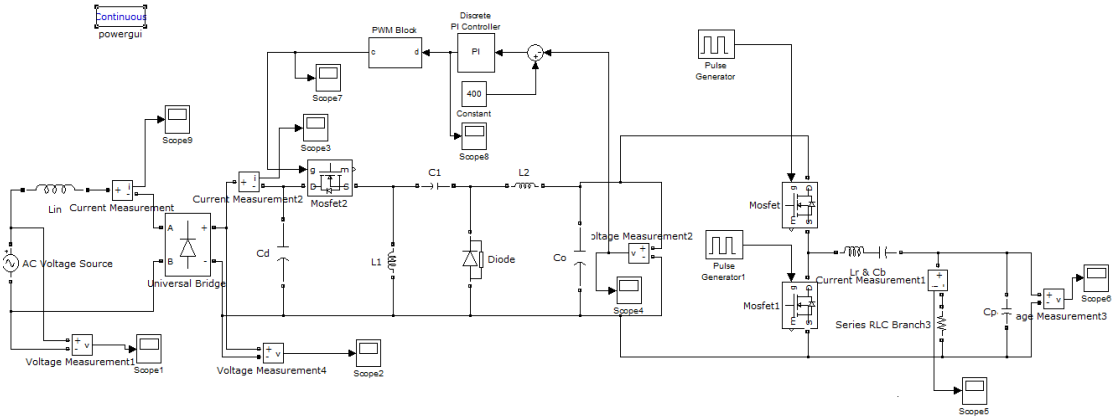

Figure 9 .Simulation of ZETA PFC based Electronic Ballast

Waveforms

The source voltage and current waveform of the proposed topology is shown in Figure 10. The output voltage of the diode bridge rectifier is shown in Figure 11.

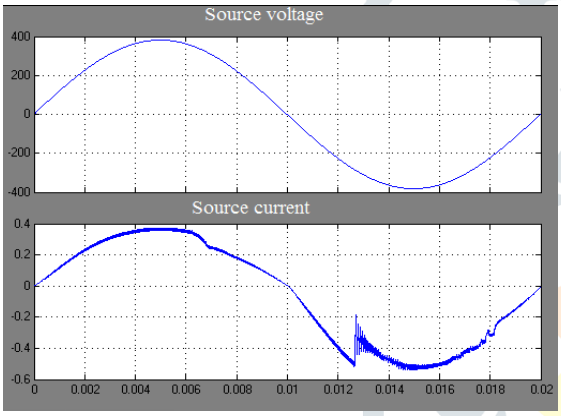

Figure 10. Waveform of Source current and voltage

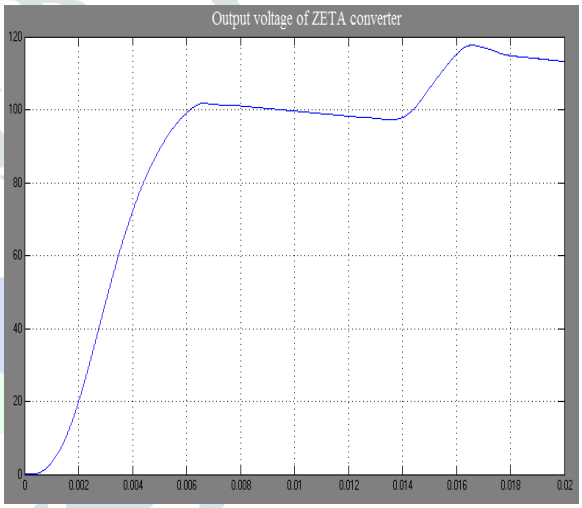

Figure 12. Output voltage of ZETA converter

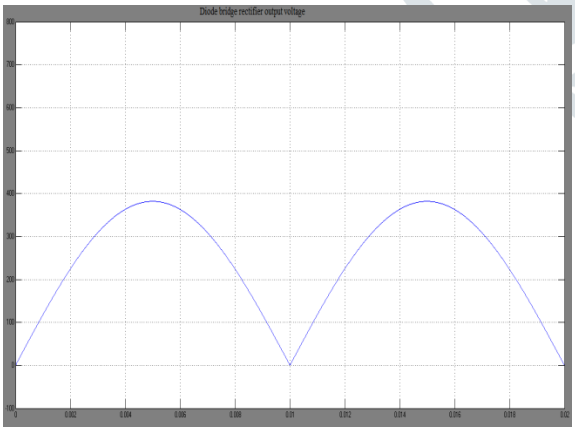

Figure.11 Output voltage Diode Bridge Rectifier

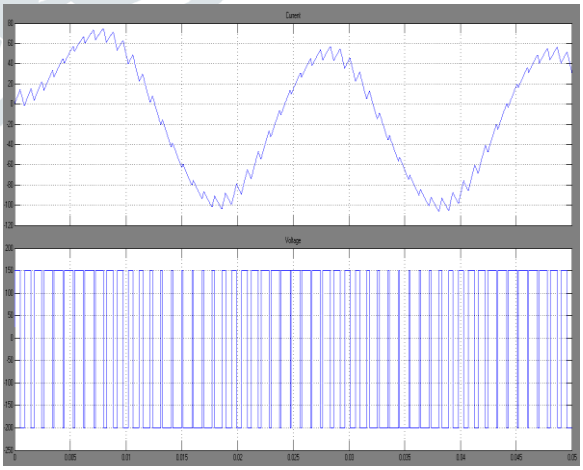

Figure 13.Output voltage of Half Bridge Inverter

THD Analysis of the Proposed System

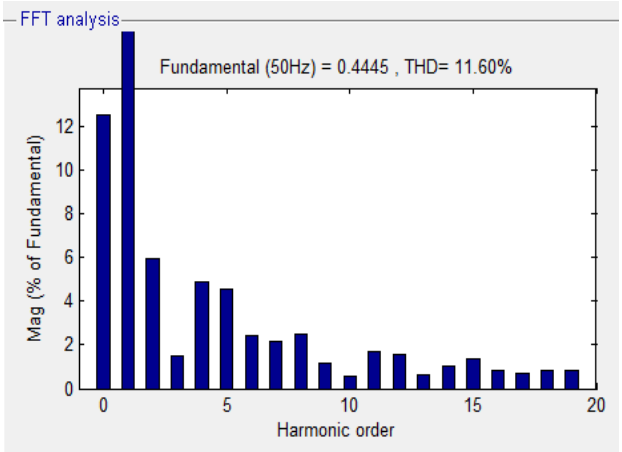

Figure 14. THD analysis of Input Current

The output voltages of ZETA converter and half bridge inverter is shown in the Figures 12 and 13 respectively.The Figure 14 shows the THD analysis of the input current of the ZETA converter based electronic ballasts. The harmonics order is shown that the THD of 11.60% is so obtained from the proposed system.

Table 2. Comparison of Results

Parameter	**SEPIC Converter based Electronic Ballast**	**ZETA Converter based Electronic ballast**
Current THD	16.11	11.60
Crest Factor	1.4501	1.237
Power factor	0.989	0.98

Table 2 shows the comparison of results of SEPIC based electronic ballast in the reference[1] and the proposed ZETA converter based electronic ballast which shows the satisfactory performance of proposed ballast.

VI.CONCLUSION

A CCM controlled ZETA converter with low THD has been proposed for PFC based electronic ballast. The proposed converter can be applied as an electronic ballast for fluorescent lamps as well as medium power supply. The proposed electronic ballast with PFC ZETA converter has shown high performance such as high power factor and crest factor of 1.237 for the wide range of input ac mains voltage. The dc link voltage has been maintained constant, irrespective of the change in ac mains voltage. Moreover, when operating in closed loop, an output power control can be achieved. With an appropriate design of PFC ZETA converter and a resonant converter, the need of electromagnetic interference filter has neglected.

The ballast can withstand the variation in the input voltage and delivers constant power to the lamp thus improving the performance and stability of the lighting by avoiding flickers. The SRPLI is used to deliver a constant power to the lamp and it is self protected against short circuit .The proposed ballast has THD of ac mains current under 11.52% for the universal voltage range of 90V-270V. The zero voltage switching (ZVS) has been ensured because switching frequency is kept more than the resonance frequency of the resonant inverter, which reduces the switching losses and improves the efficiency of ballast.

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