A REVIEW ON CMOS IMAGE SENSORS

[1]Priyanka, [2] Dr. Jyoti Kedia
[1]M.Tech Student, [2]Assistant Professor
[1]Department of Electronics and Communication Engineering,
[1]Punjab Engineering College (Deemed to be university), Chandigarh, India

Abstract: Complementary metal-oxide semiconductor (CMOS) image sensors have attracted attention these days as these devices offer low power consumption and high sensitivity. Its application is not limited only up to digital cameras or mobile on-board cameras but it has tremendous achievements in UV spectroscopy, machine vision, IR vision etc. In this paper, CMOS Image Sensors are reviewed. The difference in charge coupled device (CCD) and CMOS image sensor (CIS) is illustrated on the basis of various performance parameters of an image sensor. A basic architecture of CIS along with the types of pixel structures viz. active, passive and diagonal pixel unit is described. This paper provides information about the latest on-chip Analog to Digital converters (ADCs) as well as the comparison among its types in order to come across the best ADC(s) that could be used to design an efficient imager unit.

Index terms: **CMOS image sensors, CCDs, performance parameters, on-chip ADCs, pixel technologies**

I. INTRODUCTION

The miniaturization of image-acquisition devices has advanced a lot in the past decade. At the center of this miniaturization is the CMOS image sensor (CIS) [1]-[3]. The CIS technology has replaced the charge coupled devices (CCDs) [4] in many areas. One of the most important advantages of CMOS image sensors over CCDs is its ability to integrate sensing with analog and digital processing down to the pixel level.

Imager applications are varied, depending upon the different and changing environment. Recent advances in the design of image sensors implemented in CMOS technologies have led to their adoption in many high volume products, such as the optical mouse, PC cameras, and high-end digital cameras, making them a significant alternative to CCDs or charge coupled devices. Additionally, by exploiting the ability to integrate sensing with analog and digital processing down to the pixel level, various types of CMOS imaging devices are being created for man-machine interface, surveillance and monitoring, biological testing, and among other applications. In spite of having several advantages, CMOS image sensors have a scope of improvement majorly in the field of image distortion and noise shaping.

Charged Coupled Devices (CCDs) which are linear sensors, with an output directly related to the number of photons received and Complementary Metal Oxide Semiconductor (CMOS, or CIS for CMOS Image Sensor) is a newer and parallel readout technology. Both types of imaging devices convert light into electrons (or an electric charge) that can be further processed into electronic signals. CMOS Image Sensors integrate amplification directly in the pixel. The more advanced CIS technology provides a parallel readout architecture, where each pixel can be addressed individually or read out in parallel as a group.

II. CMOS IMAGE SENSOR PERFORMANCE PARAMETERS

There are many parameters that can be used to evaluate the performance of an image sensor. We can classify these parameters using three main metrics:

1. *Pixel Layout:* pixel count, pixel pitch, pixel fill factor
2. *Pixel Physics:* quantum efficiency, well capacity, dynamic range, conversion gain, dark current
3. *Pixel Readout:* signal to noise ratio, frame rate, percentage of linearity, power consumption, bit depth, modulation transfer function, shutter efficiency

When comparing image sensors, either CCD or CMOS, the system is essentially a box where the input is light, and the output is an image based on the light that is seen. The service provided by the sensor is the conversion of light to a digital image. There are a number of common metrics that are used for image sensors. These metrics will be explained below, as well as how they relate to the design of a sensor. These metrics can be used to facilitate an objective comparison of any type of image sensor, and most of them go beyond the notion of raw pixel counts. They will be grouped in three categories, metrics related to the pixel layout, metrics related to the pixel physics, and metrics related to the pixel readout. These categories are not hard and fast categories, as there will be some overlap amongst them.

Parameters Related to Pixel Layout

The most common metric used in comparison of image sensors is the **pixel count**, usually expressed in megapixels, or millions-of-pixels. The number of pixels in a sensor is a function of how large of a chip area the sensor designer has available. The designer must then know much of the chip can be dedicated to the pixels versus how much must be used for digital logic and readout circuitry. A key factor in this decision could be the number of devices used in a pixel. Another metric that goes hand in hand with pixel count is the **pixel pitch**, usually expressed in micrometers-squared or micron-by-micron. Since pixels are created in repeated arrays, the pitch defines how much area each pixel in an array occupies. Typically, the smaller is the pitch, the more pixels that can be fit on the sensor. Smaller pixels, however, will not collect as much light, and thus may not be desirable for high frame rate imagers, or imagers designed for low light observation.

The pixel **fill factor** is another highly used metric that deals with how a pixel is physically laid out. Fill factor is also defined as the ratio of the light sensitive area of a pixel to the total area of a pixel on a digital imaging sensor. A part of the area of an image sensor pixel is always used for transistors, electrodes or registers, which belong to the structure of the pixel of the corresponding image sensor (CCD, CMOS). Only the light sensitive part may contribute to the light signal, which the pixel detects. A fill factor of 100% would be ideal, as then all of the pixel area is used for photo-collection. Most sensors do not have a 100% fill factor, and a sensor designer has many considerations to make when deciding how much of the sensor to leave for the diode, and how much readout or charge transfer circuitry will occupy. Micro lenses may be used to improve fill factor. Micro lenses are lenses that are placed directly on top of the pixel, and they focus the incident light so that more hits the photosensitive portion of the pixel.

Parameters Related to Pixel Physics

Some image sensor metrics are related to the physics of how photons are converted into charges. **Quantum Efficiency** is measure of how many photons are converted into electrons-hole pairs, and is measured as a percentage. It is a function of wavelength, but usually the peak quantum efficiency over the visible spectrum is reported in data sheets. The integrative method of gathering photocurrent is based on the capacitance of the photodiode. The capacitance, in turn, is based on the doping, which are set by the process used in sensor manufacture, the pixel area, set during pixel layout, and the bias voltage, an operating parameter. The size of this capacitance creates a limit on the total amount of charge a pixel can hold during integration. This is referred to as the **well capacity**, measured in electrons. The well capacity leads to another important metric, the **dynamic range**, measured in decibels. The dynamic range is a metric of how well a sensor can measure an accurate signal at low light intensities all the way up until it reaches full well capacity. A higher dynamic range will allow the sensor to operate in more lighting conditions. Related to dynamic range is **conversion gain** which is measure as the change in output voltage with the absorption of one charge. It is proportional to the well size in most cases, as the output voltage is equal to the charge divided by the capacitance. A lower well capacity means a smaller capacitance, and thus a larger voltage change when a new charge is absorbed.

As new processes allow pixels to become smaller and smaller, a source of noise becomes more and more significant. This is **dark current**, measured in fA. Dark current [5] comes from three sources; irregularities in the silicon lattice at the surface of the photodiode, currents that are generated as the result of the formation of a depletion region, and currents that are present because of diffusing charges in the bulk of silicon. This current is added to the current from drift and diffusion in the photo-sensor, so that even if there is no current from external light, the pixel will still measure the dark current. Dark current is a function of temperature, becoming worse as temperatures increase. It is typically listed on data sheets when measured at room temperature.

Due to process variations, the properties of transistors across the pixel array usually vary. The threshold voltages of readout transistors may not match, widths and lengths may not be exactly the same, the doping of the silicon may have gradients, the mobility may also vary from pixel to pixel, and other non-uniformities will be present. These lead to **fixed pattern noise**, that measures how much spatial non-uniformity is present in the sensor.

Parameters Related to Pixel Readout

The reduction of unwanted noise is a very important aspect of image sensor design. Some of the noise could be inherent in the pixel, like shot noise, 1/f noise, and dark currents. Other noise can be present in the amplifiers that are used to convert the photo-voltage into an output signal. In CCD architecture, the charge from each pixel is transferred through a common readout structure, at least in single output port CCDs, where charge is converted to voltage and amplified prior to digitization in the Analog to Digital Converter (ADC) of the camera. This results in each pixel being subjected to the same readout noise. However, CMOS technology differs in that each individual pixel possesses its own readout structure for converting charge to voltage. In the CMOS sensor, each column possesses dual amplifiers and ADCs at both top and bottom (facilitating the split sensor readout).

The **Signal-to-Noise** ratio, measured in dB, is a ratio of how much of the original signal is present at the output, versus how much unwanted noise is present. A higher SNR means more of the original signal is present at the output. Signal-to-Noise ratio usually varies by light intensity, as it is typically lower for dim light and higher for brighter light. Many sensor datasheets report only the peak Signal-to-Noise ratio. **Percentage of linearity** is another metric that is important, as it measures how linear the pixel output is with respect to the incident photo-voltage.

The **frame rate** of an image sensor is the measure of how many times the full pixel array can be read in a second. Many sensors target 24 frames-per-second or higher to be considered real-time. **Power consumption** is another important metric of image sensor design. The choice of supply voltage and pixel clocking frequency can have a large impact on power consumption, since power is measured as the product of the frequency, the capacitance, and the square of the supply voltage. Lower supply voltages mean lower power, at the cost of a decreased voltage range. Typically, the higher the frequency, the higher the frame rate, but at the cost of increased power.

The output **bit-depth** is another metric listed in many image sensor datasheets. Since the photodiode signal is eventually converted into a voltage, the bit-depth measures how much of a change in the output voltage can be reliably measured. Since the number of allowable output levels is $2^{\text{bit-depth}}$, the higher the bit-depth, the more distinct output levels will be. Since image sensors must move charge from pixel to pixel, the **charge transfer efficiency** [6] is a metric that describes the percentage of charge that is transferred from one image element to another.

Following table 1 shows the difference between charge coupled device and CMOS image sensor architectures based upon different performance parameters:

S.NO.	CHARACTERISTIC	CCD	CIS
1	Signal from pixel	Electron packet	Voltage
2	Signal from chip	Analog voltage	Bits(digital)
3	Readout noise	Low	Lower at equivalent frame rate
4	Fill factor	High	Moderate or low
5	Photo-response	Moderate to high	Moderate to high
6	Sensitivity	High	Higher
7	Dynamic Range	High	Moderate to high
8	Uniformity	High	Slightly lower
9	Power consumption	Moderate to high	Low to moderate
10	Shuttering	Fast, efficient	Fast, efficient
11	Speed	Moderate to high	Higher
12	Biasing and clocking	Multiple, higher voltage	Single, low voltage
13	System complexity	High	Low
14	Sensor complexity	Low	High
15	Relative R&D cost	Lower	Lower or higher depending on series

III. CMOS IMAGE SENSOR (CIS)

A typical CMOS imager is an IC with an array of pixel sensors. Each pixel sensor contains its own light sensor and active amplifier. An analog-to-digital converter and other components critical to the operation of the pixel sensors are already located on the CMOS sensor. Light comes through the lens and is processed by the color filter before reaching the pixel sensor array. When the filtered light reaches the pixel array, each pixel sensor converts the light into an amplified voltage signal that can be further processed by the rest of the CMOS sensor.

The architecture shown in following figure 1 of CMOS image sensor has blocks viz. color filter, pixel array, digital control and ADC; however, with the trending technology additional sections for performance enhancement may also vary depending upon the required application.

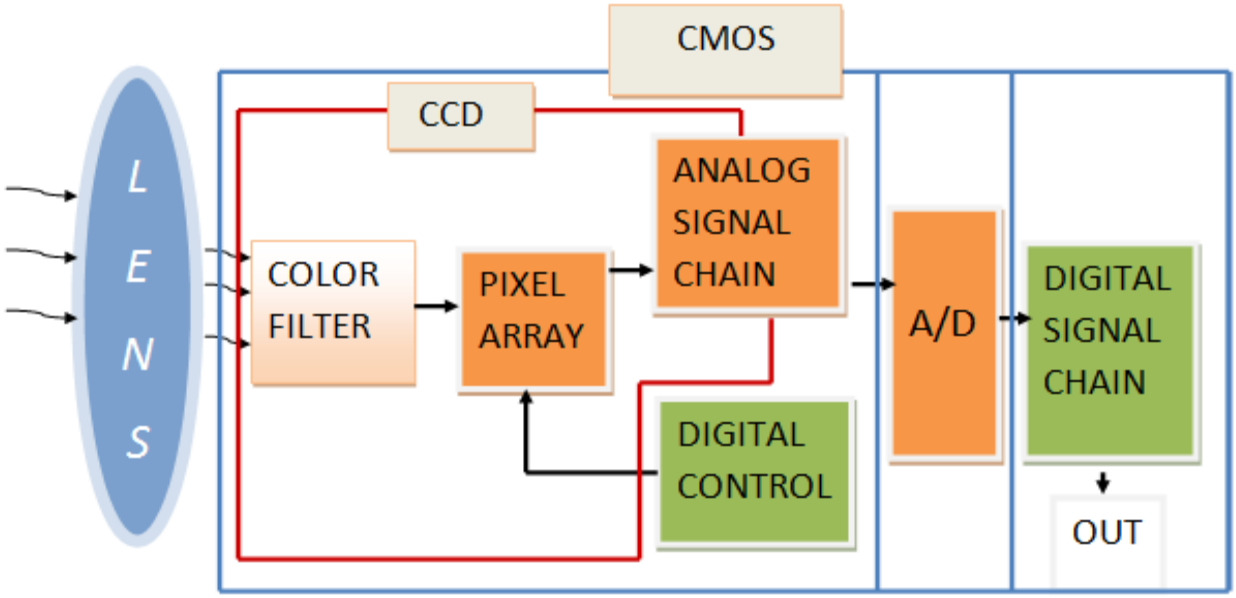

Figure 1: Basic CIS architecture

i. **Color filter:** An array or a mosaic of tiny color filters is placed over the pixel sensor array to capture color information. Color filters are necessary because the pixel sensors can only detect light intensity, and not wavelength, which dictates the color of a light incident to the pixel array.

ii. **Pixel array:** The pixel array consists of millions of active pixel sensors (APS) responsible for capturing the intensity of the pre-filtered light passing through. Each individual active pixel sensor then converts the detected intensity level into a voltage signal before passing it to the other part of the chip.

iii. **Digital control:** The digital controller is the set of circuitry integrated on the CMOS sensor that controls the pixel array. It consists of multiple components, including the clock or timing generator and oscillator to ensure that every pixel in the array is in synchronization with each other.

iv. **Analog to digital converter (ADC):** The ADC takes the analog voltage signals from the pixel sensor array and converts them into the digital signal. The final digital signal is then transferred to an image processor or another device independent of the CMOS sensor which converts or further processes the digital signal into something observable by the end user.

IV. CMOS PIXEL STRUCTURES

CIS is sensitive to environmental noise signals because of a relatively small photocell. In low-light environments, both the image signals and the noise signals are mixed due to which image distortion occurs. To obtain highly efficient CIS, the pixel structure should be such that the dark current blooming in the pixel stages must be less. Dark current in standard submicron CMOS processes is orders of magnitude higher than in a CCD and several process modifications are required to reduce it.

As the range of photocurrents produced under typical illumination conditions is too low (in the range of femto to picoamperes) to be read directly, it is typically integrated and read out as charge or voltage at the end of the exposure time. This operation, known as direct integration, is illustrated in the following figure 2.

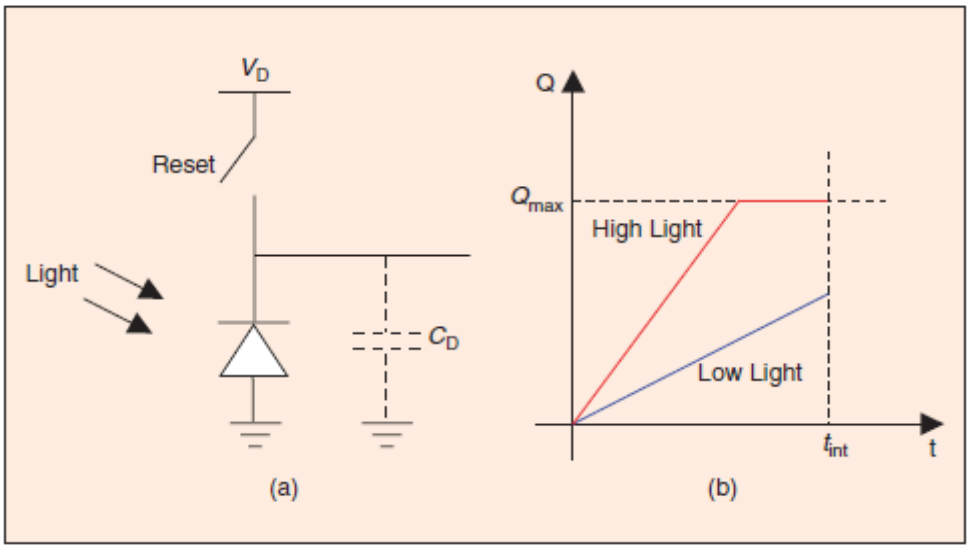

Figure 2: (a) A schematic of pixel operating in direct integration.
(b) Charge versus time for two photocurrent values.

The photodiode is first reset to a voltage VD. The reset switch is then opened and the photocurrent i_{ph} as well as the dark current, i_{dc}, are integrated over the diode capacitance. At the end of integration, the charge accumulated over the capacitance is either directly read out, as in CCDs or PPS (passive pixel sensor), and then converted to voltage or directly converted to voltage and then read out as in APS (active pixel sensor). In both cases, the charge-to-voltage conversion is linear.

The three main types of pixel structures are:

i. Passive pixel sensor (PPS): The PPS pixel in the figure 3 includes a photodiode and a row-select transistor. The readout is performed one row at a time. At the end of integration charge is read out via the column charge-to-voltage amplifiers. The amplifiers and the photodiodes in the row are then reset before the next row readout starts. The main advantage of PPS is its small pixel size. The column readout, however, is slow and vulnerable to noise and disturbances. The APS and DPS architectures solve these problems, but at the cost of adding more transistors to each pixel unit.

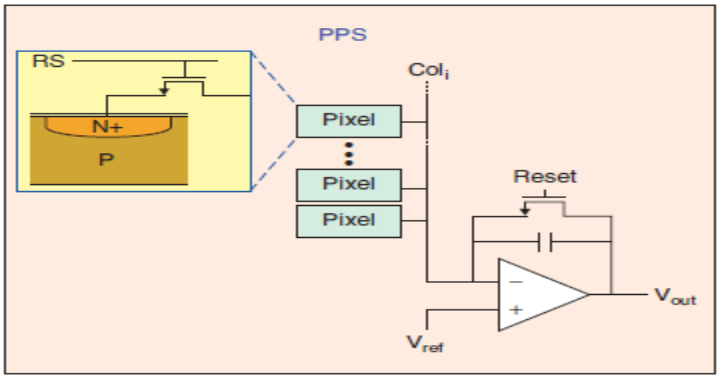

Figure 3: Schematic of PPS

ii. Active pixel sensor (APS): The 3-T APS pixel includes a reset transistor, a source follower transistor to isolate the sense node from the large column bus capacitance and a row select transistor. The current source component of the follower amplifier is shared by a column of pixels. Readout is performed one row at a time. Each row of pixels is reset after it is read out to the column capacitors via the row access transistors and column amplifiers.

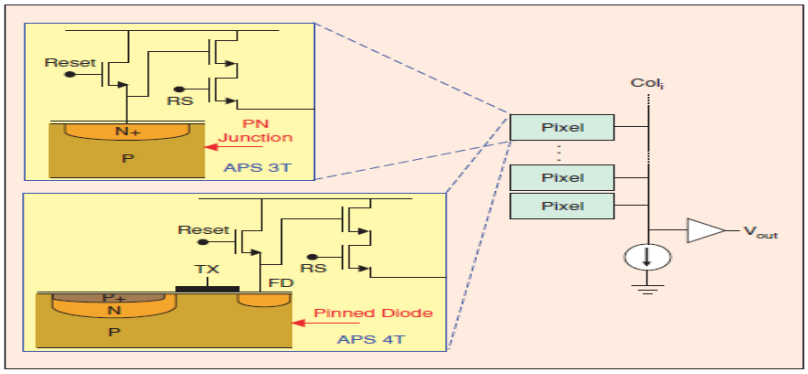

Figure 4: A schematic of a 3- and 4-T active pixel sensor (APS).

The 4-T APS architecture uses a pinned diode, which adds a transfer gate and a floating diffusion (FD) node to the basic 3- T APS pixel architecture. At the end of integration, the accumulated charge on the photodiode is driven to the FD node. The main purpose of the extra transistors in the APS pixel is to provide signal buffering to improve sensor readout speed and SNR. By appropriately setting the gate voltage of the reset transistor in an APS pixel, blooming, which is the overflow of charge from a saturated pixel into its neighboring pixels, can be mitigated. The reset transistor can also be used to enhance the dynamic range (DR) via well capacity adjusting. Each of the APS architectures has its advantages and disadvantages. A 4-T pixel either has a larger or a smaller fill factor than a 3-T pixel implemented in the same technology. On the other hand, the use of a transfer gate and the FD node in a 4-T pixel decouples the read and reset operations from the integration period, which enables true correlated double sampling (CDS).

iii. Diagram pixel sensor (DPS): The most recently developed CMOS image sensor architecture is DPS, where analog-to-digital (A/D) conversion is performed locally at each pixel, and digital data is read out from the pixel array in a manner similar to a random access digital memory. Figure 5 below depicts a simplified block diagram of a DPS pixel consisting of a photo-detector, an ADC, and digital memory for temporary storage of data before digital readout through the bit-lines. DPS offers several advantages over analog image sensors, such as PPS and APS, including better scaling with CMOS technology due to reduced analog circuit performance demands and the elimination of column FPN and column readout noise. More importantly, employing an ADC and memory at each pixel to enable massively parallel A/D conversion and high-speed digital readout, provides great potential for high-speed “snap-shot” digital imaging. The main drawback of DPS is that it requires the use of more transistors per pixel than conventional image sensors, resulting in larger pixel sizes and lower fill factors.

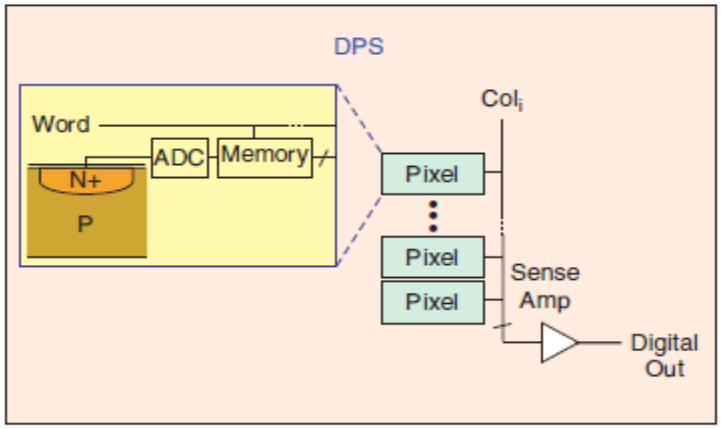

Figure 5: A schematic of a diagram pixel sensor (DPS).

Out of all the above described pixel structures, Active Pixel Sensor (APS) is most widely used in CMOS image sensors. With CMOS transistors as amplifiers, active pixel sensors perform better in obtaining high-quality images as compare to the passive

pixel sensors as they have no amplifier and also they are extremely noisy. The capability that every active pixel of CMOS image sensors can be read out separately also gives it a high read-out speed. It is very easy for CMOS sensors to achieve several hundreds of Mega frames per second (Mfps). So if a phone camera with 8 Megapixels uses this technology, the power it uses for obtaining a frame of image should be around 0.7 mW, that can definitely save energy and keep the camera working for a longer time. APS technology has several advantages over CCD technology, including; lower cost, lower power consumption (100 to 1000 times lower), higher dynamic range, higher blooming threshold, individual pixel readout, single low voltage (5, 3.3, or lower) operation, high speed, large array sizes, radiation hardness, and the smartness by incorporating on-chip signal processing.

V. ANALOG-DIGITAL CONVERTER

As image sensors become more complex, they are using an increasing number of schematics in the analog paths. Large, stand-alone, pipelined ADCs are giving way to single-slope, integrating ADCs that align with the pixel array and contain an ADC for each column of the array. The benefit of this approach is that it allows you to quickly move data off the sensor. Additionally, each ADC[7]-[10], [13]-[14] has a much longer time to operate on a sample, thus allowing longer settling times, lower noise, and higher accuracy.

The varying degree of the light intensity depends on the device that is used as a capture device, which decides the overall performance of a dynamic range(DR) of an imaging sensor. A scheme called as buried NPD is useful in boosting the gain in the sensor dynamic range. The dynamic range is dependent on the full well capacity (FWC) which is defined as the maximum number of electrons of incident light/signal that could be accommodated without saturation during the readout process. Also, the higher FWC sensor improves the noise characteristics of high luminance region as well as sensor DR.

Integrated sensor interface circuits require power-efficient and high-accuracy data converters.

Table 2: Frame rate per bit depth

FREQUENCY	BIT DEPTH(b)	FRAME RATE(frame/s) at 8MP
440 MHz	10	37
	12	16.3
570 MHz	10	40.9
	12	19.7

If the bit-depth of ADC is increased then one can get the full advantage of FWC wide dynamic range sensor but as the bi-depth, say n increases, the conversion time exponentially increases by 2^n and as a result the frame rate of the sensor output may decrease significantly.

To obtain a higher frame rate, there are advanced ADC architectures such as SAR, cyclic, and delta-sigma, which are capable of generating a high frame rate with a high bit depth.

Table 3: N-bit ADC architecture in CMOS image sensor

ADC TYPE	ADVANTAGES	DISADVANTAGES	CONVERSION RATE(TCLK)
SINGLE SLOPE	➢ Low complexity ➢ Small size ➢ Inherently monotonic	➢ High conversion time ➢ No comparator offset cancellation	2^N
SUCCESSIVE APPROXIMATION	➢ Simple control logic	➢ Large size due to N-b D/A	1N

REGISTOR		➢ Large input range ➢ No gain stage	
CYCLIC	➢ Smaller size than pipeline ADC	➢ Larger size due to amplifier	1N
DELTA-SIGMA	➢ Low-noise by noise shaping and oversampling	➢ Need high sampling frequency due to oversampling	OSR-N
PIPELINE	➢ High accuracy ➢ High sampling rate due to conversion time 1 clock	➢ Large size due to pipeline stage	1

OSR: oversampling ratio—the number of times that the actual sampling rate is greater than the minimum Nyquist frequency. ***N***: *N*-bit ADC.

In spite of these, researchers have proposed various circuits that may reduce the non-idealities at a good extent. Following table 4 shows the variation in technology for ADCs in recent years:

PREVIOUS WORKS	**PROCESS**	**ADC TYPE**	**ADVANTAGE(S)**	**DISADVANTAGE(S)**
Tomohiro Takahashi et.al [7]	55-nm CMOS	Array-parallel	Low resolution full scale image High resolution ROI image Massive parallel readout of data	Complex structure 3-D integration techniques are required
Byoung-Kwan Jeon et.al [8]	0.18-µm CMOS	SAR	High resolution Improves ADC Linearity	Higher Power consumption
Hyunkeun lee et.al [9]	0.11- µm CIS	Delta-Sigma	Reduced power Increased fill factor Least FOM factor	Increase in complexity Image distortion
Lee, I et.al [10]	0.18-µm CMOS	Incremental Delta-Sigma	Low power Small size Less power consumption	Less SNDR Complex structure
S.K Hong et.al [11]	0.13- µm CIS	SAR+ Delta-Sigma	Reduced temporal noise	Reduced frame rate

On the basis of this comparison table, it could be found that SAR ADCs and Delta-Sigma ADCs [1]-[2], [11],[12] give the best output in case of CMOS image sensor; as few structures are very complex to design and consume high power as well. In addition to that image distortion and less value of SNDR is also noticed. Though they have some non-idealities but it could be corrected.

Hence, another table could be drawn only for SAR and Delta-Sigma to illustrate their differences more clearly on the basis of comparative study.

Table 5: Comparison between SAR and DSM type ADC

PAPER	Sun-Il Hwang et.al [13]	Seong-Kwan Hong et.al [14]	Chen N. et.al [15]	Shengyou Zhong,et.al [16]
ADC TYPE	SAR	SAR	DSM	DSM
NO. OF PIXELS(M PIXELS)	2.8	1.6	0.48	0.26
FRAME RATE(FRAMES/S)	50	60	50	60
ADC RESOLUTION BIT	10	12	15	12
POWER CONSUMPTION(mW)	50	-	193	50

Based upon the above table, both the SAR ADC and Delta-Sigma ADC are efficient to design an image pixel unit which will have better performance values.

VI. CONCLUSION

CMOS image sensors are among the fastest growing and most exciting new segments of the semiconductor industry. The ability to integrate sensing with processing is enabling a plethora of new imaging applications for the consumer, commercial, and industrial markets. This review mentions the major elements of CMOS image sensors such as pixel structure and ADCs and their types in order to understand the various areas of improvisation. Also, comparison of different analog to digital converters on the basis of frame rate, resolution, power consumption etc. is described. A broad description of various performance metrics is given. Based upon this review, it could be stated that if pixel sensing structure is further modified using either the SAR ADC or Delta-Sigma ADC then there is a scope that performance of CIS may get better.

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