

# Study and Design of 16-QAM Modulator in FPGA: Review of Methods and Implementation.

<sup>1</sup>Juned K. Qureshi, <sup>2</sup>Dr. Ahmed Sajjad Khan,

<sup>1</sup>Masters Student, <sup>2</sup>Professor

<sup>1</sup>Department of Electronics & Communication Engineering,

<sup>1</sup>Anjuman College of Engineering & Technology, Nagpur, India.

**Abstract :** The interest of high data rates in wireless applications keeps on developing at an Exponential rate. The constrained accessibility of range makes accomplishing high information rates in wireless communication testing objective. There are various sorts of modulation techniques to pick from. Quadrature Amplitude Modulation (QAM) has been a prevalent decision for usage. This project will focus on performance analysis of QAM-based wireless communication system with MATLAB Simulink and implementation of QAM based wireless communication system with FPGA kit and the system waveform with FPGA resources will be observed. Designing of the QAM prototype is done by using MATLAB and the same design will be then implemented in HDL.

**IndexTerms - 16-QAM, MATLAB, FPGA, Verilog HDL.**

## I. INTRODUCTION

The improvement in the balance procedures had been seen since most recent two decades which requests dependable transmission of data with higher information rate. Because of progressively resistible to noise advanced tweak systems have made an intrigue. At present FPGAs and ASICs are assuming a crucial job in designing, simulating, testing and executing the new correspondence methods. Arrangements based on field programmable Gate Arrays (FPGAs) are appealing since they empower update establishment over a system from a focal site. FPGAs let engineers optimize fixed-point word lengths and pack numerous channels into a solitary gadget, accordingly diminishing the effective power and cost per channel. Other than their field programmability, speed, and adaptability.

Quadrature amplitude modulation (QAM) is commonly used balance procedure in the present wireless communication scheme. Choosing a higher order format of QAM permits more bits of data per symbol; likewise the information rate can be increased along these lines achieving more noteworthy separation between nearby points in the I-Q plane by distributing the points more similarly. 16-QAM is a sort of advanced digital modulation framework which transmits four bits for each symbol on two orthogonal carriers; one in phase and the last one is quadrature phase. In this manner the data rate is expanded by a factor of four. It gives high information rate for transmission. The proposed work in this project presents a complete design for a 16-QAM transmitter based on the MATLAB simulink and implementation of the design on a FPGA Kit.

## II. THEORY

The essential manner by which a QAM signal can be created is to produce two signals that are 90° out of stage with one another and afterward aggregate them. This will produce a signal that is the aggregate of the two waves, which has a specific amplitude coming about because of the total of the two signs and a phase which again is reliant upon the total of the signals. In the event that the amplitude of one of the signs is balanced, at that point this influences both the phase and amplitude of the overall signal.

QAM (Quadrature Amplitude Modulation) gives some critical advantages to information transmission. As 16QAM changes to 64QAM, 64QAM to 256 QAM, etc, higher data rates can be accomplished, however at the expense of the noise margin. The transmission rate can be additionally expanded by utilizing Mary QAM which is a blend of multi-amplitude Shift keying (MASK) and Multiphase move keying (MPSK). One practical case with M=16 uses the following 16 pulses (16 symbols), equation (1) shows that:[3]

$$P_i(t) = a_i p(t) \cos \omega_c t + b_i p(t) \sin \omega_c t \quad (1)$$

$$= r_i p(t) \cos(\omega_c t - \Theta_i) \quad i=1,2,3,\dots,16$$

$p(t)$  is a properly shaped baseband pulse. The signal  $p_i(t)$  can be generated using QAM by letting  $m_1(t) = a_i p(t)$  and  $m_2(t) = b_i p(t)$ . One possible choice for 16 pulses is shown graphically in figure 1.[3]

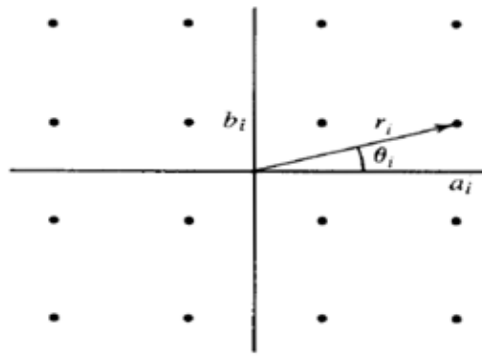


figure 1: 16-point QAM (M=16)[3]

**III. REVIEW OF METHODS TILL NOW**

Till now various methods used to implement QAM in FPGA are discussed in R. Swain and A. K. Panda proposes journal design of 16-QAM[2] concluding that there still lot of work can be done in implementing QAM on FPGA. He finished up saying that, models so far designed are only considering the design issues. The model he proposed has two random integer generators that are utilized as data source. Likewise, the mapping block compromises of adder and multiplier blocks. His procedure additionally requires a counter, two ROMS and a Mixer. Mixer here is basically a complex number multiplier. This design can be used for design issues like suitable coding. Fig 2, shows the block diagram:

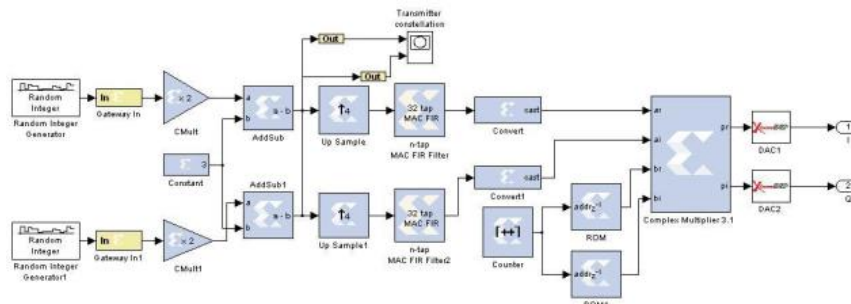


figure 2: System generator based 16-QAM transmitted Model.[2]

Another Scheme proposed in Anareen A. G., Anjana R. M., Aparna V.G., Deepika C. S, FPGA Implementation of QAM [1] QAM modulator was actualized in FPGA with client controllable information message signal. It very well may be utilized in the execution of Software Defined Radios. they used a Spartan 3 XC3S400 FPGA kit and the output was obtained on DSO using DAC 0808.

Then the third scheme studied Tarig H. M., Ali M. M., Ghasn M T Abdalla, Implementation of 16- QAM Transmitter and Receiver on FPGA [3] mostly focused on the two main transmitter functions, data mapping and intermediate frequency shifting. They used Source block to produce 4-bit input signal, then by using Xilinx Bit Slice Extractor Block they sliced the input signal in two inputs one in phase(I) and the other in Quadrature(Q). Then a counter and a multiplier is used for counting the values and multiplying 4 different amplitude coefficients. In the receiver section they used counter and two ROMs are used to generate sine cosine oscillations. Additionally, they used Low pass Filter, filtering was done by the FIR compiler and FDA tool. Proposed transmitter block diagram is shown in Fig 3 and the receiver block diagram is shown in Fig 4:

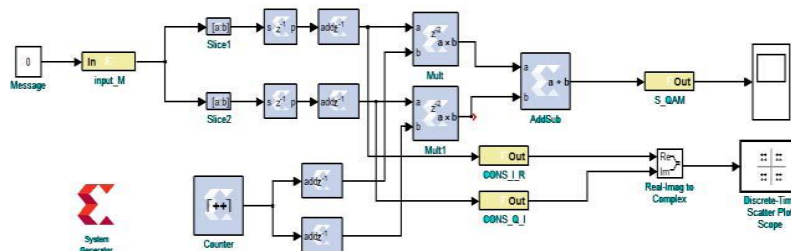


figure 3: Proposed 16-QAM Transmitter Model.[3]

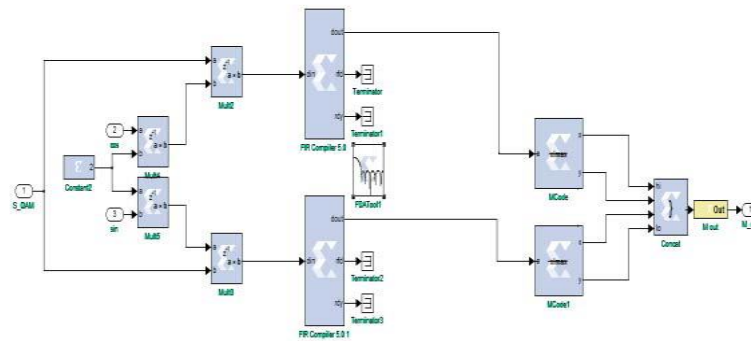


figure 4: Proposed 16-QAM receiver Model.[3]

**IV. PROPOSED SYSTEM**

The interest of high information rates in remote applications keeps on developing at an Exponential rate. The constrained accessibility of range makes accomplishing high information rates in remote communication challenging objective. High information rates are fundamental for requesting applications such a real-time video streaming. High throughput is acknowledged through tradeoffs between bandwidth, power, and framework intricacy. In modulation process, the parameter of the carrier wave is differed as per the modulating signal. There are a wide range of sorts of modulation techniques to pick from. Quadrature Amplitude Modulation (QAM) has been a prominent decision for execution. Hence this venture proposes an examination and plan of a 16-QAM digital modulation framework first in matlab then on FPGA through hardware descriptive language.

This project will concentrate on performance analysis of QAM-based wireless communication framework with MATLAB Simulink and usage of QAM based wireless communication framework with FPGA kit and the system waveform with FPGA kit will be watched. Designing of the QAM prototype is done by using MATLAB and the same design will be then implemented in HDL.

The random integer generator uniformly distributes random integer in the range [0,M-1],where, M is a set size. And it is either a scalar or a vector. Additive White Gaussian Noise(AWGN), it is the transmitter and receiver intermediates in which noise is added to the signal. BER= no. of bit error / Total no of transmitted bits during a time interval. The block Diagram for 16-QAM is shown in Fig 5:

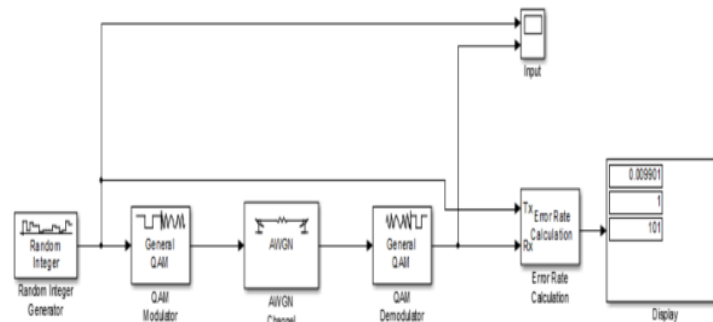


figure 5: Simulink based model of 16 QAM.

The obtained waveform are shown in the Fig 6 and Fig 7, the simulation are done using HDL(Hardware Descriptive Language) to provide the binary message PN sequence generator was used and carrier signal values were stored in the lookup tables.

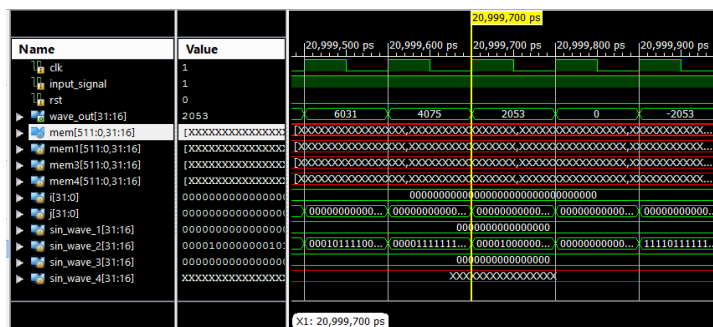


figure 6: HDL Simulated Waveform.

