ANALYSIS OF POWER CONVERSION EFFICIENCY OF BUCK CONVERTER OPERATING IN CONTINUOUS CURRENT MODE

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Abstract: This paper presents a detailed analysis of the power conversion efficiency of a low voltage high-frequency buck converter operating in Continuous current mode. The Matlab-Simulink models of a buck converter with mathematical efficiency model are built to analyze the effect of the variation of power conversion efficiency with respect to load, input voltage, switching frequency and the equivalent resistance of LC filter. Maximum efficiency of 91.01% is obtained at 0.3A of load current. The variation of the efficiency of a buck converter with respect to switching frequency is studied under light load and heavy load conditions. It is observed that power loss mainly comprises of conduction losses under heavy load conditions and switching losses under light load conditions. The Power efficiency of the buck converter is reduced from 92.21% to 69.05% at 1MHz switching frequency as the load is reduced from 800mA to 2mA.

IndexTerms **- Switching mode power supply, Efficiency, Continuous current mode, Buck converter, Conduction losses**

I. INTRODUCTION

With the continuous technology development in the field of Integrated circuits, it is possible to have more and more functionality on a single chip called System on Chips (SoCs). Such a complex system on chip (SoC) requires sophisticated power supply schemes to provide constant low-voltage over a widely varying load-current range and operating conditions with high efficiency. Power demands are growing with the sheer size and complexity of contemporary SoC devices. Power consumption has a critical impact on IC performance, and therefore, its management is important. Ineffective power supply circuitry causes lower chip performance, increases area and makes the design non-functional. The current trend of power supply for SoC is around 1V and this trend of reduction of the power supply is continuing. Also, it is essential to take care that power supply circuitry consumes minimal power as it has a major impact on IC performance. With the growing power management concern in high-performance SoCs, the requirement for efficient power supply circuitry has become a critical design challenge for product success. The current generation SoCs requires supply voltages in the range of 1V or less for their operation.

There are several types of power supplies used to deliver power at desired voltage level such as linear regulators and switched regulators. Traditionally SoC has been powered by linear regulators. They are simple, ripple-free and occupy less area. However, they suffer from poor conversion efficiency. On the other hand, the switching mode power supply delivers power at high efficiency. With the recent advancement in VLSI design and CMOS fabrication process, it is now possible to implement advanced control technology to obtain ripple free, stable output voltage to supply electronic loads [1].

In this paper, Design of DC-DC converters for supplying power to SoC is considered. DC-DC converter should be able to keep high efficiency throughout the entire operating range to extend the standby time and the battery using time. The converter inputs are generally unregulated dc input voltage and the desired outputs should be a constant or steady voltage irrespective of variation in load current or input voltage. In addition to providing a constant output voltage, a DC-DC converter should be able to operate with a high conversion efficiency. Therefore, constant output voltage and high conversion efficiency are the two crucial problems to design the DC-DC converter. The research work presented in this paper focuses on the design of digital power supply regulators for low voltage, low power SoCs. Considering battery with a voltage in the range of 1.8V to 3.6V as a supply source, a switch mode power supply namely buck converter is employed to down-convert the battery voltage to 1V to drive SOCs. The buck converter operates at a high switching frequency of 10MHz which reduces area requirement and makes it suitable to drive high-speed SoCs. The analysis of the power conversion efficiency of buck converter operating in continuous current mode (CCM) with respect to load, switching frequency, and resistances of the LC filter is performed in detail.

This paper is organized as follows. The buck converter and its operating modes are explained in Section II. Section III describes the various losses that take place in a buck converter. In Section IV, Results and its analysis are shown. Section V summarizes the conclusions.

II. BUCK CONVERTER: PRINCIPLE AND MODES OF OPERATION

A switching buck converter is a step-down converter which converts a higher supply voltage to one of a lower level. The buck converter is usually operated in closed loop control to supply a constant voltage irrespective of changes in load current and supply voltage [2]. Traditionally, the switching buck converter is controlled by pulse-width modulation (PWM). The output voltage Vout is determined by the on-time ratio of the driving PWM signal, known as the steady-state duty cycle D and is written as

$$D = \frac{V_{out}}{V_{in}} \qquad (1)$$

It consists of an inductor, capacitor, and two switches. The circuit operates in two modes namely ON and OFF states. Fig.1 shows the schematic diagram of a buck converter. The MOSFET Q1 is called the main switch as it connects the Inductor to main supply and MOSFET Q2 is called synchronous switch as its switch condition is in synchronous with main switch Q1.

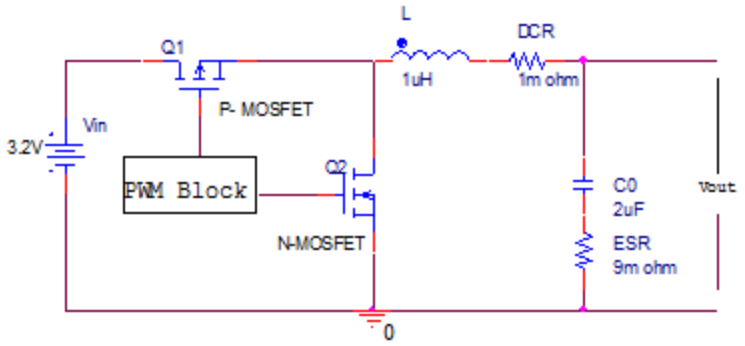


Fig.1 Schematic Diagram of synchronous Buck converter

When Q1 is on and Q2 is off, the input voltage appears across the inductor and current in inductor increases linearly and in the same cycle, the capacitor is charged. When the transistor Q2 is on and Q1 is off, the voltage across the inductor is reversed. However, current in the inductor cannot change instantaneously and the current starts decreasing linearly. In this cycle also the capacitor is also charged with the energy stored in the inductor. The capacitance reduces output voltage ripple acts as a low pass filter. The average output voltage V_0 is lower than that of input voltage V_g. Typically Q1 and Q2 are MOSFETs and their ON and OFF states are controlled by using Pulse Width Modulation (PWM) techniques. By varying duty cycle(d) of the PWM pulses applied to switches Q1 and Q2, the desired output voltage is obtained($V_o = d\ V_{in}$)

Buck converter can operate in continuous or discontinuous mode during ON and OFF state. In continuous current mode (CCM), the current through inductor flows continuously and it never falls to zero. For most of the buck converter applications, CCM mode is advantageous when the maximum load current is high. In discontinuous current mode (DCM), the current through inductor falls to zero and remains zero for some portion of the switching cycle. It starts at zero, reaches peak value and returns zero during each switching cycle. This mode becomes advantageous for the applications where the maximum load current is low.

In this paper, a buck converter operating in CCM is considered. The design of the buck converter starts with LC filter design[2]. The minimum value of inductance L required to operate the buck converter in CCM is given by

$$\mathrm{L} = (\mathrm{V_{in}} - \mathrm{V_{out}}) \times \frac{\mathrm{V_{out}}}{\mathrm{V_{in}}} \times \frac{1}{\mathrm{f_{sw}}} \times \frac{1}{\mathrm{I_{LR}} \times \mathrm{I_{out(max)}}} \qquad (2)$$

Where I_{LR} is the inductor current ratio expressed as a percentage of output load current I_{out} and f_{sw} is the switching frequency of the buck converter.

Output capacitance is required to minimize the voltage overshoot and ripple present at the output of a buck converter. The output capacitance C_o in CCM is calculated as:

$$C_O = \frac{L(I_{out(max)} + \frac{\Delta I_{inductor}}{2})\text{^}2}{(\Delta V + \mathrm{V_{out}})^2 - (\mathrm{V_{out}})\text{^}2} \qquad (3)$$

The DC resistance (DCR) and Equivalent Series resistance (ESR) of Inductor and capacitor of LC filter greatly influences the efficiency of the buck converter and their values are chosen such that efficiency is higher with the ripples in output voltage and inductor current are within the limits of 1% and 20% respectively. The MOSFET characteristics such as ON resistance and various parasitic capacitances are taken into considerations while designing the buck converter for high efficiency. Table I shows the specifications of buck converter under study.

TABLE 2.1 BUCK CONVERTER SPECIFICATIONS

Parameter	Minimum	Nominal	Maximum
Input Voltage (V_{in})	1.8 V	3.2 V	3.6V
Output Voltage (V_{out})	0.9V	1 V	1.2V
Output current(I_{out})	2mA	-	800mA
Switching frequency (f_s)	-	10MHz	-
Output inductor (L)	-	1uH with DCR=1mΩ	-
The output capacitor (C)	-	2uf with ESR=9mΩ	-
P-Channel MOSFET R_{onP}	-	160mΩ	-
N-Channel MOSFET R_{onN}	-	70mΩ	-

III. POWER LOSSES OF A BUCK CONVERTER IN CONTINUOUS CURRENT MODE

The power conversion efficiency of a buck converter can be expressed as:

$$\eta = \frac{P_{out}}{P_{out} + P_{LOSS}} \quad (4)$$

Where P_{Loss} is the total power loss in a switching buck converter which can be classified as conduction losses, switching losses. Power losses will be different for CCM and DCM modes of operation due to the different elements that are active during its operation. In this paper, the losses occurring in CCM only will be discussed.

3.1 Conduction Losses

During the continuous conduction mode where the load current is relatively large, the main contribution of power losses is the conduction loss of the on-resistance of high-side (R_{onP}) and low-side(R_{onN}) switches and the series resistance of the inductor and the capacitor (DCR, ESR)[3][4].

The main and synchronous switches are turned on and off depending on the duty cycle. Hence, the average resistance for these switches can be expressed as the on-resistance multiplied by the duty cycles. The on-resistance in one switching cycle is written as

$$R_{swon} = R_{onP} * D + R_{onN} * (1 - D) \quad (5)$$

The conduction loss due to on-resistance inside the MOSFET is given by

$$P_{switchesOn} = R_{swon} {I_{out}}^2 \quad (6)$$

Where I_{out} is the RMS value of the output current.

The non-ideal inductor has series resistance DCR which contributes to power loss when current passes through it. In steady-state, the average inductor current is also the same as the load current. The power loss due to the inductor series resistance is given by

$$P_L = DCR * (I_{out} + \Delta I_{inductor} * \sqrt{2})^2 \quad (7)$$

Where DCR is inductor resistance, I_{out} is the load current and $\Delta I_{inductor}$ is the variations in inductor current.

For a capacitor, ESR is the main cause of power loss and is written as

$$P_C = (\Delta I_{INDUCTOR} * \sqrt{3})^2 * ESR \quad (8)$$

3.2 Switching Losses

The power switches conduct momentarily during the turn-on and turn-off transient. The high voltage across the power switch and the current that flows through it can cause significant loss which is referred to as hard switching loss. As the MOSFET switches from ON to OFF or vice-versa, the voltage across its drain and source and the current flowing from drain to the source would have a time window during which voltage and current are nonzero. Thus, hard switching power loss of a switch can be written as

$$P_{swLoss} = 0.5 * V_{in} * I_{out} * [t_{off} + t_{on}] * f_s \quad (9)$$

Where t_{off} is the time taken for the current to fall down to zero when ON gate voltage is removed and V_{DS} goes to high whereas t_{on} is the time taken for the current to rise when ON gate voltage is applied and V_{DS} goes low[6][7].

The power loss in the gate drives is predominantly the dynamic power used to charge and discharge parasitic capacitors of the power transistors. Since the power switch size is relatively large to handle the load current with proper on-resistance the capacitance associated with it at the switching node could be quite significant. The gate drive loss is written as

$$P_{GateDrive} = V_{in}^2 * f_{sw} * (C_{gN} + C_{gP}) \quad (10)$$

Where C_{gN} and C_{gP} are the gate capacitance of P and N channel MOSFET.

The dead-time is the amount of time that both MOSFETs are off. It is used when there are two complementary PWM signals (one on when the other is off) so that main and auxiliary switches are not conducting simultaneously. The dead time is an important parameter in the analysis of the efficiency of buck converter [10][11]. The more dead time, the less efficient the converter will be since during that period it is not actually doing anything at all. But, if the dead time is too short. the shoot- through problem can the damage the MOSFET. During this time the diode or parallel Schottky diode is in forward conduction. Its power loss is given as

$$P_{dt} = V_d * t_{deadtime} * f_s * I_{out} \quad (11)$$

IV. Results and Discussion

Fig.2 shows the Digital PWM controlled buck converter operating in CCM mode. The buck converter is modeled using state-space averaging principle[5][8][9]. The closed-loop control is implemented in digital mode. The buck converter load current is varied between 0.001A to 10A and the corresponding variations in Efficiency, Conduction loss, and switching loss are studied.Fig.3 shows the plot of Efficiency, conduction loss and switching loss which are normalized to total loss with respect to the load current. Maximum efficiency of 91.05% is obtained at a load current of 0.3A. The efficiency decreases drastically as low load current as switching losses become predominant at light load. The conduction losses contribution is more at heavy load where switching loss at light load.

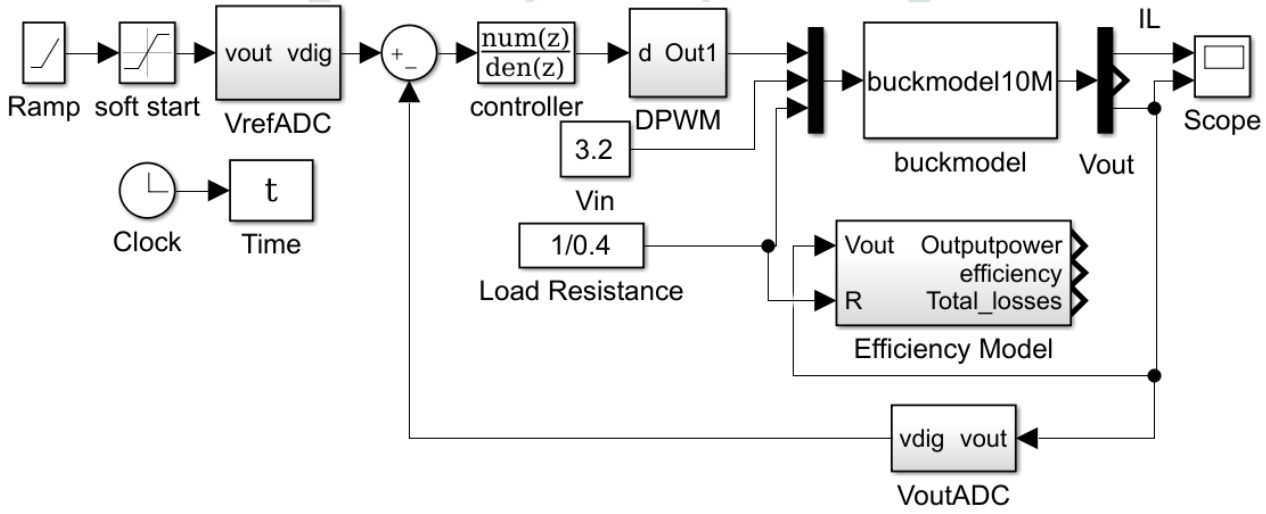


Fig.2 The implementation of Digital PWM controlled Buck Converter

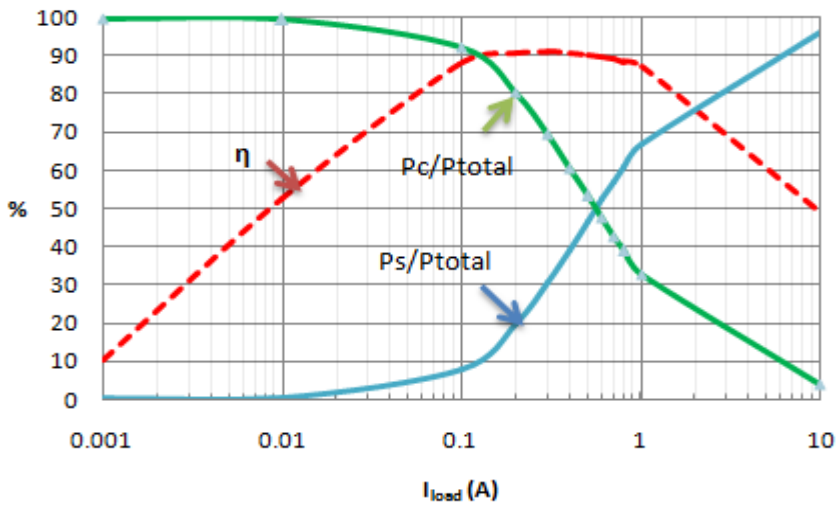
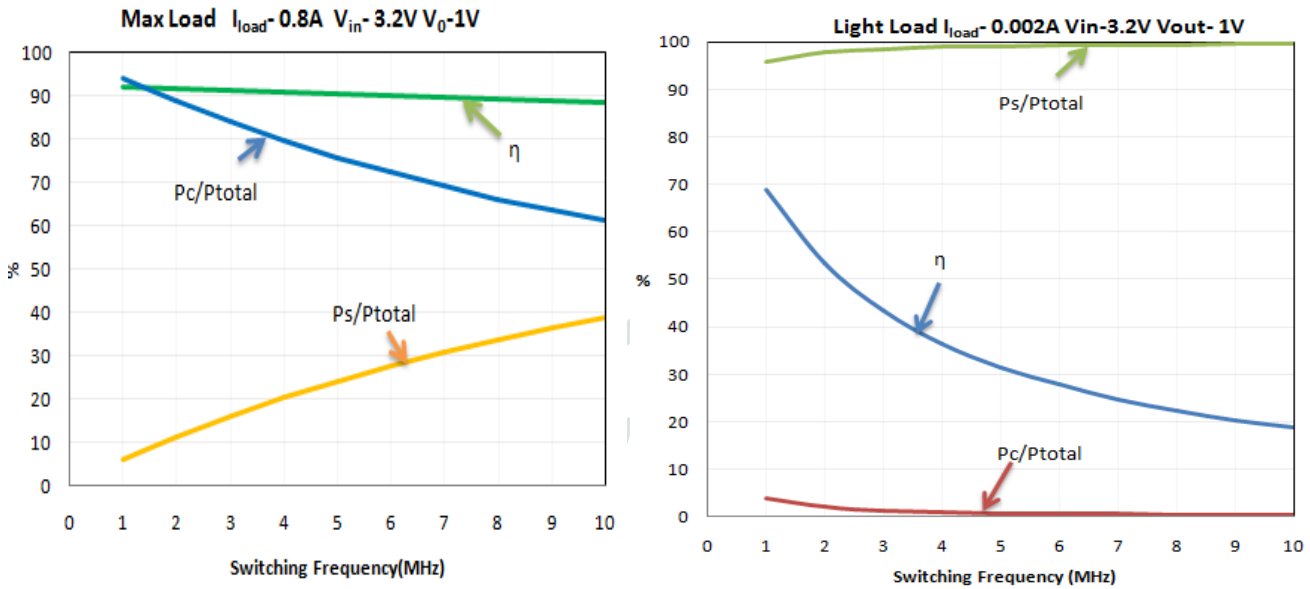


Fig.3 The variation of Efficiency, Conduction losses (P_c/Ptotal) and switching losses (P_s/Ptotal) (normalized to total losses) with respect to load current

The switching frequency is one of the most important parameters in analyzing the efficiency of the buck converter. A high switching frequency reduces the efficiency, especially at light load.Fig.4 (a) and (b) shows the variation of efficiency, conduction losses and switching losses with switching frequency. At heavy load as in fig.4(a) efficiency is high as conduction loss is more and is independent of switching frequency. At light load as in fig.4(b), switching loss becomes predominant and hence as switching frequency is increased the efficiency decreases drastically. Hence it is concluded that under heavy load, conduction loss is more and under light load, switching loss is more.



(a) (b)

Fig.4 The variation of Efficiency, Conduction losses (P_c/Ptotal) and switching losses (P_s/Ptotal) (normalized to total losses) with respect to switching frequency (A) heavy load (B) light load.

The analysis of efficiency with respect to the input voltage and Equivalent resistance R_{eq}(DCR and ESR) of the LC filter is also performed. It is observed that as the input voltage is increased, the efficiency of buck converter decreases slightly as in fig.5 (a). Fig 5(b) shows the variation of efficiency of a buck converter with R_{eq} of the LC filter. It is observed that as R_{eq} increases, there is a reduction in efficiency. Hence it is advantageous to choose an LC filter with low resistance value.

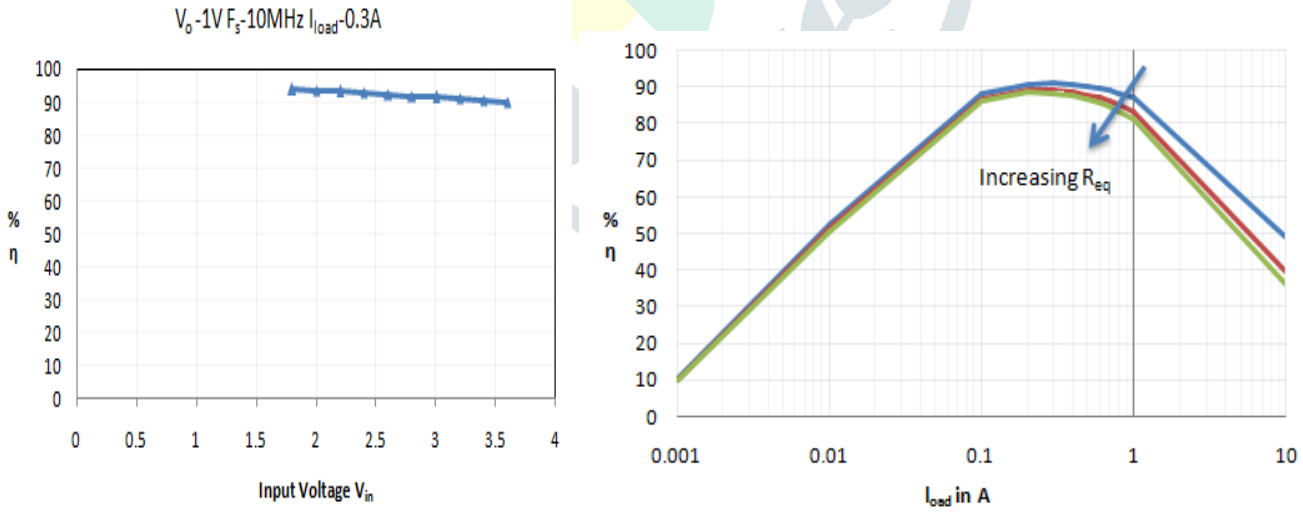


Fig.5 Efficiency variation with respect to (a) input voltage (b) Equivalent resistance of LC filter

V. CONCLUSIONS

The conversion efficiency of a low voltage, high switching frequency buck converter is obtained through Matlab-Simulink based simulation. The effects of load current, input voltage, switching frequency and the equivalent resistance of LC filter on efficiency are obtained and analyzed. Maximum efficiency of 91.01% is obtained at 0.3A of load current. The efficiency decreases drastically at low load conditions because of the effect of switching losses. It is concluded that PWM control is not effective under light load conditions as far as high efficiency is concerned. The variation of the efficiency of a buck converter with respect to

switching frequency is studied under light load and heavy load conditions. It is observed that efficiency mainly depends on conduction losses at heavy load and on switching losses at light load. A low value of equivalent resistance of LC filter is desired as efficiency is improved but the stability of closed loop operation of buck converter may become unstable.

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