Dynamic Voltage Scaling Using FPGA

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***Abstract*— Emerging multicore processors are progressively power guarded by design ambiguity due to process dissimilarities. With the help of dynamic voltage scaling energy consumption can be reduced in microprocessor can be achieved without affecting the peak performance. In handy electronic devices processors are having a average load which is having a time-varying performance requirement. A methodology to vary DVS is by varying supply voltage of the processor's so that it ingests the least amount of energy by operating at the lowest performance level required by the dynamic software processes. It is a key method in developing the hardware characteristics of processors to decrease energy dissipation by dropping the operating frequency and supply voltage. To meet energetically varying performance requirement the method varies the voltage of processor below software control. The DVS algorithm are shown to be proficient to make dramatic energy storing while providing the essential peak average power in general purpose systems.**

***Keywords*— FPGA, DVS, VCO, VHDL, Xilinx.**

I. INTRODUCTION

Customers interest for progressively versatile yet superior sight and sound and correspondence items forces stringent limitations on the power utilization of individual inward parts. Of these, multipliers perform a standout amongst the most much of the time experienced math tasks in digital signal processors (DSPs). For installed applications, it has turned out to be basic to plan more power-mindful multipliers. Given their genuinely complex structure and interconnections, multipliers can display countless ways, bringing about generous glitch age and engendering. This deceptive exchanging action can be relieved by adjusting inner ways through a blend of design and transistor-level advancement methods.

Notwithstanding evening out inner way delays, dynamic power decrease can likewise be accomplished by observing the viable dynamic scope of the info operands in order to debilitate unused segments of the multiplier as well as truncate the yield item at the cost of diminished accuracy. For instance, in counterfeit neural system applications, the weight exactness utilized amid the learning stage is roughly twice that of the recovery stage .interestingly, the majority of the present full-custom DSPs and application-specific integrated circuits (ASICs) are intended for a settled most extreme word-length to suit the most dire outcome imaginable. Hence, a 8-bit duplication figured on a 32-bit Booth multiplier would bring about pointless exchanging action and power misfortune.

In Most applications depend on 8– 16-b operands, the proposed multiplier is intended to perform single 16-b as well as performs single 8-b, or twin parallel 8-b duplication tasks. in some applications,16 and32 bit operands are send to littler duplication circuit with parallel task lessen control utilization and furthermore diminishes territory over head.

Because of the perplexing structure and interconnections, multipliers have extensive measure of unequal way which causes undesirable flag age and spread. This can be maintained a strategic distance from by appropriate inward adjusting through engineering and transistor level enhancement. by and large of multipliers, greatest word length is given. Henceforth little increases are done in vast multipliers, this causes undesirable exchanging movement and furthermore control utilization. So word length improvement is the best strategy in which 8-bit multiplier is reused for 16-bit and 32-bit augmentation. Here it is conceivable to fuse the pipelining for expanding the speed of the multiplier.

Concluding Introduction

Input oriented voltage scaling multiplier can overcome the drawback of conventional system where power and circuit area is wasted by disabling unused section of multiplier. By this there is reduction in path delays and unwanted switching.

II. NEED OF DVS

In many cases we there is lot of power consumption which is almost wastage of energy. So to avoid this wastage of energy we are having a provision in FPGA that we can make use of power (voltage) as per our requirement i.e. depending on data bits we can change the amount of power to be consumed.

III. OBJECTIVES

- To design a adaptive system according to workload.
- To reduce the circuit area and power consumption.

- To report the issues of fixed length ASIC's to avoid power loss and unnecessary switching activity.

IV. Problem Statement

To design and implement Input Oriented Dynamic Voltage Scaling Multiplier for effectively use of circuit area and to achieve lowest power consumption.

V. Literature Survey

X. Zhang, et.al.[1] ,Dynamic voltage/frequency scaling management unit configures the multiplier to operate at the proper precision and frequency. Adapting to the run-time workload of the targeted application, razor flip-flops together with a dithering voltage unit then configure the multiplier to achieve the lowest power consumption. an operands scheduler that re-arranges the input data, hence to determine the optimum voltage and frequency operating conditions for minimum power consumption.
K. Craig et.al.[2],This paper presents a 32 b, 90 nm data flow processor capable of executing arbitrary DSP algorithms using fine grained Dynamic Voltage Scaling (DVS) at the component level. For designs in the high performance design space, energy efficient operation reduce shot spots, lowers cooling costs, and avoids dark silicon issues. Many systems across this broad design space have applications that require high performance. However, due the varying nature of their applications, the workload requirements remain below this upper limit for the majority of their lifetime. Since different applications have varying workload requirements an energy efficient solution, such as dynamic voltage scaling (DVS), is needed. Dynamic voltage scaling is the conventional solution for adjusting energy consumption based on varying workload requirements.
S.R. Kuang et.al.[3],Power-efficient 16times, 16 configurable Booth multiplier (CBM) that supports single 16-b, single 8-b, or twin parallel 8-b multiplication operations is proposed. To efficiently reduce power consumption, a novel dynamic-range detector is developed to dynamically detect the effective dynamic ranges of two input operands. The detection result is used to not only pick the operand with smaller dynamic range for Booth encoding to increase the probability of partial products becoming zero but also deactivate the redundant switching activities in ineffective ranges as much as possible. Moreover, the output product of the proposed multiplier can be truncated to further decrease power consumption by sacrificing a bit of output precision.
K.-S. Chong et.al.[6],For embedded applications, it has become essential to design more power-aware multipliers Given their fairly complex structure and interconnections, multipliers can exhibit a large number of unbalanced paths, resulting in substantial glitch generation and propagation. This spurious switching activity can be mitigated by balancing internal paths through a combination of architectural and transistor-level optimization techniques.

VI. System Architecture

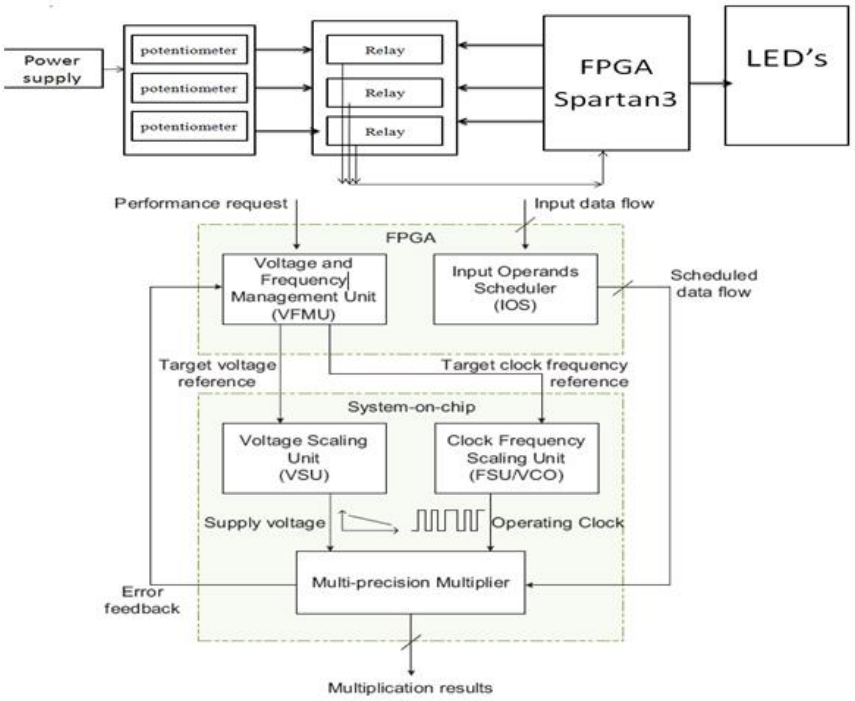


Fig1. System architecture diagram

IOS (Input operand scheduler)

The input operands scheduler which rearranges the input data and hence reduce the supply voltage transition, thus power consumption will be reduced. It consists of range detector, buffer (RAM), and a voltage and frequency analyzer. These help to rearrange the input and detect the precision and send to MP multiplier. Here proposed an IOS that will perform the following tasks:

i. reorder the input data stream so that same-precision operands are grouped together into a buffer and
ii. takes the minimum supply and frequency from the LUT

Frequency Scaling Unit

Frequency scaling unit of proposed MP multiplier is used for frequency tuning to meet the system throughput requirements. The frequency scaling unit is one which equipped with VCO is used to select frequency for each combination of multiplication. Depending on the control signal, it gives frequency that pre-calculated for 8 x 8bit, 16 x 16 bit and 32 x 32 bit for proper multiplication to reduce delay. Depending on the voltage VCO adjust the frequency. For each combination of multiplication, we can select the corresponding suitable frequency.

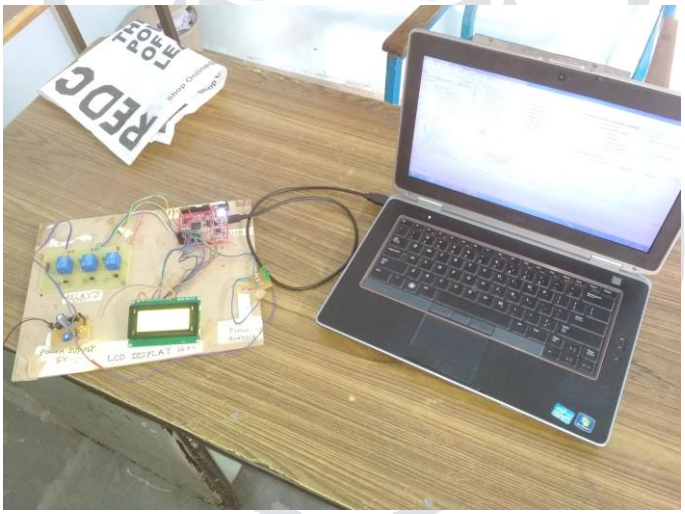
Voltage scaling Unit

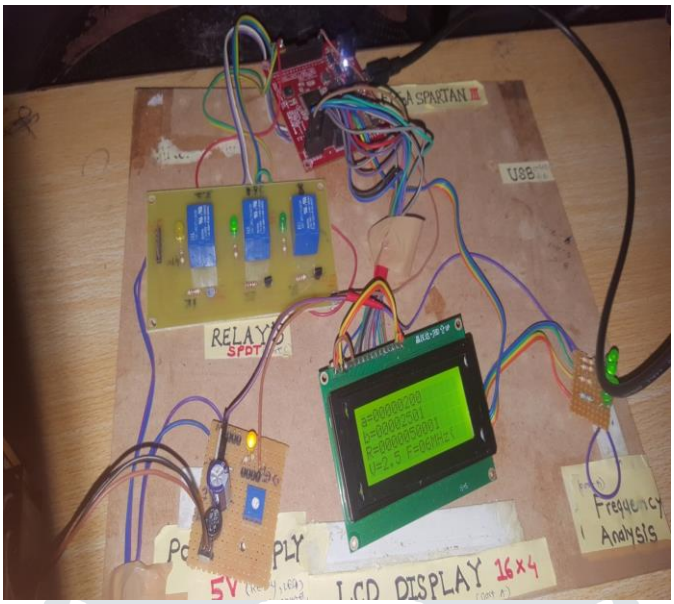
The voltage scaling unit (VSU) , its function is to dynamically generate the supply voltage so as to minimize power consumption.

Voltage /frequency management unit

The dynamic voltage/frequency management unit (VFMU) that receives the user requirements(e.g. through put).The VFMU sends control signals to the VSU and FSU to generate the required power supply voltage and clock frequency for the MP multiplier.

VII. RESULTS





VIII. CONCLUSIONS

It is understood that DVS is a noteworthy technique to reduce the power consumption of CMOS processor. In this thesis work many DVS algorithms are discussed that are very loosely-coupled with the underlying OS task management mechanisms and real-time scheduler, which can achieve significant energy savings, while simultaneously preserving timeliness guarantees made by real-time scheduling.

A DVS simulator was developed for the operation of hardware capable of voltage and frequency scaling with real-time scheduling. It is a unified simulation environment for evaluating dynamic voltage scaling algorithms. It supports DVS algorithms and it can be used to compare the energy efficiency of different DVS algorithms using the same task set specification under the same machine configuration. It can be used as well when evaluating a given DVS algorithm under various evaluation conditions.

The simulator was designed in such a way that any new DVS algorithm can be evaluated easily by adding new task execution module to it. It also supports adding new machine specifications to it.

A novel dynamic voltage scheduling algorithm is presented based on task deferring and an efficient slack estimation heuristic. The proposed UBFG DVS algorithm is compared with the Pillai RT- DVS algorithms for real-time periodic task sets, analyzing their energy efficiency, and discussing the performance differences quantitatively. The most significant parameters affecting energy conservation through RT-DVS mechanisms are shown in the simulation results. The proposed DVS algorithm can be close to the theoretical lower bound on energy since idle time utilization and slack passing are used efficiently. Simulated results indicate that the proposed algorithm reduces the energy consumption by 10-15% over the look ahead EDF algorithm, even including irreducible system energy overheads and using task sets with high values for worst-case utilizations.

The proposed DVS algorithm, which combines the goodness of static EDF and look ahead EDF algorithm, is implemented as a modular system in the Linux kernel and performance is analysed with the existing algorithms. The proposed algorithm achieves significant energy savings while preserving timeline guarantees compared to the previously proposed algorithms. Due to the modularity of the implementation, additional algorithms can be implemented and validated using the system.

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