Area Optimized Decimation Filter for Wideband ΣΔ Analog to Digital Converters

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Abstract: Presently Sigma-Delta (ΣΔ) analog to digital converters (ADCs) are the best suited for implementing architectures in nm CMOS technology. The applications of ΣΔ ADCs are increasing with time in different areas like wideband applications (SDR, LTE etc), audio and medical domains. The work in this paper focused on the designing of the decimation filter by modifying the already present architectures with different approaches and techniques. The proposed filter has been targeted for wideband applications. The algorithms and the filter structures chosen are hardware realizable in which area is the most important constraint. The suitable area optimization techniques are applied in each case to minimize area of the device targeted. The designed filter was targeted for being implemented in FPGA kit. The designed and implemented digital decimation filter consists of six stages (Comb-HBF-FIR) for high-resolution delta-sigma applications. Shift and add operations are used to implement multiplications of CSD-encoded coefficients. HDL synthesis has been preferred choice to implement the functions, including the storage of coefficients and computation, instead of RAM and ROM due to its time-to-market advantage. Experimental results show that use of multi-stage structure, with a proper selection of the decimation factor and filtering stage, ensures efficient performance of decimation filter. It has been shown that use of both non-recursive and recursive comb filters results in reduction in word-lengths as achieved by proposed architecture and thereby an area optimized decimation filter is obtained.

IndexTerms **- Analog to Digital Converter, Decimation filter, FIR filter, FPGA.**

I. INTRODUCTION

As we know that filter is an integral part of a DSP system. Due to the requirements on high data rates in many communication systems, the corresponding subsystems and circuits must have a high throughput as well low area. Since significant parts of such communication systems are customer products that are produced in large quantities and are sold at low prices, efficient, fast, and reliable design methods as well as low cost circuit implementations are required [1-5]. The possibility of integrating an entire system or parts of a system, on a single chip also requires subsystems with low power consumption. As such DSP functions are usually implemented on dedicated DSP processors or Application Specific Integrated Circuit (ASICs). While as DSP processors are flexible and less expensive but offer low speed for operation, ASICs have high speed but have cost and flexibility problem. So an alternative approach is provided in the form of Field Programmable Gate Arrays (FPGAs) as such they offer all above advantages and remove problems. Also as FPGA architectures offer system programmability the functionality of the device can be modified as per the need [6,7].

The three main modules of a DSP system include: Analog to Digital Converter, Processor and Digital to Analog System (DAC) [8]. Figure 1 shows the basic block diagram of a digital system. For carrying out various necessary filtering processes in a converter various levels of filtering is required. Multi-rate filters are one among class of filters which have different sampling rates at different stages of the filtering process [9]. These include interpolators, decimators, and narrow-band low-pass filters used for decimation, traditional low-pass filtering. Several papers have proposed methods to improve the performance of multi-rate decimation filters but at the expense of increased area [10]. Others have used only recursive filter algorithms at initial stages of decimation filter [11]. This work seeks to better the factors that like power consumption, speed of operation along with the minimum possible area utilization while implementing complete decimation filter. The use of HBF's and conventional FIR filters ensure that stopband and passband response did not get affected. In this paper we discuss the design and implementation of high speed area optimized decimation filter using non-recursive as well as recursive filter algorithms and the designs are compared. Previous research has used only recursive filter algorithms at initial stages of decimation filter [12]. This work seeks to better the factors that like power consumption speed of operation along with the minimum possible area utilization. In this paper, we discuss the design and implementation of low power high speed decimation filter using non-recursive as well as recursive filter algorithms. The main focus of this work is the design of Sigma-Delta (ΣΔ) modulator and decimation filter. The specifications of the design model of ΣΔ modulator are formulated in the Matlab employing the techniques to fulfill the required specifications. The Matlab model and the architecture are designed and modified simultaneously, to meet the correct functionality. The filter model created in Matlab is then

translated into HDL code required for implementation of the design. The filter is then implemented in using this code in the Xilinx platform. Finally, this HDL model is synthesized successfully in Xilinx.

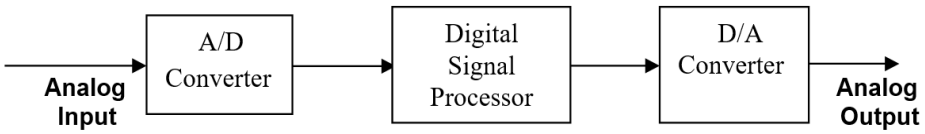

Fig. 1. Three main modules of a DSP system

II. PRELIMINARIES

A decimator has the function to decrease the frequency of the output from the oversampled modulator up to the Nyquist rate. Decimation is performed by an integer factor by removing the samples from a sequence until the required sampling rate is obtained. Another function of the decimation filter is to keep the passband aliasing within the prescribed limits. Usually the input signal to the decimator is band limited in order to avoid aliasing after decimation. This is done by a low pass anti-aliasing filter before the removing of samples. A decimation structure, including the anti-aliasing filter and the sample removal, is shown in Fig. 2.

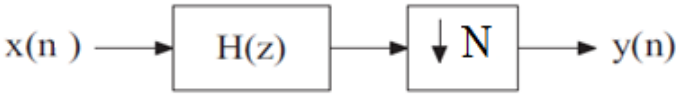

Fig. 2. Decimation filter

There are several architectural options available for implementing a decimation filter which are discussed in subsections.

2.1. Recursive Filter

One of the most important breakthroughs in the decimation filter design was achieved by E. Hogenaeur [11] who put forward decimation filter which is highly area efficient. The filter presented reduced complexity and storage issues that were usually present with conventional FIR filters. These filters require no multipliers, which are responsible for area increase in a silicon chip. Also they use limited storage of coefficients as usually only additions/subtractions are required. These filters are designated as cascaded-integrated-comb (CIC) filters after their architectural configuration as they consist of combs (differentiators) and integrators. CIC filters can be used to implement multistage decimation filters economically [14, 15]. The transfer function of a CIC filter is:

$$F(z) = F_I^k(z)F_C^k(z) = \left(\frac{1-z^{-DN}}{1-z^{-1}}\right)^k \qquad (1)$$

Where F_I is the transfer function of the integrator part of the filter, F_C is the transfer function of the comb part of the filter, k is the order of the filter, i.e. number of sections of the comb part or the integrator part as they are equal, N is the decimation factor and D is differential delay where D = 1 or 2. Such filter architecture is shown in Fig. 3.

Hogenauer's [11] CIC filter structure also called IIR-FIR structure comprise of an equal number of integrator (IIR) and comb (FIR) filter stages. Also due to the presence of the IIR section they are also called recursive filters. The frequency response CIC filter can be easily tuned by simply selecting the appropriate number of integrator and comb filter pairs. It provides a designer with a hardware efficient implementation due to its highly symmetric structure. The CIC filter is an area-efficient, symmetric FIR filter having phase linearity.

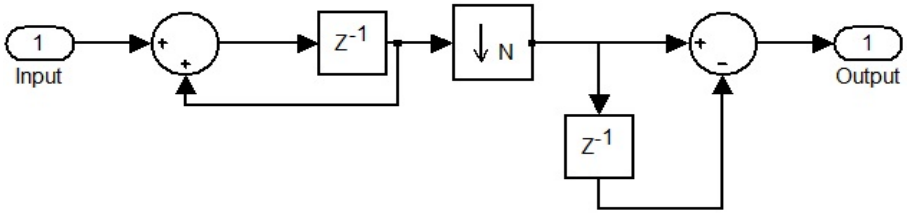

Fig. 3. Block diagram of IIR-FIR decimator

In its normal mode of operation, the CIC Decimation block allows the adder's numeric values to overflow and wrap around. The Fixed-Point infrastructure then causes overflow warnings to appear on the command line. This overflow is of no consequence. As the whole circuit is working at input sampling frequency which is very high, the power consumption of the circuit will be high. So a different decimation filter architecture is required in order to reduce power consumption. Other architectural options are the efficient non-recursive and polyphase structures; half band filters (HBFs) and several other modified structures.

2.2. Non-recursive filters

The stability issues arise in recursive filter because of presence of IIR filters in the structure. A modified transfer function can be obtained from original comb decimation filter one by simplifying Eq. (1) [16, 17] to:

$$H(z) = \prod_{i=0}^{M-1}(1 - z^{-2i})^k \quad (2)$$

Where decimation factor $N = 2^M$. An effective way to realize this decimation filter is by using a cascade of $\log_2 N$ FIR filters each providing a decimation factor of 2. This is called 'non-recursive structure' because recursive IIR is not present in the architecture and is wholly realized by only FIR filters unlike IIR-FIR structure which is recursive one due to presence of IIR filters. Thus stability related issues are absent in this structure.

2.3. Polyphase Decomposition

A limitation of the decimation structures discussed previously is that at the higher sample rate digital filtering is performed which results in effects like higher power consumption. The limitation can be avoided by using a technique called polyphase decomposition of the filters [17-19]. An *N*-component polyphase decomposition of a digital filter can be performed such that the transfer function of the filter can be rewritten as

$$H(z) = \sum_{i=0}^{N-1} z^{-i} E_i(z^M) \quad (3)$$

where $E_i(z)$ are the polyphase components of the filter $H(z)$. For the case when $M = 2$ we obtain

$$H(z) = E_o(z^2) + z^{-1} E_1(z^2) \quad (4)$$

Using polyphase decomposition technique all filtering can be done at the lower sampling rate which will improve the efficiency of an implementation significantly with respect to power consumption. In Figure 4 the area utilization of above three filters is presented and compared. It can be seen from the Figure that area utilization is less in case of recursive filters.

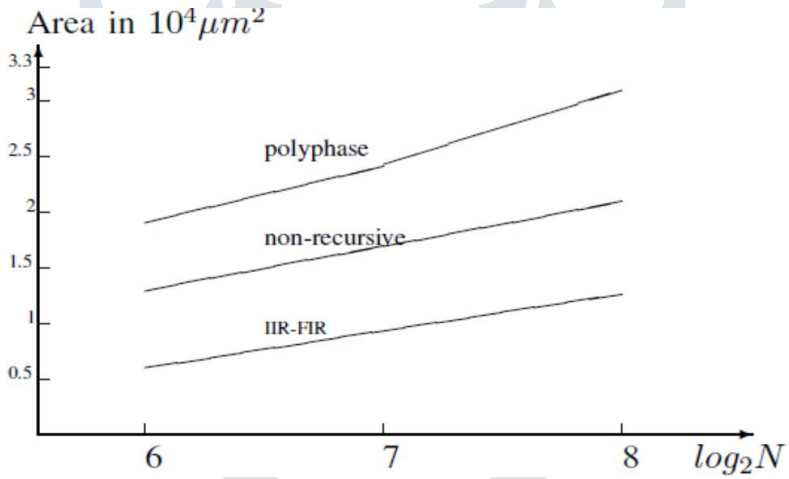

Fig. 4. Comparison of area utilization for various decimation filters

III. Proposed Decimation Filter Architecture

The proposed filter is a wideband decimation filter for 0.7-10 MHz to be used in wideband ΣΔ ADCs for application like LTE. The designed decimation filter is a high speed area optimized filter with the decimation ratio of 128 which can be programmed easily as per need by choosing different sampling rates for different input signal bandwidth. The decimation filter consists of two non-recursive comb filter, a recursive CIC filter, two half band filters and a FIR filter. Matlab Simulink with ΣΔ toolbox from SIMSIDES is being used for simulation with ΣΔM designed by SIMSIDES toolbox [de la Rosa 22]. The decimation filter is implemented using Xilinx design suite. The following specifications were taken into consideration while designing the decimator.

Table 1. Specifications of the Decimation Filter

Input/output	Parameters
Input no. of bits	3 bits
Output no. of bits	12 bits
Decimation factor	128
Output rate	0.8 MHz

The decimation filter comprises of decimation by- 2 non recursive input stages followed by decimation by 4 Sinc stage. The multistage architecture offers the advantage that most of the filter hardware can operate at a lower clock frequency, and thus hardware complexity gets reduced as compared to a single state decimator. In order to filter and suppress majority of the quantization noise initially three comb filters are used which also provide a clock rate decimation factor of 16. Also a higher decimation factor should be avoided in first stage as it results in drastic power consumption.

After the comb filters a second type of filter follows, called half band filter (HBF), is used which provides a sharp passband to stop band transition and decimation factor of 2. To achieve the droop compensation an introduced by the comb stages an FIR equalizer is used. Various techniques have been used to optimize the custom designed decimation filters. These techniques include multirate filtering, pipelining, retiming, resource sharing and employing power efficient number systems e.g. canonical signed digits (CSD). Similarly, during the synthesis of digital logic there is need of various optimizations. All sub-filters of the decimation filter are described in detail in the following sections.

3.1. Non-recursive comb filters (1st and 2nd stage)

The first two stages of the decimation filter designed are non-recursive filters with first one of 4th order and second of 3rd order respectively keeping in mind the compatibility issues and decimation factor requirements. The non-recursive filters are used due to the low power consumption and ability to increase the circuit speed. It is usually required that for a Kth-order modulator the order of the anti-alias filter should be one up in order for meeting the anti-aliasing requirements. As the noise shaping order of the ΣΔM is taken to be 3 in the design so the 4th order first stage non-recursive filter is used for better performance and anti-aliasing characteristics. This first stage operates at the rate of oversampling obtained from the oversampling modulator. Input stage of the design is very important due to the fact that it can result in large power dissipation as being working at the highest clock frequency that is why only decimation by 2 stages are used.

As described earlier that for the 3rd order modulator a 4th order filter is used for better performance.

$$H_1(z) = (1 + z^{-1})^4 = 1 + 4z^{-1} + 6z^{-2} + 4z^{-3} + z^{-4}$$
$$= 1 + 6z^{-2} + z^{-4} + z^{-1}(4 + 4z^{-2})$$
$$= E_0(z) + z^{-1}.E_1(z) \quad (9)$$

First stage is followed by 3rd order non-recursive filter derived from following expression:

$$H_2(z) = (1 + z^{-1})^3 = 1 + 3z^{-1} + 3z^{-2} + z^{-3}$$
$$= 1 + 3z^{-1} + z^{-1}(3 + z^{-2})$$
$$= E_0(z) + z^{-1}.E_1(z) \quad (10)$$

These filters are best choice for initial filtering in order to suppress most of the noise introduced by the quantization in the modulator. Both these filtering stages are implemented using polyphase decomposition technique.

3.2. CIC or Sinc Filter (3rd stage)

The Sinc filter forms the third stage of the decimation filter and is used for further suppression of the quantization noise. This filter is used after the non-recursive filters in order to meet the area constraints of the decimation filter because Sinc filter is an area efficient filter due to the absence of the multipliers and storages.

In the proposed decimation filter the 3rd order Sinc filter performing decimation of 4 is used. If the differential delay D=1 then its transfer function is

$$H_3(z) = \left(\frac{1-z^{-4}}{1-z^{-1}}\right)^3 \quad (12)$$

which can be solved as

$$H_3(z) = (1+z^{-1})^3 (1+z^{-2})^3 = (1+z^{-1}+z^{-2}+z^{-3})^3$$
$$= 1+3z^{-1}+6z^{-2}+10z^{-3}+12z^{-4}+12z^{-5}+10z^{-6}+6z^{-7}+3z^{-8}+z^{-9}$$
$$= 1 + 12z^{-4} + 3z^{-8} + z^{-1}(3+12z^{-4}+z^{-8}) + z^{-2}(6 + 10z^{-4}) + z^{-3}(10 + 6z^{-4}) \quad (13)$$

The polyphase decomposition technique used removes the critical path problem present in the CIC filter architecture and thus increases the speed of operation of the design. Adding to it, only first three registers having small internal word-length operate at higher sampling frequency than others proceeding after down sampler.

Hence we can get for polyphase implementation

$$E_0(z) = 1 + 12z^{-1} + 3z^{-2} \quad (14)$$

$$E_1(z) = 3 + 12z^{-1} + z^{-8} \quad (15)$$

$$E_2(z) = 6 + 10z^{-1} \quad (16)$$

$$E_3(z) = 10 + 6z^{-1} \quad (17)$$

3.3. Half Band Filters (HBFS)

The use of comb filters which are simple in structure have largely reduced the rate of sampling. However, the stopband attenuation achieved is not sufficient to meet the desired application demands. Therefore, a cascaded combination of two FIR HBFs is used to further increase the stopband attenuation [20]. In this paper, the HBF is implemented with a direct form transposed FIR polyphase decimator structure to reduce hardware complexity. The output sampling rate (13MHz) of the 3rd order CIC filter is same as the input sampling rate of the first HBF. Like 4th stage the 5th stage used in the design is the computationally efficient HBF. Their efficiency lies in the fact that they have approximately half of the coefficients equal to zero implying that large amount of computing power can be saved. Other characteristic of HBFs is that they have equivalent passband and stopband ripples and symmetrical passband and stopband frequencies around Fs/4 of sampling frequency. Due to these advantages they are used as the 4th and 5th stage of the decimation filter design. The 4th stage HBF used in the design is of 6th order. While the 5th stage HBF is of 14th order. The HBFs used in the design are obtained using the *"*filter-builder*"* option in the MATLAB. The "filter-builder" option helps us to both realize HBF block to be used in SIMULINK and HDL code generation to be used in XILINX.

3.4. FIR Low Pass Filter

The last stage of the decimation filter is a 36th order decimation filter [21]. It is a LPF which performs down-sampling by a factor of 2. Like HBFs FIR filter is designed and realized using the "Filter-builder" option in the MATLAB and its HDL code is generated using HDL Coder Toolbox therein. For the HDL code generation CSD format is used to encode the tap coefficients of the HBFs in order to technique in order to increase speed of operation and reduce the computation power.

IV. Results and Discussions

The aim of this paper is to design a decimation filter for wideband applications with special focus on the design and implementation of decimation filter part. Design and simulation is done for whole ADC and implementation is only done for decimation section of the converter. The decimation filter is designed in the Simulink environment of MATLAB. The block diagram of the decimation filter which is fed with the output of SD modulator is also shown in Figure 5.

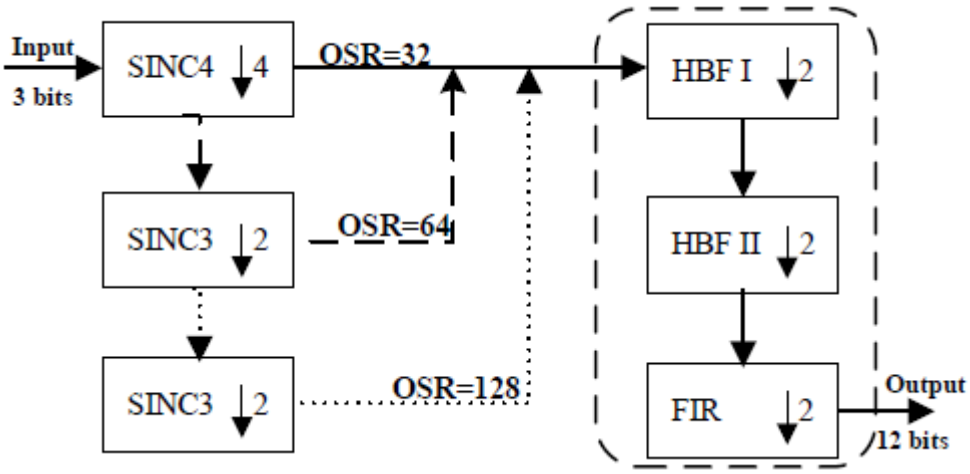

Figure 5. Block diagram of proposed decimation filter

The internal structure of all the filtering blocks like first and second non-recursive filters, third stage of CIC filter etc have been presented in detail in following sub sections. The simulation results of this ADC are shown in Figure 6(a) where first shows results in time domain and Figure 6(b) one shows the filtered signal in frequency domain. from the figure it is clear that the proposed design works properly.

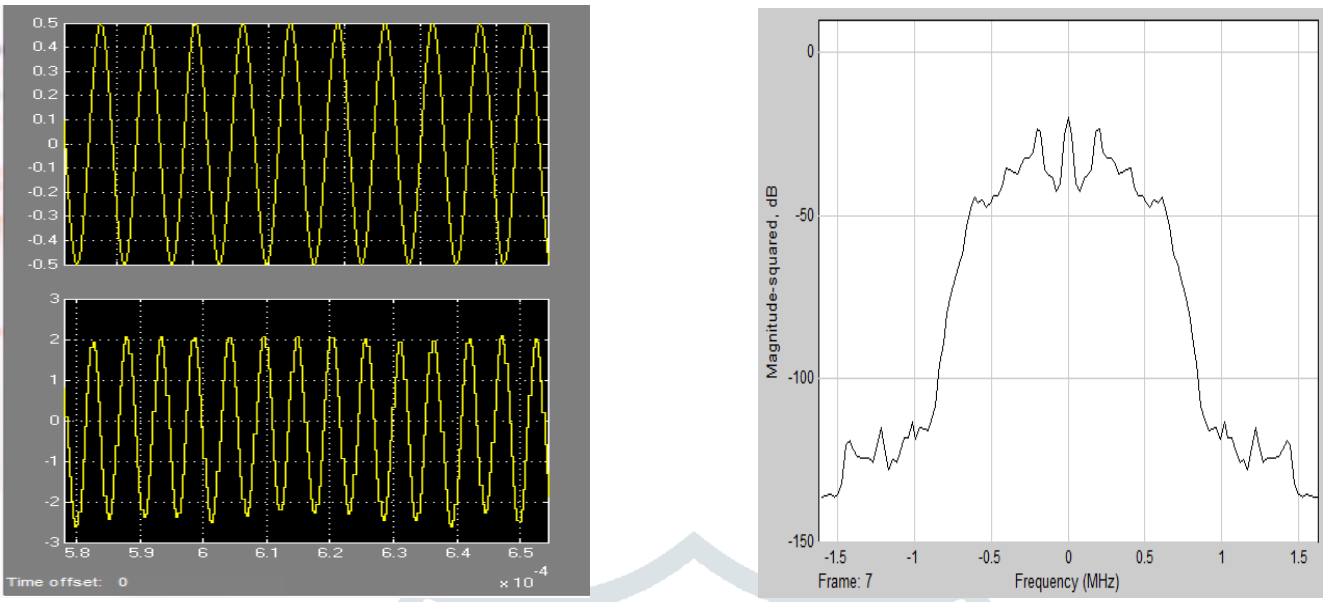

Figure 5.2: a) Input and output waveforms of ADC in time domain. b) Spectrum of filtered output signal.

4.1 Area utilization

The resources used by the decimation filter are shown in Figure 7 and Table 2. It has been seen from the comparison that utilization of resources is almost same for the decimation filter with and without using non-recursive filtering stages. Thus the idea of using CIC and non-recursive comb filters in designing decimation filter results in optimized area. Also one can increase/decrease the number and order of these stages as per the application requirement. Figure 7 shows the device utilization reports after synthesizing the previous and proposed architecture by Precision Synthesis Tool.

Resource	Used	Avail	Utilization
IOs	19	210	9.05%
Global Buffers	1	32	3.13%
LUTs	627	63400	0.99%
CLB Slices	157	15850	0.99%
Dffs or Latches	890	126800	0.70%
Block RAMs	0	135	0.00%
DSP48E1s	50	240	20.83%

(a)

Resource	Used	Avail	Utilization
IOs	18	210	8.57%
Global Buffers	1	32	3.13%
LUTs	1447	63400	2.28%
CLB Slices	362	15850	2.28%
Dffs or Latches	744	126800	0.59%
Block RAMs	0	135	0.00%
DSP48E1s	29	240	12.08%

(b)

Figure 7: Device utilization using Precision Synthesis Tool

The final device utilization report obtained after implementation process in the FPGA vendor tool is shown in Table 2. Here vendor tool used is Xilinx ISE and the results are obtained after place and route step of implementation process.

Table 2: Comparison of resource utilization in Xilinx

	Architecture [14]			Proposed Architecture		
Slice Logic Utilization	***Used***	***Available***	***Utilization***	***Used***	***Available***	***Utilization***
1) Number of Slice Registers	915	126,800	1%	744	126,800	1%
2) Number used as Flip Flops	867			712		
3) Number of Slice LUTs	989	63,400	1%	1,175	63,400	1%
4) Number of fully used LUT-FF pairs	634	1,253	50%	603	1,298	46%
5) Number of occupied Slices	388	15,850	2%	439	15,850	2%
6) Number of bonded IOBs	19	210	9%	18	210	8%
7) Number of DSP48E1s	33	240	13%	26	240	10%

V. CONCLUSION

The designed and implemented digital decimation filter consists of six stages (Comb-HBF-FIR) for high-resolution delta-sigma applications. This filter designed provides a time-to-market advantage. Multiplications of CSD-encoded coefficients are implemented by using shifters and adders. The complete functions, including the storage of coefficients and computation, are implemented by using HDL synthesis instead of RAM and ROM. Experimental results show that use of non-recursive comb filters results in reduction in word-lengths is achieved by proposed architecture. Also due to the use of both non-recursive and recursive combs area optimized decimation filter is obtained. Further study can be carried in following areas:

1. The proposed filter can be implemented and fabricated using ASIC and its parameters can be checked therein.
3. The designed filter can be analyzed for different frequencies to be used in different applications like digital audio, portable electronics, and other telecommunication applications.
4. The non-recursive and recursive comb stages of decimation filter can be increased or decreased as per the area and speed requirements of the targeted application

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