# DESIGN AND IMPLEMENTATION OF LOW AREA AND HIGH SPEED MULTIPLIERS USING 4-2 COMPRESSORS

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**Abstract**: In Digital Signal processing, data compression is a widely used technique which primarily focuses on multimedia and image processing applications by delivering the information/data in a compact size. Approximate computing can decrease the design complexity with an increase in performance and power efficiency for error resilient applications. This brief deals with a new design approach for approximation of multipliers .approximate computing is one of the interesting paradigm in arithmetic designs. The main objective of the approximate design is to reduce the area and delay. In this paper, we are desigining 8X8 dadda multiplier and 8x8 Wallace multipliers using 4:2 compressors for reducing number of partial products .The reduced number of partial products of this work offers the great advantage in the reduction of area and delay. Detailed simulation results are provided. The utilization of proposed approximate compressors in Dadda Multiplier and Wallace Multiplier is analyzed and is compared with the normal multiplier. The results show that there is a significant reduction in the delay and area when compared with the normal multiplier.

## I.INTRODUCTION

Multipliers are one of the most significant blocks in computer arithmetic and are generally used in different digital signal processors. There is growing demands for high speed multipliers in different applications of computing systems, such as computer graphics, scientific calculation, and image processing and so on. Speed of multiplier determines how fast the processors will run and designers are now more focused on high speed with low power consumption. There are generally three phases in tree multiplier architecture, which are partial product generation phase, partial product reduction phase and finally the addition phase to obtain the final result. Among these three phases, the second phase - partial product reduction phase consumes most of the power and is responsible for overall critical path delay. Therefore in order to optimize this stage, Compressors can be used for partial product accumulation. Compressors are used for addition operation and they contribute for reduced critical path delay, which is important in maintaining circuit's performance.

This can be accomplished with usage of 4-2 Compressors. These compressors are internally made of XOR-XNOR and multiplexer modules and their improved design will contribute a lot towards the overall system performance.

In present work, 4-2 Compressor made from high-speed and low-Area XOR-XNOR module and multiplexer was used. A new technique of partial-product reduction using 4-2 Compressors in multipliers have been proposed based on pre-determined sequence of matrix heights to give minimum number of partial-product reduction stages, with reduces delay and area of multiplier.

## II. OVERVIEW OF MULTIPLIER

Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore lowpower multiplier design has an important part in low-power VLSI system design. A system is generally determined by the performance of the multiplier because the multiplier is generally the slowest element and more area consuming in the system. Hence optimizing the speed and area of the multiplier is one of the major design issues. However, area and speed are usually conflicting constraints so that improvements in speed results in larger areas. Multiplication is a mathematical operation that include process of adding an integer to itself a specified number of times. A number (multiplicand) is added

itself a number of times as specified by another number (multiplier) to form a result (product). Multipliers play an important role in today's digital signal processing and various other applications. Multiplier design should offer high speed, low power consumption. Multiplication involves mainly 3 steps

1. Partial product generation
2. Partial product reduction
3. Final addition

**PROPOSED DADDA MULTIPLIER:**

The Dadda multiplier was designed by the scientist Luigi Dadda in 1965. Dadda Multiplier is similar to Wallace multiplier.

Dadda Multiplier was defined in three steps

- Multiply the each bit of one argument with the each and every bit of other argument and continues until all arguments are multiplied
- Reduce the number of partial products to two layers of full and half adders.
- Group the wires in two numbers, and add them with a conventional adder.

In this paper we have designed an 8*8 multiplier using dada multiplier design. Instead of using conventional full adders and half adder for designing the Multiplierwe introduce compressors which will reduces the complexity of the multiplier.

**Compressor:**

A compressor is a device which is mostly used in multipliers to reduce the operands while adding terms of partial product.Compressors of type 4-2 are generally used for performing addition. In multiplier design, 4-2 compressor ideal for constructing regularly structured Dadda tree and Wallace tree with less complexity. Usage of compressors will help to higher order can be designed by interconnecting lower order compressors, like a 4-2 Compressor can be, made from two full adders.

**4:2 Compressor Design**

Figure 1 shows the 4-2 compressor architecture. It has five inputs, X1, X2, X3, X4, Cin and three outputs, Cout, Carry, and Sum. The following equations give the outputs and table I provides the truth table.

$$Sum = X1 \oplus X2 \oplus X3 \oplus X4 \oplus Cin \quad (1)$$

$$Cout = (X1 \oplus X2)X3 + (\overline{X1 \oplus X2})X1 \quad (2)$$

$$Carry = (X1 \oplus X2 \oplus X3 \oplus X4)Cin + (\overline{X1 \oplus X2 \oplus X3 \oplus X4})X4 \quad (3)$$

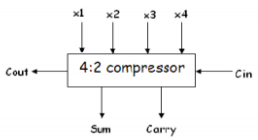


Fig 1 : Block Diagram of 4:2 compressor

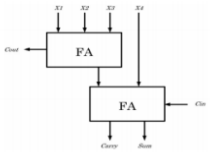


Fig 2 :Compressor using two full adders

## III. APPROXIMATE COMPRESSOR DESIGN

The exact compressor was reducing by proposing approximate compressors the two approximate compressors are shown below

**Design1:** In the design 1 approximation the we approximate the result by making Carry'=Cin With this approximation the carry output in an exact compressor has the same value of the input cin 24 out of 32 states. In particular, the simplification of sum to a value of 0 reduces the difference between the approximate and the exact outputs as well as the complexity of its design. Also, the presence of some errors in the sum signal will results in a reductions of the delay of producing the approximate sum and the overall delay of the design the change of the value of coutin some states, may reduce the error distance provided by approximate carry and sum and also more simplification in the proposed design.

$$Sum' = \overline{Cin}(\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$

The change of the value of coutin some states may reduce the error distance provided by approximate carry and sum and also more simplification in the proposed design.

$$Cout' = \overline{(\overline{x1x2} + \overline{x3x4})}$$

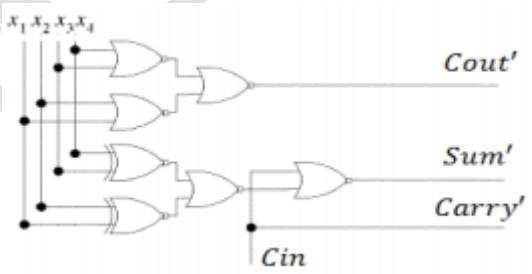


Fig3: Gate level implementation of Design 1

**Design2:** A desgin2 was designed for more approximation than the design1 further increase performance by reducing the error rate. In the proposed design we approximate the carry' and cin since they are having the same weight. In this design we take Cin as o so that we can remove the carry'.

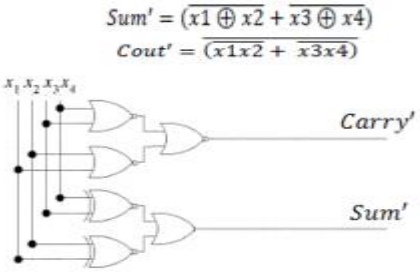


Fig4: Gate level implementation of Design

**Dadda Multiplier using Design1:**

•A 8×8 unsigned Dadda tree multiplier is considered to assess the impact of using the proposed compressors in approximate multipliers.

• The proposed multiplier uses in the first part AND gates to generate all partial products

• The reduction part uses half-adders, full-adders and 4-2 compressors; each partial product bit is represented by a dot. In the first stage, 2 half-adders, 2 full-adders and 8 compressors are utilized to reduce the partial products into atmost four rows.

• In the second or final stage, 1 half-adder, 1 full-adder and 10 compressors are used to compute the two final rows of partial products. • Therefore, two stages of reduction and 3 half-adders, 3 full-adders and 18 compressors are needed in the reduction circuitry of an 8×8Dadda multiplier

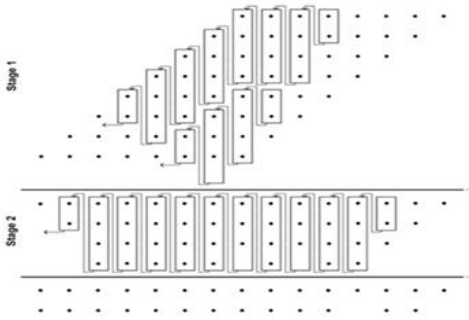


Figure 5: 8*8 Dadda multiplier 1 using 4:2 compressors

**Dadda Multiplier using Design2:**

• In the first case (Multiplier 1), Design 1 is used for all 4- 2 compressors in Figure.

• In the second case (Multiplier 2), Design 2 is used for the 4-2 compressors. Since Design 2 does not have cin and cout, the reduction circuitry of this multiplier requires a lower number of compressors (Figure 9(b)). Multiplier 2 uses 6 half-adders, 1 full-adder and 17 compressors.

• In the third case (Multiplier 3), Design 1 is used for the compressors in then-1 least significant columns. The other n most significant columns in the reduction circuitry use exact 4-2 compressors

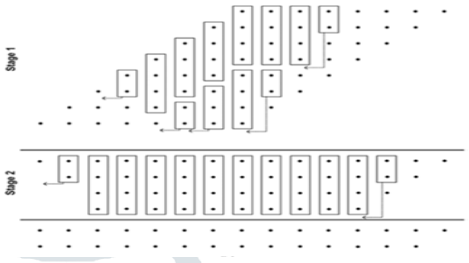


Figure 6: 8*8 Dadda multiplier 2 using 4:2 Compressors

**PROPOSED WALLACE MULTIPLIER:**

8x8 Wallace Multiplier using 4:2 Compressors (rounded rectangles) is shown in figure 4. On using compressors the number of reduction stages gets reduced to 3, instead of 5 stages when only half and full adders are used. By using 4:2 compressors delay also reduced.The Multiplier uses 17 no. of 4-2 compressor,18 full adders and 9 half adders. This Wallace tree has lesser delay compared to the one which does not use 4-2 compressors.

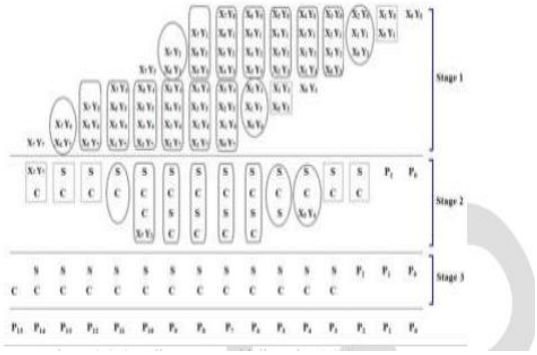

Figure 7: Wallace tree multiplier using 4:2 compressors

**IV.SIMULATION RESULTS**

**A. Dadda Multiplier1 using 4:2 Compressor**

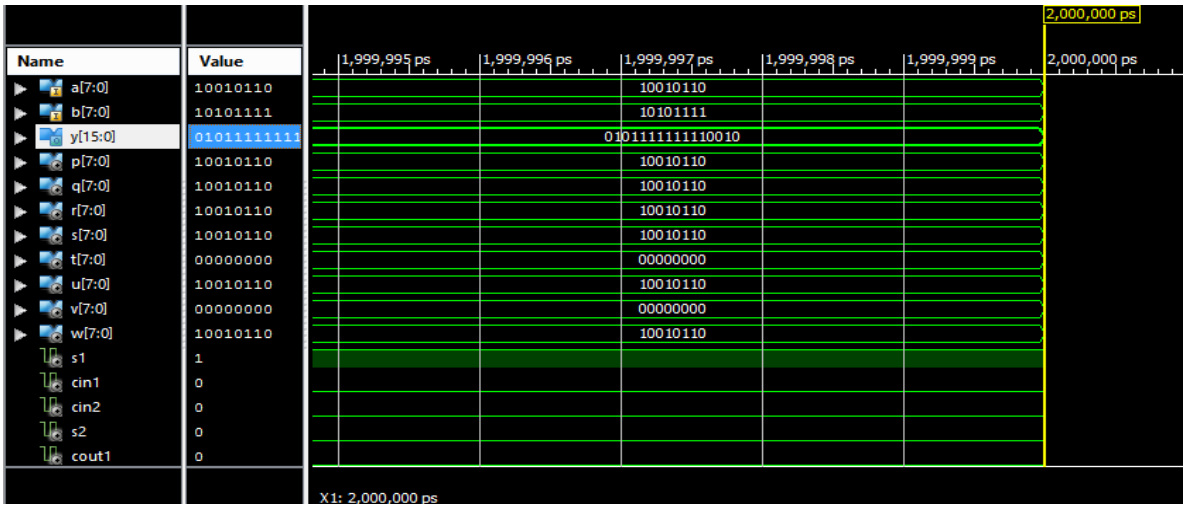


Figure 8: 8x8 Dadda multiplier1 using 4:2 Compressor

**B. Dadda Multiplier2 using 4:2 Compressor**

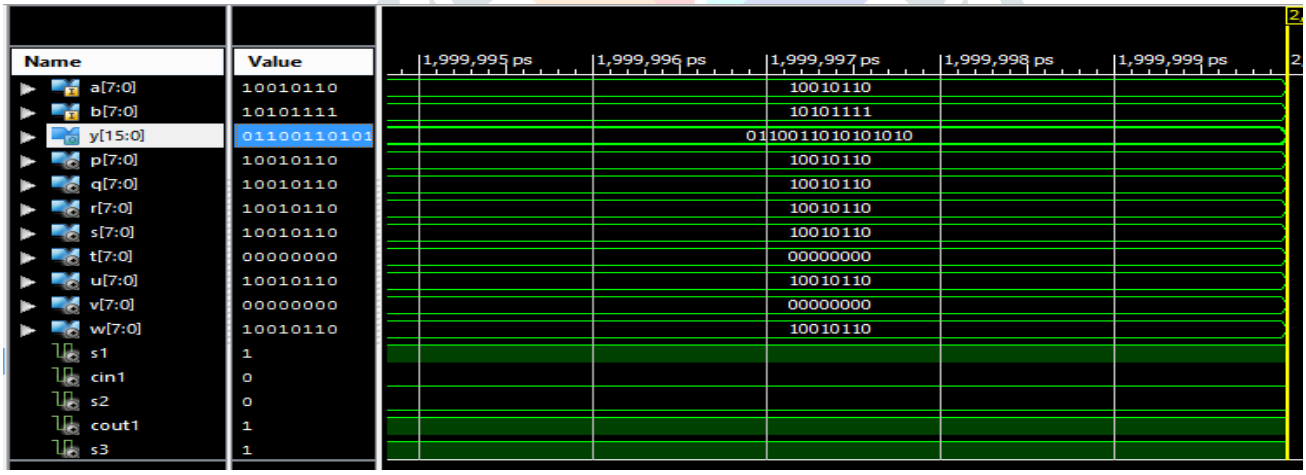


Figure 9: 8x8 Dadda multiplier2 using 4:2 Compressor

**C. WallaceMultiplier using 4:2Compressor:**

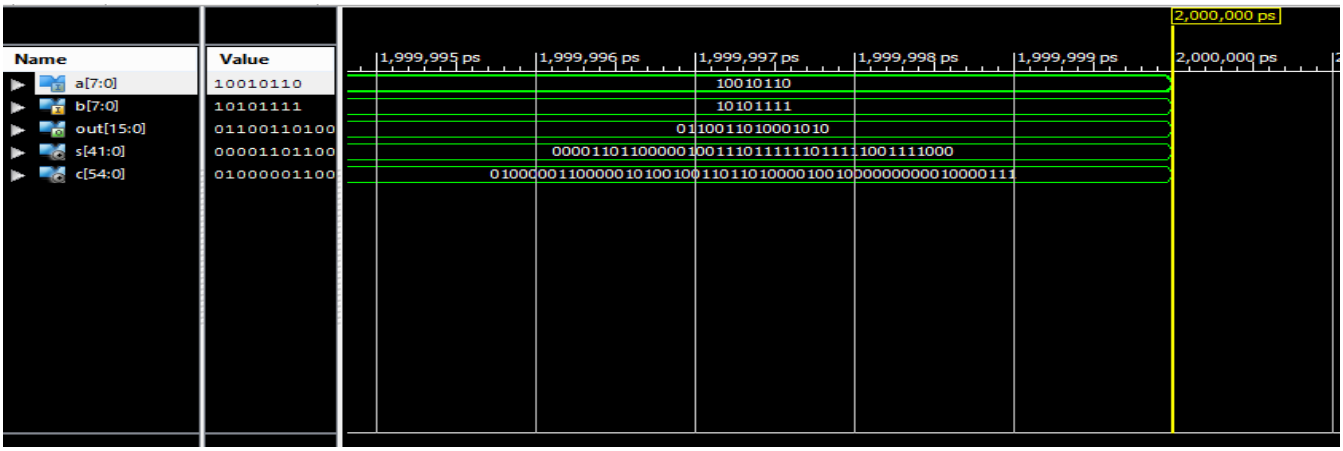


Figure 10: 8x8 Wallace Multiplier using 4:2Compressor

**D.Performance Comparision of Multipliers:**

Comparison Table of Normal Multiplier without 4:2 Compressor and dadda multiplier with 4:2 Compressor and wallace multiplier with 4:2 Compressor.

| Parameter | Normal Multiplier | Dadda multplier1 | Dadda multplier1 | Wallace Multiplier |
|---|---|---|---|---|
| No. Of LUT'S | 154 | 131 | 125 | 114 |
| Delay(ns) | 22.13 | 19.26 | 19.60 | 9.92 |

## VI. CONCLUSION

A 8x8 Dadda Multiplier and Wallace Multiplier has been presented for high speed performance, which uses 4-2 compressors based on an XORXNOR gate of high speed and low area multiplexer made of transmission gates.The normal multiplier shows less speed performance when compared to the proposed Dadda multiplier and Wallace Multiplier implemented with 4-2 Compressors. The performance Comparisions and results show that the 4:2 Compressor gives significantly less delay and area than the existing normal multiplier .This proposed reduction format can also be applied to higher order NxN multipliers for high speed results.

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