Power Optimization of ALU Using Advanced GDI Technique

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Abstract- This article provided a design of 4-Bit Arithmetic Logic Unit (ALU) using Full-Swing GDI Technique, which considered an effective method for low power digital design while reducing the area of the circuit compared using various CMOS techniques are discussed. The proposed ALU design consists of two 2x1 Multiplexer, two 4x1 Multiplexer and low power Full Adder cell to realize the arithmetic and logic operations. Later, using this low power GDI technique a 4-bit ALU is compared with a proposed ALU. The proposed ALU is obtained by solving the truth table, using KMap (Karnaugh Map). The simulation carried out using HSPICE using 35nm TSMC process. The simulation shows that the proposed 4-bit ALU design dissipates low power, while improving delay and area among all the design taken for comparison.

Keywords- Arithmetic Logic Unit (ALU); Gate Diffusion Input (GDI); Full-Swing GDI.

I. INTRODUCTION

Now-a-days, as the technology is going on increasing in terms of IC design, a greater number of transistors are getting packed into an IC so that the size and the area of the physical design of an IC increases. So, at present, scaling is also more important for designing any device. The main requirement in the designing field of digital circuit is minimizing the power consumption. In any digital system, one of the main parts is Processor. But to build this processor, Arithmetic Logic Unit (ALU)[1] is important component. Similarly, if we consider any system, CPU works as a brain. But for CPU, ALU works as a brain. So, ALU treated as a brain of computers brain. ALU is a combinational digital electronic circuit which perform both arithmetic and logical operations on integer binary numbers. An ALU is a fundamental building block of many types of computing circuits including graphics processing units (GPUs), FPU, CPU. A single CPU, GPU, FPU may contain multiple ALUs. Modern CPUs contain very powerful and complex ALUs. Most of the operations of a CPU are performed by one or more ALUs, which load data from input registers. A typical ALU consists of three types of functional parts: storage registers, operations logic, sequencing logic. ALU contributes the highest power density locations on the processor. As it is active all the time which results in thermal hotspots and sharp temperature gradients within the execution core. For designing an ALU the required components are: MUX, Full adder, logic gates etc...

A multiplexer is known as the data selector in electronics. It is a device that selects between several analog or digital input signals and forwards those signals to a single output line. A MUX functions as a multiple-input, single-output switch. A mux is used to increase the efficiency of the communication system by allowing the transmission of data, such as audio and video data from different channels through cables and single lines. A MUX of 2n inputs [2] has select lines, which are used to select which input line to send to the outputs. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. They can also be used to implement Boolean functions of multiple variables.

Full adder is the adder which adds three inputs and produces two outputs [1]. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. A Full adder reduces the circuit complexibility. It can be used to construct a ripple carry counter to add an n-bit number. Thus, it is used in ALU. It is used in Processor chip like Snapdragon, exynous or Intel Pentium for CPU

part. To generate memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU makes use of this adder. For graphics related applications where, there is a much need of complex computations, the GPU uses optimized ALU which is made up of full adders.

The performance of digital circuits can be optimized by proper selection of logic styles. Based on the transistor count, power consumption, full adder design, space required, delay, reliability, high speed some techniques are discussed. They are CMOS and GDI logic.

II. EXISTING METHODS

CMOS:

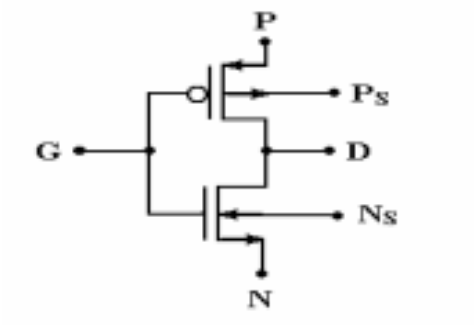
One of the most popular MOSFET technologies available today is the "Complementary Metal Oxide Semiconductor" or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application specific integrated circuits (ASICs). CMOS technologies are firmly established in modern electronics. CMOS provides the important characteristics needed for high-density logic designs. Today's computer memories, CPUs and cell phones make use of this technology due to several key advantages. The "complimentary" part of CMOS refers to the two different types of semiconductors have a greater concentration of electrons than holes, or places where an electron could exist. P-type semiconductors have a greater of holes than electrons. These two semiconductors work together and may form logic gates based on how the circuit is designed.

This technology makes use of both P channel and N channel semiconductor devices. Each MOSFET includes two terminals Source and Drain and a Gate, which is insulated from the body of the transistor. When enough voltage is applied between the gate and the body, electrons can flow between the source and the drain terminals. CMOS transistors are known for their efficient use of electric power. The result is a low power design that gives off minimal heat. For this reason, CMOS transistors have replaced other previous designs (such as CCDs in camera sensors) and used in most modern processors.

GDI LOGIC:

We use a lot of portable electronic devices. These devices are basically low power, high speed, VLSI circuits. One of the circuits is ALU. In CMOS design it takes more delay and more power consumption. So, we choose GDI [5] over CMOS. GDI technique depends on the implementation of an elementary cell.

GDI cell is designed by using one PMOS and one NMOS transistors. It is same as CMOS inverter. But there are two differences shown in below fig(a).



Fig(a) Basic GDI Cell [1]

(i) It is having 3 input pins i.e., G, P, N and one output pin.

a) Input pin G is Common gate of PMOS and NMOS.
b) Input pin P is input to Source/drain of PMOS.
c) Input pin N is input to Source/drain of NMOS.

(ii) It requires bulk of NMOS and PMOS transistors are connected to P(or)N [1].

Sr. No.	Input			Output	Function
	P	G	N		
1	B	A	0	$A.\overline{B}$	F1
2	1	A	B	$A \overline{+} B$	F2
3	B	A	1	A + B	OR
4	0	A	B	A.B	AND
5	B	A	C	$A.\overline{B} + A.C$	MUX
6	1	A	0	$A\ \overline{\ }$	NOT

Functions of basic GDI cell:

In CMOS all of the functional operations are not possible, but they can strongly actualize in silicon on inverter. Boolean functions are versatile in CMOS as well as PTL. But these functions are very simple in GDI technique. The GDI technique is different from other techniques, and it has some

valuable characteristics that allow some upgradation in designing multiplicity level, power dissipation, transistor count. GDI cell needs a code functional determination of the elementary cell in several cases and configurations. In these GDI technique, firstly we have to design the basic digital gates and then these gates are further used in the implementation of different types of adders and multipliers. Adder is selected based on the performance. This selected adder is further used in the design of multipliers. Firstly, one-bit full adder is designed using GDI technique. This adder is used to analyse the other complex adders for their better performance. 4-bit full adder is designed by using GDI technique. It requires a smaller number of transistors compared to CMOS technique. ALU is designed using GDI technique. By using ALU in GDI technique it reduces the integral blocks and power consumption compared to CMOS technique. ALU design using GDI technique uses a smaller number of transistors, so, area is optimized, speed is increased, operating time is reduced and it consumes less power. The main drawback of GDI gate is that it suffers due to threshold voltage drop. This reduce the current driven and affects the performance of the gate.

Advantages of GDI:

- Less power consumption
- Less Area
- Required a smaller number of transistors
- Efficient for placement and routing
- Shorter interconnects
- High speed operations
- Less crosstalk

Drawbacks of GDI:

- Output voltage swing degradation
- Power consumption
- Fabrication complexity

III. PROPOSED METHOD

The proposed 4-bit ALU was designed using a low power adder cell realized by the Advanced GDI technique and compared to existing system power dissipation and transistor count is reduced.

Arithmetic Logic Unit(ALU):

In this paper the Full-Swing GDI technique is used to realize the circuits required to design the ALU as follows:

2x1 Multiplexer:

A multiplexer is a digital switch chooses the output from several inputs based on a select signal, shown in Fig:2 a 2x1 multiplexer consists of 6 transistors.

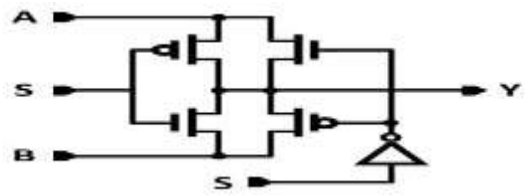


Fig (a): Advanced GDI 2x1 Multiplexer

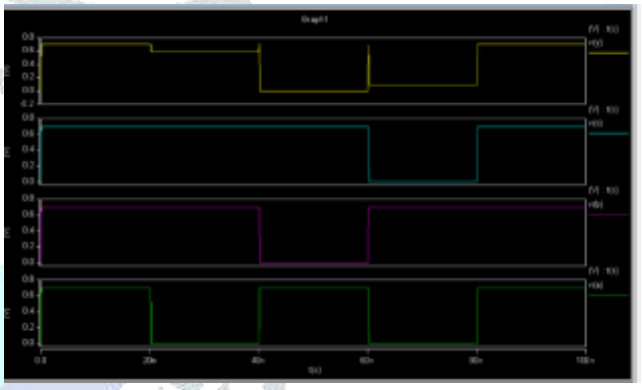


Fig (b): Waveform for 2x1 mux using Advanced GDI technique

4x1 Multiplexer:

Using the previously discussed 2x1 multiplexer a 4x1 multiplexer realized as shown in below fig consists only of 16 transistors.

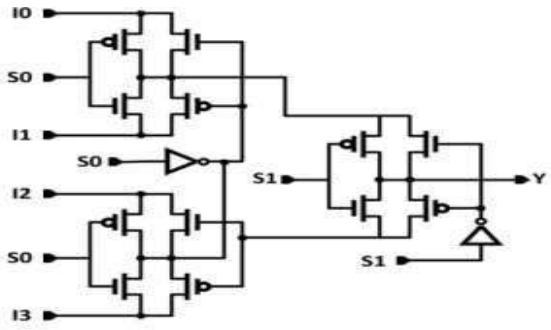


Fig (c): Advanced GDI 4x1 Multiplexer

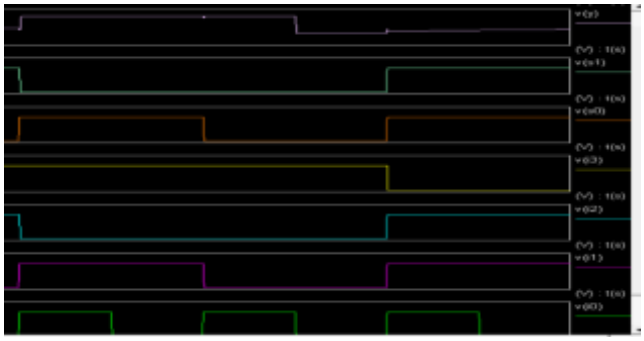


Fig (d): Waveform for 4x1 mux using Advanced GDI technique

Full Adder:

A full adder is a combinational circuit that performs the arithmetic sum of three input bits. It consists of three inputs and two outputs. The adder cell used in this design realized using full-swing AND, OR, and XOR gates. This design was chosen among 3 designs to maintain low power operation, it has the lowest delay among the three designs, and with some modifications it performs the logic operations as well, these modifications will save large area of the ALU design.

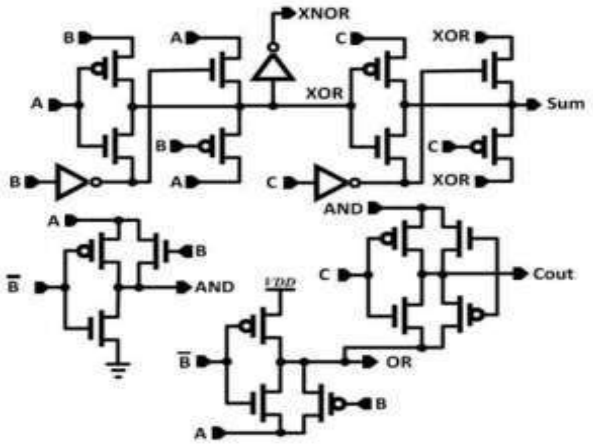


Fig (e): Advanced GDI Full Adder cell

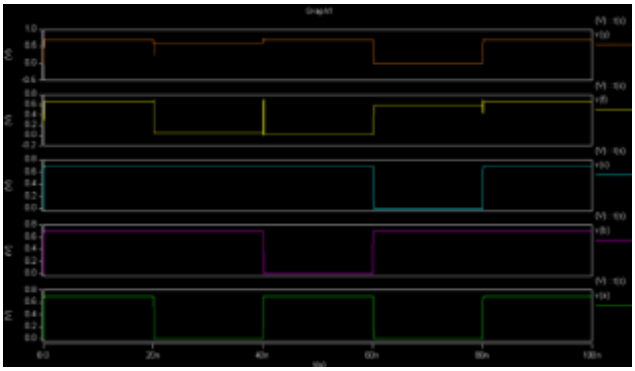


Fig (f): Waveform for full adder cell using Advanced GDI technique

Design of Arithmetic Logic Unit:

An ALU is a key component in the Central Processing Unit (CPU) of any computer; even the simplest microprocessors contain one. It performs arithmetic operations such as addition, subtraction, increment, decrement and logic operations such as AND, OR, XOR and XNOR [6]. The proposed design of the 4-Bit ALU consists of 4 stages, each stage is a 1-Bit ALU realized using the previously discussed circuits as follows: Each 1-Bit ALU stage consists of one 2x1 multiplexers, one 4x1 multiplexers and one full adder cell, this design requires 46 transistors as depicted in Fig. (a). Any desired operation can be performed based on the selection line S0, S1, S2 code, Table II summarizes the truth table of the proposed ALU.

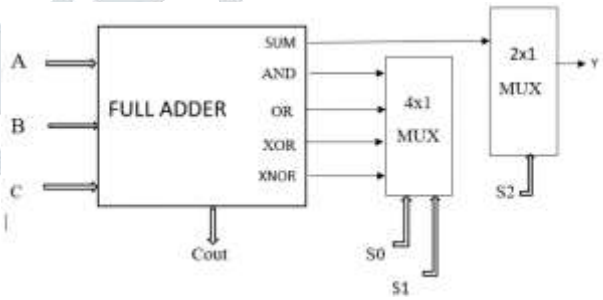


Fig (a): Schematic of 1-Bit ALU using Advanced GDI

S0	S1	S2	Output
0	0	0	AND
0	1	0	XNOR
1	0	0	XOR
1	1	0	OR
0/1	0/1	1	SUM

Fig (b): Truth table for 1-bit ALU using Advanced GDI

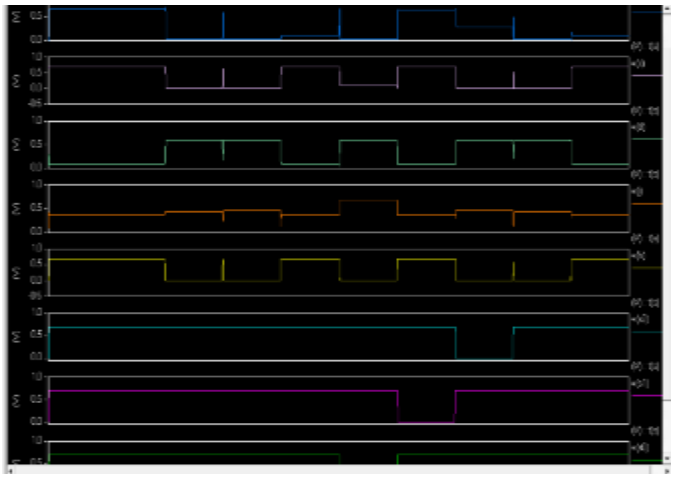


Fig (b): Waveform for 1-bit ALU using Advanced GDI technique

***Design of 4-bit ALU using Advanced GDI technique*:**

To realize the 4-Bit ALU four stages were used as shown in Fig. (a). Here four ALU blocks are connected to S0, S1, and S2. Here, carry output of ALU0, ALU1 and ALU2 are given to the input of other blocks. Final carry output is taken at ALU3 block. From each block we are getting an output such as Y0, Y1, Y2 and Y3[9]. The waveform for a proposed 4-bit ALU is shown in below figure (b)

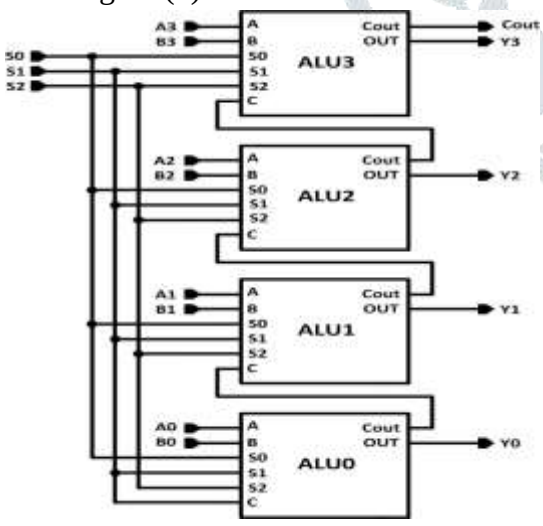


Fig (a): Proposed 4-bit ALU using Advanced GDI

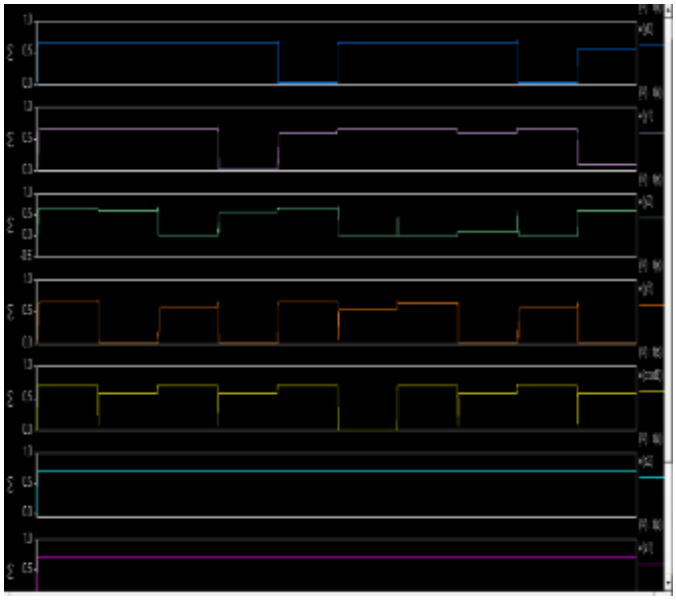


Fig (b): Waveform for 4-bit ALU using Advanced GDI

IV. SIMULATION RESULT

The power and delay for proposed 4-bit ALU using Advanced GDI technique are shown in Table. By using HSPICE tool we are going to get power and Delay.

Circuit design	Power	Delay
Proposed 4-bit ALU	$1.891e^{-3}$	$1.018e^{-8}$

V. CONCLUSION

The proposed 4-bit ALU was designed in TSMC 32nm CMOS process using the Advanced GDI technique and simulated using HSPICE software tool. The simulation result shows benefit in terms of Delay and Power Consumption of the new ALU circuit maintaining Full Swing operation. The architecture proposed is made up of 184 transistors and operates under 0.7v

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