High Breakdown Voltage Trench RF laterally-diffused MOSFET on 4H-SiC

Mohit Payal[1], Parag Jain[2], Vibhor Sharma[3], Deepak Arya[2], Amit Kumar Tanwar[2]

[1] Shivalik College of Engineering, Dehradun, Uttarakhand, India, [2] Roorkee Institute of Technology, Roorkee, Uttarakhand, India, [3] Swami Rama Himalayan University, Dehradun, Uttarakhand, India.

*Corresponding author: mohitpayaal1986@gmail.com

***Abstract*-- On 4H-SiC, a power trench-gate LDMOSFET (TG-LDMOS) structure is proposed with improved electrical properties. The gate is set vertically in a trench in the new device. In the proposed TG-LDMOS structure, simultaneous application of positive voltage creates vertical channels that conduct output current in parallel for positive drain voltages. This improves the output current (I_D) and transconductance (g_m) with raises the cut-off frequency and (f_T). By placing trenches in the drift layer to boost blocking voltage (V_{br}), the reduced-surface-field effect is enhanced. The novel device provides a V_{br} of 320 V with a f_T of 12.2 GHz with drift layer doping of $4x10^{16}$ cm^3. When compared to the traditional equivalent with the same doping and cell length, the two-dimensional simulations demonstrate that the TG-LDMOS can deliver 1.7 times higher I_D, 1.3 times rise in g_m, 1.9 times higher f_T, 1.8 times improvement in V_{br} and 3 times increase in BFOM.**

***Index Terms*--4H-SiC, RF LDMOS, breakdown voltage, cut-off frequency, BFOM, RESURF, and Trench-gate.**

1. INTRODUCTION

Silicon carbide (SiC) is a potential semiconductor for high-voltage, high-power, high-frequency, and high-temperature power devices due to its wide band-gap, strong breakdown field, high saturation velocity, and high thermal conductivity, [1], [2]. At high power densities, SiC's broad breakdown field and thermal conductivity result in reduced power dissipation and cooling needs [3, 4]. In comparison to other poly-types of SiC, 4H-SiC has the highest bulk mobility, the smallest anisotropy, and the highest level of material quality maturity. For a number of power electronics applications, the lateral diffused power metal-oxide field-effect transistors (LDMOSFETs) made on 4H-SiC are a desirable option [5]. Higher drain current, low threshold voltage, high transconductance, high breakdown voltage, and rapid switching speed are key characteristics of a power LDMOSFET for these circuits. These factors are interrelated in a conventional LDMOSFET (Con. LDMOS), therefore a trade-off must be made between them. Reports on 4H-SiC LDMOSFETs [6] that employ RESURF methods to enhance the trade-off between breakdown voltage and ON-resistance to raise the figure-of-merit (FOM) [7], [8]. In lateral power devices, the RESURF effect lowers the electric field in the drift area, increasing the breakdown voltage. On the other hand, trench-gate structure concepts have successfully shown to boost output current and breakdown voltage while decreasing ON-resistance and threshold voltage because of enhanced doping concentration [9]. In order to incorporate two trenches in the drift region, the Con. LDMOS structure has been modified in this study.

The proposed device includes a vertically positioned gate-electrode in a trench, in contrast to the planar gate-electrode of Con. LDMOS, and an additional trench, filled with oxide, is inserted in the drift area to increase the RESURF effect. Trench-gate LDMOSFET (TG-LDMOS), a novel structure on 4H-SiC, is made up of a gate that creates a channel in the p-body region for parallel conduction. The performance of the TG-LDMOS is assessed using two-dimensional simulations in the device simulator SILVACO [10] and contrasted with that of the Con. LDMOS. The suggested device structure outperforms the traditional design by a significant margin in terms of the performance characteristics.

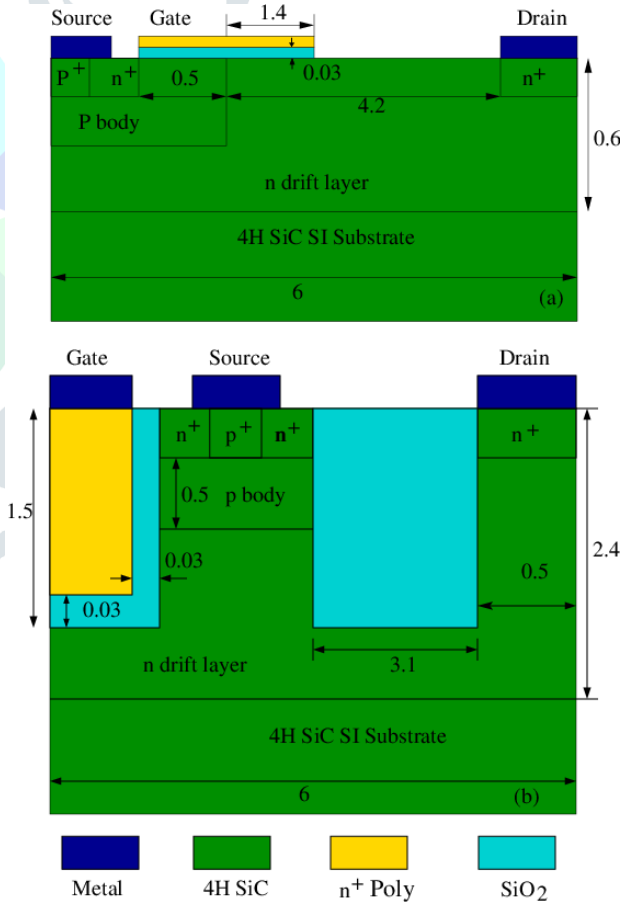

***Fig. 1.** Unit cell in schematic form for the (a) Con. LDMOS and (b) TG-LDMOS. All measurements are in μm.*

2. Device Structure and Mechanism

In Fig. 1, the unit cell of the Con. LDMOS and proposed TG-LDMOS structures built on 4H-SiC with a semi-insulating substrate can be seen from a cross-sectional perspective. The Con. LDMOS structure uses a field-plate over the drift area, as illustrated in Fig. 1 (a), to minimize the electric field on the SiC surface and increase the device's breakdown voltage. In the suggested construction, the drift zone of a typical LDMOSFET is changed by placing trenches. The N^+ polysilicon gate is located in one trench, while the oxide is located in the other trench. Since a channel is constructed vertically in the P-body region of the proposed device, it is a trench-gate device.

The channel in a p-body carries current vertically from the drain to the source for positive drain voltages when a positive gate voltage that is higher than the threshold voltage is applied. This increases the output current of the proposed device's while improves transconductance simultaneously resulting in increased cut-off frequency (f_T). Due to enhancement in the RESURF effect brought on by the presence of trenches in the drift zone, the TG-LDMOS displays a greater breakdown voltage. Despite this, the TG-LDMOS offers higher ON-resistance due to an increase in the length of the drift zone and the cross-area for drain current flow. However, because of a significant improvement in breakdown voltage, the total figure of merit rises.

3. Results and Discussion

The performance of both Con. LDMOS and TG-LDMOS structures is assessed and contrasted using two-dimensional simulations in the device simulator ATLAS [10]. We developed identical models with parameters to replicate the terminal characteristics of devices as well as structures in the device simulator for the simulation investigation. Shockley-Read-Hall, concentration-dependent mobility, electric-field-dependent mobilities, and impact ionisation (IMPACT SELB) are some of these models. Further, the carrier mobility in the channel area of both devices was calculated using the drift-diffusion model. The simulated output characteristics of Con. LDMOS and TG-LDMOS devices are shown in Fig. 2. Due to the development of a vertical channel that carries drain current in parallel in the proposed device, it has been discovered that the drain current of TG-LDMOS is larger than that of Con. LDMOS device for all gate voltages (V_{GS}).

The output drain current at V_{GS}=8V, measuring 0.97 and 0.55 mA/µm for the proposed and conventional devices, respectively which leads to the 1.7 times increase I_D of the proposed device in comparison to the traditional device. Additionally, for Con. LDMOS and TG-LDMOS, respectively, the specific ON-resistance computed from the linear section of output characteristics is determined to be 74 and 85 mΩ.mm^2. A greater ON-resistance is achieved for TG-LDMOS due to the drift region length and cross area for drain current flow increase for the proposed device.

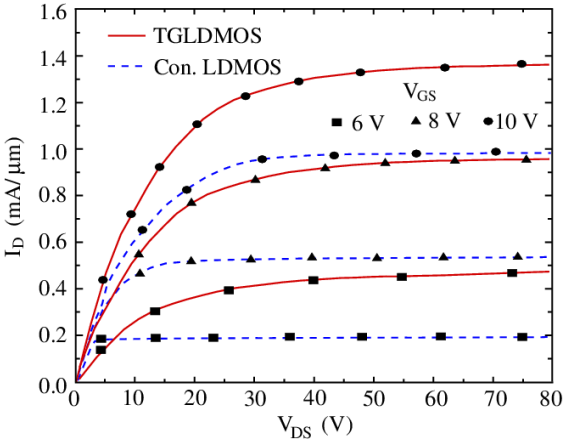

Fig. 2. *Output characteristics of the Con. LDMOS and TG-LDMOS*

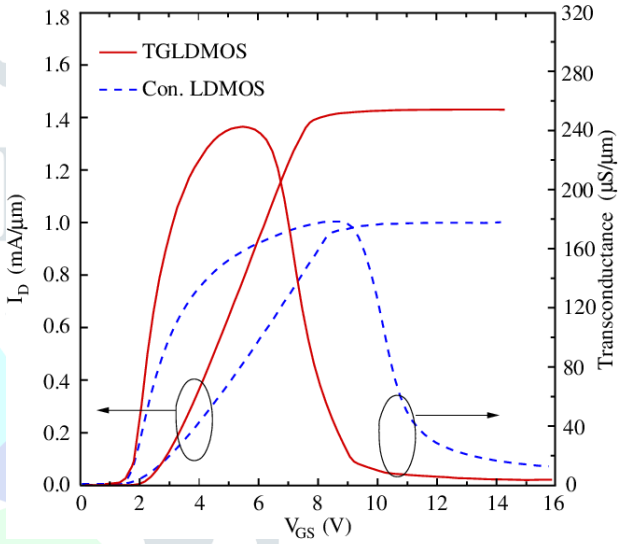

Fig. 3. *Variation of I_D and g_m with V_{GS} of the conventional LDMOS and DGTLDMOS.*

Fig. 3 displays the transfer characteristics of both configurations. The threshold voltage of a device is calculated from these features as the intercept of a tangent made at the point where the curve's greatest slope meets the gate voltage axis. TGLDMOS has a 2.8 V threshold voltage compared to a 3.2 V threshold voltage for Con. LDMOS. The suggested structure's lower threshold voltage value implies that the device's drain current achieves a set level at a relatively lower gate voltage. Figure 3 also displays the transconductance curves for both devices. We can observe that the transconductance of the proposed device is significantly greater than that of Con. LDMOS. Peak transconductance for DGTLDMOS and CLDMOS devices was determined to be 250 and 180 µS/µm, respectively, provide 1.3 times increase in peak transconductance. The suggested device's higher transconductance demonstrates its applicability for RF amplifier applications.

Fig. 4 compares the breakdown characteristics of the TG-LDMOS and Con. LDMOS under off-state conditions, when there is no gate terminal bias applied. The breakdown voltage of the TG-LDMOS occurs at 320 V while the breakdown voltage of the Con. LDMOS is only 170 V for similar drift region doping. This increases the breakdown voltage of the suggested structure by 1.8 times. Because of the suggested device's reduced electric field in the drift area, the breakdown voltage has improved.

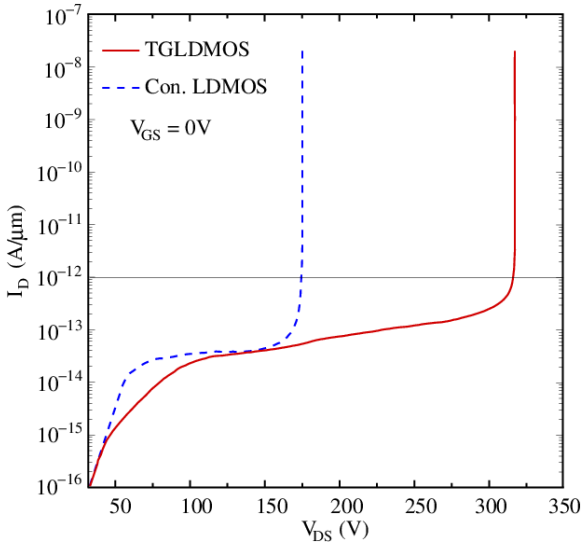

Fig. 4. *Breakdown characteristics of the Con. LDMOS and TG-LDMOS.*

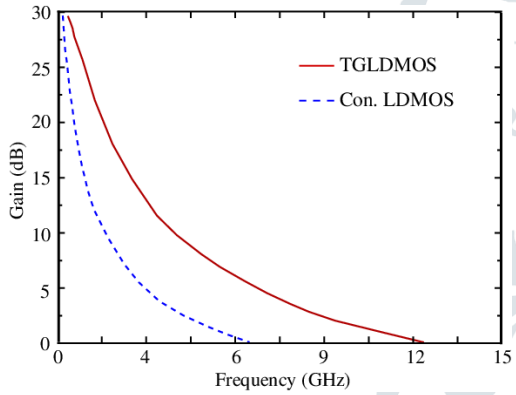

Fig. 5. *Variation of Short-circuit current gain variation with frequency of the Con. LDMOS and TG-LDMOS.*

.

The impact of frequency variation on the proposed and planar devices' short-circuit current gain is shown in Figure 5. High-frequency properties have been improved with the new structure. The cut-off frequency (f_T) of the planar and the TG-LDMOS is determined to be 6.3 and 12.2 GHz, respectively, which results in a 1.9 times improvement in comparison with the Con. LDMOS.

Although TG-LDMOS has a larger ON-resistance than Con. LDMOS, we have found that a significant increase in breakdown voltage results in a better trade-off between ON-resistance (R_{ON}) and breakdown voltage (V_{br}). This trade-off is illustrates as the Baliga's figure-of-merit ($BFOM=V_{br}^2/R_{ON}$), which should be as high as feasible for a greater power LDMOSFET. According to calculations, the BFOM for Con. LDMOS and TG-LDMOS is 3.9 and 12 MW/cm^2, respectively. In comparison to the traditional device, this results in a 3 times improvement in the BFOM of the proposed device.

4. Conclusion

A TG-LDMOS structure on 4H-SiC for integrable trench-gate LDMOSFETs has been introduced. The suggested device comprises of a gate electrode that is positioned vertically in a trench. A vertical gate employed to build parallel drain current channel in the p-body region, which increases the device's output current and transconductance. The TG-LDMOS incorporates a second trench filled with oxide in the drift zone, which lowers the electric field and significantly improves breakdown voltage of the proposed device. The TG-LDMOS device gives a 4 times greater Baliga's figure-of-merit than the conventional device for the same cell pitch, improving trade-off between ON-resistance and breakdown voltage.

References

1. Saha and J. A. Cooper, “A 1-kV 4H-SiC power DMOSFET optimized for Low ON-Resistance,” vol. 54, pp. 2786 – 2791, Oct 2007.
2. G. I. Gudjnsson, F. Allerstam, E. . Sveinbjrnsson, P.-k. N. Hans Hjelmgren, K. Andersson, H. Zirath, T. Rdle, and R. Jos, “Design and Fabrication of 4H-SiC RF MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 54, pp. 3138 – 3145, Dec 2007.
3. R. S. Howell, S. Buchoff, S. V. Campen, T. R. McNutt, A. Ezis, B. Nechay, C. F. Kirby, M. E. Sherwin, R. C. Clarke, and R. Singh, “A 10-kV Large-Area 4H-SiC Power DMOSFET With Stable Subthreshold Behavior Independent of Temperature,” *IEEE Transactions on Electron Devices*, vol. 55, pp. 1807 – 1815, Aug 2008.
4. M. Noborio, J. Suda, and T. Kimoto, “4HSiC Lateral Double RESURF MOSFETs With Low ON Resistance,” *IEEE Transactions on Electron Devices*, vol. 54, pp. 1216 – 1223, May 2007.
5. S. Harada, M. Okamoto, T. Yatsuo, K. Adachi, K. Fukuda, and K. Arai, “8.5 mΩ.cm2 600 V Double Epitaxial MOSFETs in 4HSiC ,” *IEEE Electron Device Letters*, vol. 25, pp. 292 – 294, May 2004.
6. R. S. Howell, S. Buchoff, S. V. Campen, T. R. McNutt, H. Hearne, A. Ezis, M. E. Sherwin, R. C. Clarke, and R. Singh, “Comparisons of Design and Yield for Large-Area 10-kv 4H-SiC DMOSFET,” vol. 55, pp. 1816 – 1823, Aug. 2008.
7. J. Wang, A. Q. H. Jun Li, R. Callanan, F. Husna, and A. Agarwal, “Characterization, Modeling, and Application of 10-kV SiC MOSFET,” *IEEE Transactions on Electron Devices*, vol. 55, pp. 1798 – 1806, Aug 2008.
8. Agarwal, H. Fatima, S. Haney, and S.-H. Ryu, “A New Degradation Mechanism in High-Voltage SiC Power MOSFETs,” *IEEE Electron Device Letters*, vol. 28, pp. 587 – 589, July 2007.
9. R. Singh, D. C. Capell, M. K. Das, L. A. Lipkin, and J. W. Palmour, “Development of High-Current 4HSiC ACCUFET,” *IEEE Transactions on Electron Devices*, vol. 50, pp. 471 – 478, Feb 2003.
10. “ATLAS user’s manual: Device simulation software, Silvaco Int., Santa Clara, CA,”2010.