A Review on Low power efficiency of Novel Sleep Transistor on 180nm

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***Abstract*--In the technology of nanotechnology, excessive overall performance feature is embedded into small scale tool. As the technology is improving into micro scale to deep submicron scale, and the transistor size is cut back. As the end result power intake, signal energy, speed and tool length minimizing are predicament undertaking. Generally chip encompass a million of transistor. So a lots of parameters optimization related to transistor together with strength dissipation is take care for circuit synthesis.**

Keywords: CMOS, Power Dissipation, Novel Sleep, Transistor.

1. Introduction:

With reducing channel length for successive technology generations, threshold voltage and gate oxide thickness are also being scaled down. Leakage current consequently increases exponentially with reduction in threshold voltage. As per the ITRS [1], leakage current is going to be a limiting factor for successive scaling down of transistors. Due to the smaller feature sizes in nanometre technologies, shorter channel lengths cause subthreshold current to increase when the transistor is in the off state. The lower subthreshold voltage gives rise to increased subthreshold current as well, because transistors cannot be switched off completely. Since with every successive technology the number of transistors per given area is on a rise, the leakage power in an integrated circuit for successive generations is increasing , because transistors leak even when they are not activated and significant power dissipation takes place even during inactive state of circuits.

Thus it is essential to reduce static power during the idle or standby mode of operation of the circuits. SRAMS are integral and vital components of almost all processors, SOCs and Embedded Systems and are occupying a larger area on chips. Various leakage power reduction methods are invariably applied to SRAMs to save valuable battery resources in hand held mobile applications.

Since SRAM peripheral circuits such as input drivers, word line drivers, and output drivers occupy major portion of on chip caches in processors, savings in leakage power of peripheral circuits is also advantageous for better performance. Since the on chip memory utilisation might involve long inactivity states during cache misses or might be spending larger time in idle or sleep modes in some applications, static power reduction is going to be a greater concern for such cases.

For a CMOS circuit, the total power dissipation includes dynamic and static components during the active mode of operation. In the standby mode, the power dissipation is due to the standby leakage current [2] [3].

2. Related Work:

In 1994 Shin'ichiro Mutoh et. Al proposed their work related to 1 -V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS.In this work stated that 1-V power supply high-speed low-power digital circuit technology with 0.5-pm multithreshold-voltage CMOS (MTCMOS) is proposed. This technology features both lowthreshold voltage and high-threshold voltage MOSFET's in a single LSI. The low-threshold voltage MOSFET's enhance speed Performance at a low supply voltage of 1 V or less, while the high-threshold voltage MOSFET's suppress the stand-by leakage current during the sleep period. This technology has brought about logic gate characteristics of a 1.7-11s propagation delay time and 0.3-pW/MHz/gate power dissipation with a standard load. In addition, an MTCMOS standard cell library has been developed so that conventional CAD tools could be used to lay out low-voltage LSI's. To demonstrate MTCMOS's effectiveness, a PLL LSI based on standard cells was designed as a carrying vehicle. 18-MHz operation at 1 V was achieved using a 0.5-µm CMOS process. Multithreshold-voltage CMOS (MTCMOS) circuit technology has been proposed as a way to achieve a 1-V supply voltage high-speed and low-power LSI operation. This technology uses MOSFET's with two different threshold voltages on a single chip and introduces a sleep control scheme for efficient power management. Low-threshold voltage MOSFET's improving the speed performance at a low supply voltage of 1 V, while high-threshold MOSFET's suppress the standby power dissipation. In addition, a standard cell library has been developed to simplify low-voltage LSI designs. To demonstrate the effectiveness of this technology, a PLL LSI based on standard cells was designed as a carrying vehicle using a 0.5-µm CMOS process. High-speed operation of 18 MHz at 1 V confirmed the validity of this new technology.

In 1997 James Kao et. Al proposed their work related to Transistor Sizing Issues and Tool For Multi-Threshold CMOS Technology.In this work stated that Multi-threshold CMOS was an increasingly popular circuitapproach that enables high performance and low power operation. However, no methodologies have been developed to size the high V, sleep transistor in an intelligent manner that trades off area and performance. In fact, many attempts at sizing the sleep transistor without close consideration of input vector patterns or internal structures could lead to large overestimates or large underestimates in sleep transistor sizing. In this work described some of the issues involved in sizing transistors for MTCMOS and also introduces a variable breakpoint switch level simulator that could rapidly calculate delay in MTCMOS circuits as functions of design variables such as Vdd, Vt and sleep transistor sizing. Multithreshold CMOS was becoming a very popular circuit technique for low power, high performance applications. Recently there has been a great number of MTCMOS implementations, but as this technology becomes more widestream, it will be important to develop some important sizing methodologies for the high V, sleep transistor. This work described some of the issues presented in sizing MTCMOS circuits, and then proceeded to develop a simple MTCMOS delay model that was applied to a variable break-point switch level simulator that could very quickly simulate large numbers of input vectors. The key for this tool was to provide the circuit designer with initial delay information as a function of input vector, Vdd, V,, and sleep transistor sizing, so that the they might recognize input vector patterns that may be especially susceptible in MTCMOS circuits. After the design and simulation space is narrowed sufficiently, the designer could then use a more detailed simulator like SPICE to verify circuit details.

In 2002 Mohab Anis et. Al proposed their work related to Dynamic and Leakage Power Reduction in MTCMOS Circuits Using an Automated Efficient Gate Clustering Technique. In this work stated that Reducing power dissipation is one of the most principle subjects in VLSI design today. Scaling causes subthreshold leakage currents to became a large component of total power dissipation. This work presented two techniques for efficient gate clustering in MTCMOS circuits by modeling the problem via Bin-Packing (BP) and Set-Partitioning (SP) techniques. An automated solution is presented, and both techniques was applied to six benchmarks to verify functionality. Both methodologies offer significant reduction in both dynamic and leakage power over previous techniques during the active and standby modes respectively. Furthermore, the SP technique takes the circuit's routing complexity into consideration which is critical for Deep Sub-Micron (DSM) implementations. Sufficient performance is achieved, while significantly reducing the overall sleep transistors' area. Results obtained indicate that they proposed techniques could achieve on average 90% savings for leakage power and 15% savings for dynamic power. Two techniques was applied to efficiently cluster gates in MTCMOS circuits. The first gives the minimum number of sleep transistors to be employed, while the second takes the circuit's routing complexity into consideration. On average the BP technique reduces dynamic and leakage power by 15% and 90% respectively. The SP technique also reduces dynamic and leakage power on average by 11% and 77% respectively. Future work involves improving the computation time involved to solve the SP and BP problems by using heuristic search techniques in the form of Genetic Algorithms that were suitable for multi-objective optimization problems.

In 2003 Changbo Long et. Al Described their work related to Distributed Sleep Transistor Network for Power Reduction .In this work described that Sleep transistors are effective to reduce dynamic and leakage power. The cluster-based design was proposed to reduce the sleep transistor area by clustering gates to minimize the simultaneous switching current per cluster and then inserting a sleep transistor per cluster. In this work, they proposed a novel distributed sleep transistor network (DSTN), and show that DSTNi s intrinsically better than the cluster based design in terms of the sleep transistor area and circuit performance. They reveal properties of optimal DSTN designs, and then develop an efficient algorithm for gate level DSTNs synthesis. The algorithm obtains DSTNde signs with up to 70.7% sleep transistor area reduction compared to cluster-based designs. Furthermore, they present custom layout designs to verify the area reduction by DSTN. Sleep transistors were effective to reduce both dynamic and leakage power. They have proposed a novel distributed sleep transistor network (DSTN), and have convincingly illustrated that DSTNha s reduced area, less supply voltage drop, and no conflict with timing-driven placement when compared to existing module-based and cluster-based sleep transistor structures. They have revealed several properties of the optimal solution to the DSTN sizing problem, and have proposed an effective and efficient DSTNsizin g algorithm based on these properties. Based on the experimental comparison with a rigorous cluster-based design, DSTN assuming conservative virtual-ground wires achieves on average 49.8% sleep transistor area reduction and leads to less performance lost. Having these advantages, DSTN could be used to implement power gating for reducing dynamic and leakage power. Sleep transistor could be viewed as an essential part of the power/ground network. They assumed that the power/ground network (both global and virtual) was given a priori in this work, and plan to investigate the co-design of DSTN and power/ground network in the future.

In 2003 Suhwan Kim et. Al described their work related to Understanding and Minimizing Ground Bounce during Mode Transition of Power Gating Structures. In this work they introduced and analyze the ground bounce due to power mode transition in power gating structures. To reduce the ground bounce, they proposed novel power gating structures in which sleep transistors were turned on in a non-uniform stepwise manner. Their power gating structures reduce the magnitude of peak current and voltage glitches in the power distribution network as well as the minimum time required to stabilize power and ground. Experimental simulation results with PowerSpice fixtured in a package model demonstrate the effectiveness of the proposed power gate switching noise reduction techniques. This work investigates the ground bounce caused by large discharge current through a sleep transistor during the mode transition of the power gating structure. Two novel power gating structures were proposed to reduce the magnitude of voltage glitches in the power distribution network as well as the time required for the network to stabilize. In Power Spice simulation of a 16-bit arithmetic and logic unit (ALU) with a DIP-40 package model, the maximum magnitude of voltage glitches on the VDDL and GNDL rails of the ALUs with their power gating structures were reduced by up to 89.04% and 88.40%, respectively, compared to the ALU with a conventional gating structure. At the same time, the time required for VDDL and GNDL rails to stabilize is reduced by up to 81.16%.

In 2004 Jason H. Anderson et. Al described their work related to A Novel Low-Power FPGA Routing Switch. In this work they proposed a new programmable FPGA routing switch that could operate in three different modes: high-speed, low-power or sleep. High-speed mode offers similar power and performance to a traditional routing switch. In low-power mode, power is reduced at the expense of speed. Leakage power is reduced by 36-40% in low-power vs. high-speed mode (on average); dynamic power is reduced by up to 28%. Leakage power in sleep mode is 61% lower than in high-speed mode. The applicability of the new switch is motivated through an analysis of timing slack in industrial FPGA designs. Specifically, they shown that a considerable fraction of routing switches might be slowed down (operate in low-power mode), without impacting overall design performance. Static and dynamic power dissipation in FPGAs was dominated by that consumed in the interconnection fabric, making low power interconnect a mandatory feature of future low-power FPGAs. In this work, they proposed a new FPGA routing switch that could be programmed to operate in high-speed, low power or sleep mode. Leakage in low-power mode was reduced by 36-40% vs. high-speed mode; dynamic power was reduced by up to 28%. Sleep mode offers leakage reductions of 61%. They showed that timing slack in typical FPGA designs permits the majority of switches to operate in low-power mode. The switch requires only minor changes to a traditional PGA routing switch and had no impact on router complexity, making it easy to deploy in current commercial FPGAs.

In 2004 Suhwan Kim et. Al proposed their work related to Experimental Measurement of A Novel Power Gating Structure with Intermediate Power Saving Mode. In this work stated that A novel power gating structure was proposed for low-power, high-performance VLSI. This power gating structure supports an intermediate power saving mode as well as a traditional power cut-off mode. To evaluate their power gating structure, They design and fabricate three different macros in 0.13 µm CMOS bulk technology. Their measurement results show that the additional intermediate power-mode allows us to cover various power-performance trade-off regimes, compared to conventional power gating structures. A power gating structure with two power saving modes for both high leakage reduction without state retention and intermediate leakage reduction with state retention was proposed and evaluated. Representative logic circuits with and without power gating circuit were designed and fabricated in 0.13 µm CMOS bulk technology. Measured results show when moderate area overhead was dedicated to the sleep transistor of power gating structure (< 2.6%), maximum operating frequency decreases by less than 2.0%. Leakage current was dramatically reduced when the ground supply to the logic circuit was interrupted by the switch and was moderately reduced (slightly better than by a fact of two) when the builtin PFET switch was used to reduce the rail-to-rail voltage. Ground bounce induced by switching between power modes were measured as well as it was effect on performance of neighboring circuits. The intermediate leakage saving mode was shown to significantly reduce the ground bounce and effect on the neighboring circuit performance.

In 2004 Fei Li, et. Al proposed their work related to FPGA Power Reduction Using Configurable Dual-Vdd .In this work described that power optimization is of growing importance for FPGAs in nanometer technologies. Considering dual-Vdd technique, they show that configurable power supply was required to obtain a satisfactory performance and power tradeoff. They designed FPGA circuits and logic fabrics using configurable dual-Vdd and develop the corresponding CAD flow to leverage such circuits and logic fabrics. They then carry out a highly quantitative study using area, delay and power models obtained from detailed circuit design and SPICE simulation in 100nm technology. Compared to single-Vdd FPGAs with optimized Vdd level for the same target clock frequency, configurable dual-Vdd FPGAs with full and partial supply programmability for logic blocks reduce logic power by 35.46% and 28.62% respectively and reduce total FPGA power by 14.29% and 9.04% respectively. To the best of their knowledge, that was the first in-depth study on FPGAs with configurable dual-Vdd for power reduction. They have shown that configurable Vdd was required to obtain a satisfactory performance and power tradeoff in FPGAs. They have designed circuits and logic fabrics using programmable dual Vdd, and have developed a CAD flow to leverage such circuits and logic fabrics. They have carried out a highly quantitative study using area, delay and power models obtained from detailed circuit design and SPICE simulation in 100nm technology. Compared to single-Vdd FPGAs with Vdd level optimized for the same target clock frequency, dual-Vdd FPGAs with full supply programmability for logic blocks reduce logic power by 35.50% and increase logic block area by 24%. Dual-Vdd FPGAs with partial supply programmability reduce logic power by 28.62% and increase logic block area by 14%. Because FPGA chip area is mainly determined by routing area, such logic area increase is not significant. To the best of our knowledge, it is the first in-depth study on FPGAs with configurable dual-Vdd. Power supply network to support configurable Vdd or dual-Vdd may introduce extra routing congestion. Leveraging our recent research on optimal synthesis of sleep transistors and power supply network . They have studied power delivery design and optimization for configurable dual-Vdd FPGAs. Currently, They only applied configurable Vdd to logic blocks. The total power reduction percentage for dual-Vdd FPGAs is significantly lower than the logic power reduction percentage. They studied how to reduce interconnect power by dual-Vdd in the future.

In 2006 Kaijian Shi et. Al proposed their work related to Challenges in Sleep Transistor Design and Implementation in Low-Power Designs. In this work stated that Optimum power gating sleep transistor design and implementation were critical to a successful low-power design. This work described important considerations for the sleep transistor design and implementation including header or footer switch selection, sleep transistor distribution choices and sleep transistor gate length, width and body bias optimization for area, leakage and efficiency. It also investigated various power-on current rush control methods for the sleep transistor implementation. Although the concept of sleep transistor was simple, optimum sleep transistor design and implementation were challenge. They required optimizing gate length, width, body bias and finger configuration with overall considerations of efficiency, leakage, drive, area and IR-drop effects which are often conflicting and need to be weighed based on application requirements. Increasing Lgate results in higher Vth and hence lower leakage and higher Ion/Ioff efficiency, at the price of significant increase of Ron and decrease of Ion. Applying optimal reversed body bias is more efficient and effective alternative to produce a higher efficiency and Ion and lower Ron and Ioff sleep transistor than by increasing Lgate. Correct choices in sleep transistor implementations such as header or footer switch and ring or grid distributions were also important. Current rush at power-on is a critical issue in the sleep transistor implementation. It could cause large IR-drop and short term VDD collapse resulting in malfunctions in the design. Among various current rush control methods, the two stage charge method was most effective. The size and number of the weak transistors are largely determined by the power-on current rush limit. The main header turn-on can be controlled by a design dependent delay circuit using the weak transistor daisy-chain or a voltage detector such as a Schmitt trigger. The main headers could be configured as clusters or daisy chains which were turned on in sequence. The configurations and optimal number of chains were determined based on max peak current and power-on latency budget.

Static power has become the most important factor in the fabrication of integrated circuits. Power gating techniques minimize leakage currents and help to develop ultra-low{power and high-performance digital circuits. In **Kavitha et. al. (2016) [12]** a power gating approach is proposed to minimize leakage for subnanometer technologies. Simulation results reveal that the proposed technique reduces maximum of 96% leakage power, 33% dynamic power, 49% drowsy power, and 16% energy as compared to conventional techniques. The proposed technique offers good leakage reduction, even under variation of different operating parameters.
In this work, an effective power gating technique to reduce leakage, drowsy and dynamic power in generic logic circuits is proposed. It is apparent from the power characteristics that the LPMS approach is better than conventional techniques. The LPMS technique also minimizes energy consumption to a maximum of about 16% over other approaches. The proposed LPMS technique provides excellent leakage and drowsy power reduction even when sleep transistor width, threshold voltage, and temperature change. LPMS technique can be used in applications like wireless sensor nodes, SoC, and microprocessors to extend the battery life of these devices.

Full subtractor is a combinational circuit that performs subtraction between the three inputs and provides result in difference and borrow outputs. Implementing the MTCMOS technique on this circuit results in reduction of leakage current and power consumption. The proposed Full Subtractor has been designed and simulated using DSCH 3.1 and MICROWIND 3.1 software. The simulation technology used is 45 nm. The simulation level is BSIM advanced level. The proposed design power consumption calculated as 0.341 mW and maximum current Idd max equal to 2.420 mA at 0.7 Supply voltages.
In **Tanvi Nagariya et. al. (2016), [13]**, reduction in average power which leads to reduction in leakage current and dynamic power dissipation is analyzed for conventional and modified Full Subtractor circuits using Microwind / DSCH tool in 45nm technology. Proposed Full Subtractor circuits in MTCMOS mode is analyzed in terms of power, current, area. The proposed design power consumption calculated as 0.341mW, maximum current equal to 2.420 mA and average current as 0.487 mA at 0.7 Supply voltages. The simulation level is BSIM advanced level. The completion of this main task was satisfactory since the theoretical expectations matched our experimental results.

The most vulnerable of these circuits are memory arrays that cover large areas of the silicon die and often store critical data. Radiation hardening of embedded memory blocks is commonly achieved by implementing extremely large bit cells or redundant arrays and maintaining a relatively high operating voltage. However, in addition to the resulting area overhead, this often limits the minimum operating voltage of the entire system leading to significant power consumption. In this paper, we propose the first radiation-hardened static random access memory (SRAM) bit cell targeted at low-voltage functionality, while maintaining high soft-error robustness. **Mutha Jyothi et. al. (2017) [14],** proposed A novel sleep techniques was at circuit level for the reduction of power consumption, delay and leakage.
Sub threshold leakage power consumption is a great challenge in nano-meter scale (CMOS) technology, although previous techniques are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, based upon technology & design criteria the designers can choose the techniques. In this paper, we provide novel circuit structure in terms of static & dynamic powers named as “sleep method” it’s a new remedy for designers. This technique shows the least speed power product among all techniques. The Proposed technique achieving ultra-low leakage power consumption with much less speed, especially it shows nearly 50-60% of power than the existing. So, it can be used for . future IC'S for area & power Efficiency

In this work, **Manisha B S et. al. (2018),** [15] present two different methods to implement 1-bit full adder namely MTJ based full adder design also called MFA and Lector method based full adder design. These adders are designed and implemented using CADENCE Design Suite 6.1.6 Virtuoso ADE. The implemented design is verified using CADENCE ASSURA. The performance is measured for 45nm technology and a comparative analysis of transistor count; delay and power of the adders were performed. When compared with the previous MFA the proposed MFA overcomes the SEU error which is a result of body biasing. In Lector technique the transistor density is reduced by implementing the sum logic in terms of carry thus reducing the area. In order to attain the complete logic levels buffers are introduced at the sum and carry outputs of both Lector and MFA. The Lector method uses less number of transistors when compared with proposed MFA, but the proposed MFA is efficient because it achieves minimum power dissipation when compared to the Lector method.
The LECTOR approach has an advantage of not impacting the dynamic power and additionally in this method; less number of transistors are used when compared to the circuit in [14]. The proposed MFA circuit offers SEU tolerance. The proposed MFA circuit consumes less power when compared to the Lector method. To summarize, we can assert that the magnetic full-adder is efficient since the

power dissipation in adder circuit is less when compared with the lector technique.

In **Hemlata et. al. (2018) [16],** inverter pairs are designed using leakage power reduction technique known as sleepy stack technique. The static CMOS inverter in conventional DDFF is replaced by sleepy stack inverters because as feature size scales down below 0.1u leakage power gets increased. The simulations were performed under 90 nm technology in Tanner Tool. The supply voltage is given as 1.8V throughout for the entire simulation analysis. The leakage power and total power for static CMOS inverter and sleepy stack inverter were compared. It is observed that sleepy stack inverter has reduced leakage power to 98% and the total power is reduced to 14.2%. The total power is reduced to approximately 18%, in proposed D, flip flops. The leakage power is reduced to 90.1%. As proposed flip-flop has improved performance in term of leakage power, total power and power delay at high speed, it can be widely used in high performance application.

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Power can be further reduced by using adiabatic logic which utilizes low input as a supply voltage instead of supply. Dynamic families can also be integrated at ease with different flip flops in order to improve the speed of device.

4. Conclusion

With the continuous technology scaling devices, the power consumption is of exquisite challenge for designs in nanometer technologies and is becoming a main contributor to the whole power consumption; leakage power has turn out to be more dominant compared to Dynamic electricity. The gate leakage has come to be dominant resources of leakage and is predicted to growth with the era scaling. The answers for leakage energy dissipation or reduction of leakage power dissipation must be sought both on the system technology and circuit tiers. Here we very well reviewed the work of different authors in area of Power dissipation.

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