Reduction of voltage sags and harmonics by using dynamic voltage restorer

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***Abstract*—a Dynamic voltage restorer (DVR) is introduced to reduce voltage sags and harmonics is preferred. In this work, the construction of the DVR has shunt and series converters coupled back to back by a dc- to dc step up converter. The existence of the dc to dc step up converter access the DVR to reduce voltage sags for longer period. The series converter coupled to the supply side and the shunt converter coupled to the load side. By this, no requirement for using long dc capacitors in this. The control strategy of the recommended DVR is rests on the hysteresis voltage control. The recommended DVR is simulated using MATLAB/SIMULINK. Time domain simulations are preferred to examine the working and behavior of the DVR with linear and non-linear loads**

keywords—dynamic voltage restorer; total hormonic distortion; dc-dc step upconverter;harmonics; voltage sags

1. INTRODUCTION

Dynamic voltage restorer (DVR) is a series coupled flexible ac transmission systems (FACTS) controller adopted to reduce voltage sags in uneven situations in distribution systems. The DVR has distinct system techniques. These techniques are: (i) DVR with no storage and supply-side coupled shunt converter, (ii) DVR with no storage and load-side-coupled shunt converter, (iii) DVR with energy storage with varying dc-link-voltage and (iv) DVR with energy storage and with constant-dc link voltage. The preferred DVR is a DVR with no storage and load side coupled shunt converter to acquire maximum gains from the device. The control strategy has two control loops; the internal loop for producing the gate signal of the switches of the DVR and the external loop for the reference voltage signal of the DVR.

2. CONFIGURATION AND CONTROL OF DVR

The shunt converter coupled to the load side is uncontrolled rectifier, has uncontrollable dc output voltage V_{dc1}. The uncontrolled rectifier is coupled to the load bus by a step down transformer. The dc resultant voltage of the rectifier V_{dc1} is the input voltage of the dc-to-dc step up converter. The resultant voltage of the step up converter V_{dc2} is the input dc voltage of the VSC of the DVR. By this, the uncontrolled rectifier receives non-linear current, the DVR can able to reduce all harmonics obtained with the load voltage.

2.1 DC VOLTAGE CONTROL OF THE DVR

The step up converter restricts the duty cycle D to withstand its dc output voltage V_{dc2} at the reference value V_{dcref}. It can be achieved using proportional and integral (PI) controller as shown in Fig. 1. The PI controller compares between V_{dcref} and V_{dc2} to cause the error e_{vdc}. The error e_{vdc} is passed by the PI controller to trigger the respective duty cycle D which in turns fed into the switching pulse generation block to generate the switching pulses of the MOSFET.

2.2 VOLTAGE SAG DETECTION SCHEME

Fig.2 represents a SIMULINK model of the sag detection scheme. In Fig.1 the 3-phase instantaneous output voltage (v_{sa}, v_{sb}andv_{sc}) from the voltage sag detection model is the first

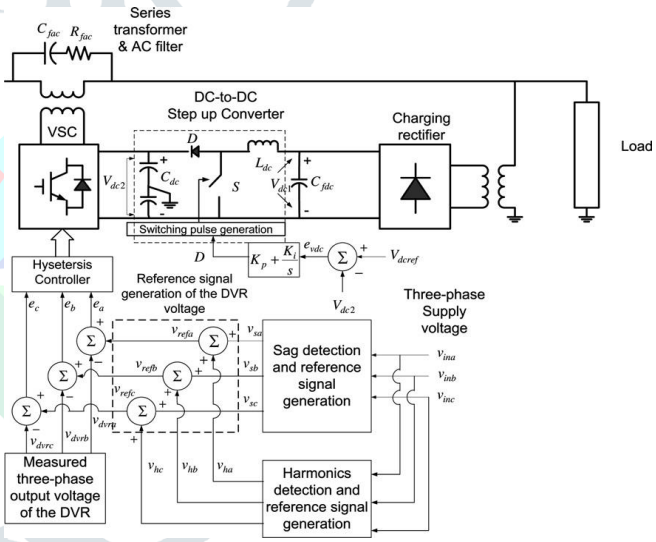


Figure1: schematic diagram of the DVR

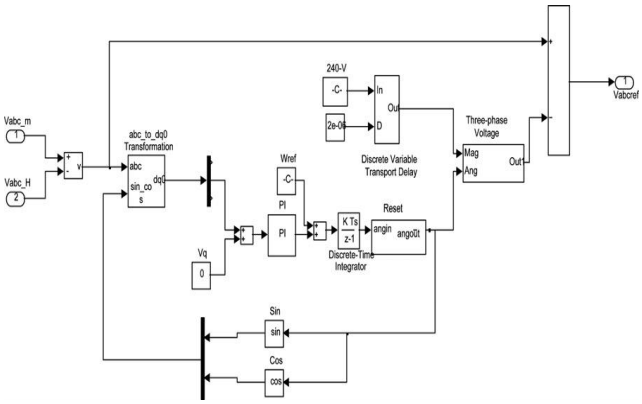


Figure2:Simulink model of the voltage sag detection

reference input to the hysteresis controller block.

2.3 HARMONIC'S DETECTION SCHEME

In the model Fig.3, the fundamental component of respective phase is taken from the equivalent distorted supply voltage. Then, the fundamental component of respective phase taken out from the equivalent distorted supply voltage to obtain the harmonics existed in its concerned phase voltage. With this arrangement, all harmonics available in the supply voltage can be detected. The harmonics, obtained in its respective phase, are the 2nd reference instantaneous input voltages (v_{ha},v_{hb} and v_{hc}) to the hysteresis controller block.

2.4 AC VOLTAGE CONTROL OF THE DVR

Standard two-level hysteresis voltage control, which is a kind of non-linear voltage control lies on the voltage error, is implemented. The hysteresis controller generates the switching pulses that are fed to the VSC. The generated 3-phase voltage o f the DVR is feed by a series transformer. As shown in Fig. 1, an ac filters (R_{fac} and C_{fac}) are coupled across the series transformer to remove the switching ripples produced by the VSC.

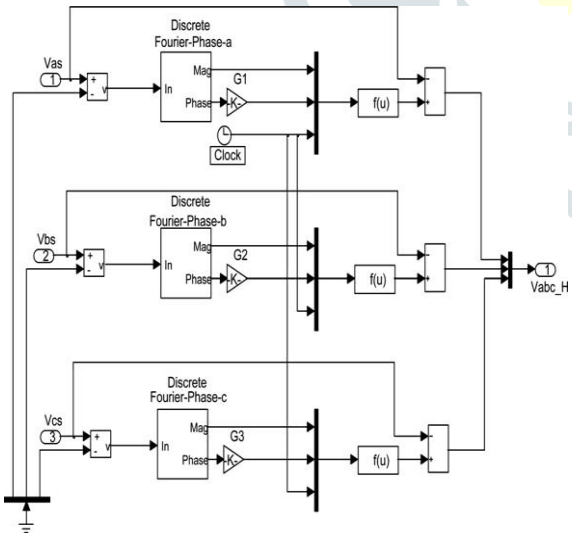


Figure3: Simulink model of the harmonics detection scheme

3. DESIGN OF DVR COMPONENTS

In this section, the dc capacitor C_{fdc} of the uncontrolled rectifier, the dc capacitor C_{dc} and the inductor L_{dc} of the dc-to-dc step up converter are designed based on 1-ϕ voltage sag which produces a voltage fluctuation with double the line frequency of the dc capacitor.

The voltage sag factor k_{sag} is notified as

$$\overline{k_{sag}} = \frac{\bar{V}\ \text{sag}}{\bar{V}\ \text{spre} - \text{sag}}$$

where $\bar{V}_{\text{sag}}$ is the sag load voltage and $\bar{V}_{\text{spre-sag}}$ is the pre-sag load voltage

The magnitude of the voltage sag factor $|\overline{k_{sag}}|$ is equal to the Depth of the voltage sag D_{sag} that is

$$D_{sag}=|\overline{k_{sag}}|$$

3.1 SIZING OF THE DC CAPACITOR C_{FDC}

The required capacitance of the dc capacitor C_{fdc} is represented as

$$C_{fdc}=\frac{D_{sag}V_{sL-L}I_L\cos\varphi}{2\sqrt{3}\omega\varepsilon V_{dc1}{}^2(3-D_{sag})}$$

Where V_{sL-L} is the line-line rated load voltage, I_L is the rated load current, cosφ is the power factor of the load, ω is the angular speed ($\omega=2\pi f$), ε is the allowable dc voltage fluctuation ($\varepsilon = \Delta V_{dc1}/V_{dc1}$) and$V_{dc1}$ is the dc voltage of the uncontrolled rectifier. The dc voltage of the uncontrolled rectifier (Vdc1) is almost equal to the value of line-to-line load voltage ($V_{dc1}=V_{s\ L-L}$).

$$C_{fdc}=\frac{D_{sag}I_L\cos\varphi}{2\sqrt{3}\omega\varepsilon V_{s\ L-L}(3-D_{sag})}$$

In Fig.4 As voltage sag increases, the size of the dc capacitor C_{fdc} has to be increased because the dc capacitor should supply higher Power at high sag depths.

3.2 Sizing the inductor L_{dc} and the dc capacitor C_{dc}

The inductor L_{dc} and the capacitor C_{dc} of the dc-to-dc step up converter are given as

$$L_{dc}=\frac{V_{dc1}D}{\Delta I_{dc2}f_s}$$

$$C_{dc}=\frac{I_{dc2}D}{\Delta V_{dc2}f_s}$$ where D is the duty cycle of the dc-to-dc step up converter, f_s is the switching frequency of the switch (MOSFET) of the dc-to-dc step up converter, ΔI_{dc2} is the dc output current ripple of the dc-to-dc step up converter, I_{dc2} is the dc output current of the dc-to-dc step up converter and ΔV_{dc2} is the ripple dc output voltage of the dc-to-dc step up converter. From this the inductor L_{dc} is directly proportional to the duty cycle D and the dc voltage of the uncontrolled converter V_{dc1} .since $V_{dc1}=V_{s\ L-L}$ and by taking $D=D_{max}$, then $L_{dc}=\frac{V_{sL-L}D_{max}}{\Delta I_{dc2}f_s}$

The maximum duty cycle D_{max} is given by

$$D_{max}=\frac{V_{dc2}-V_{dc1min}}{V_{dc2}}$$

Where $V_{dc2}$is the dc output voltage of the dc-to-dc converter and V_{dc1min} is the minimum dc voltage of the uncontrolled rectifier.

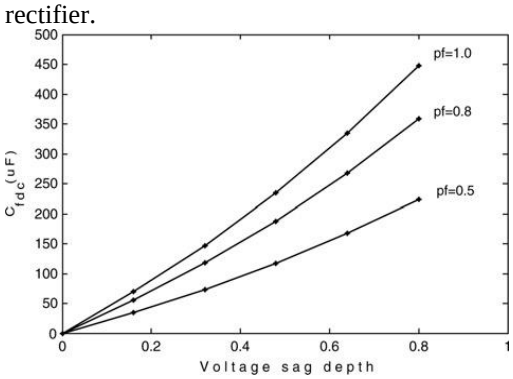


Figure4: Relation between dc capacitor c_{fdc} and voltage sag depth (D_{sag})

So finally the magnitude of the inductor L $_{dc}$ can be achieved by

$$L_{dc} = \frac{V_{sL-L}(V_{dc2}+D_{sag}V_{sL-L}-1)}{\Delta I_{dc2} f_s V_{dc2}}$$

The dc capacitor of the dc to-dc step converter C_{dc} can be achieved by

$$C_{dc} = \frac{I_{dc2}(V_{dc2}+D_{sag}V_{sL-L}-1)}{\Delta V_{dc2} f_s V_{dc2}}$$

The active power feed by the DVR during the voltage Sag, disregarding the losses in the PWM converter, is achieved by

$$P_{inj} = D_{sag}\frac{V_{sL-L}}{\sqrt{3}} I_L \cos\varphi = V_{dc2} I_{dc2}$$

Thus, the dc capacitor C_{dc} can be obtained by

$$C_{dc} = \frac{D_{sag} V_{sL-L} I_L \cos\varphi (V_{dc2}+D_{sag}V_{sL-L}-1)}{\sqrt{3}\Delta V_{dc2} f_s V^2_{dc2}}$$

In Fig.5 as the D_{sag} increases the magnitude of the inductor L_{dc} has to be increased

4. TIME DOMAIN SIMULATION

To examine the working of the recommended DVR, four different cases are introduced. They are:

1. Recompensing 60% 3-phase voltage sag with +28° Phase jump concerning linear and non-linear loads (Figs.6 and 7).

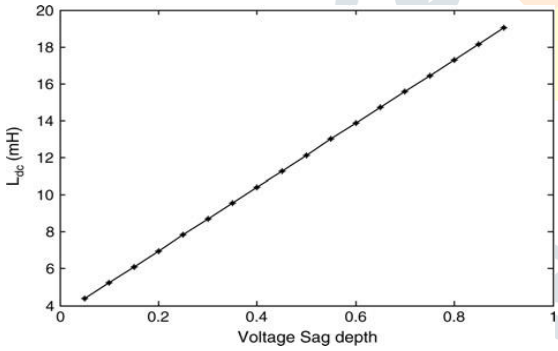


Figure5: Relation between capacitor L_{dc} and voltage sag depth (D_{sag})

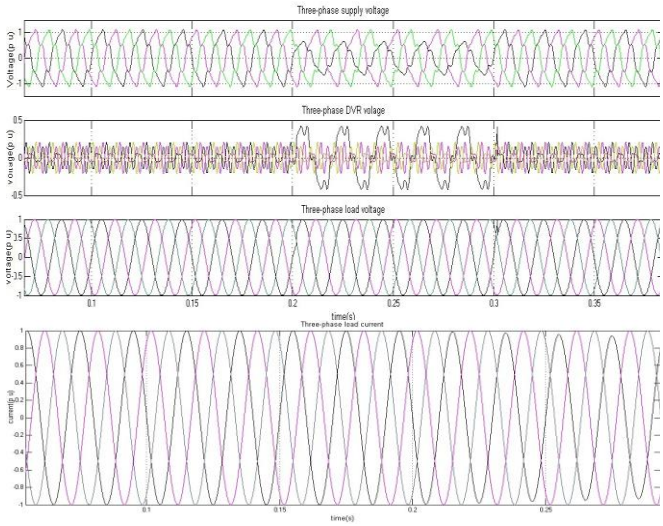


Figure6: System response because of 3-phase 60% voltage sag at +28° phase jump (linear load)

2. Recompensing supply voltage harmonics (fifth and seventh harmonics) only with linear and non-linear loads (Figs. 8and9).

3. Simultaneous Recompensing of 60% 3-phase voltage with +28°phase jump and supply voltage harmonics (fifth and seventh harmonics) with linear and non-linear loads (Figs. 10and11).

4. Simultaneous Recompensing of 50% $1-\phi$ voltage sag with +28° phase jump and supply voltage harmonics (fifth and seventh harmonics) with linear and non-linear loads (Figs. 12and13).

As the supply voltage sags, the dc voltage of the three-phase rectifier (Vdc1) falls and rests constant at lower value. To maintain the output voltage of the dc- to-dc converter at the pre setting value (V_{dc}=500 V) the PI controller enhances the duty cycle D. The duty cycle D returns to its value as the supply voltage restored.

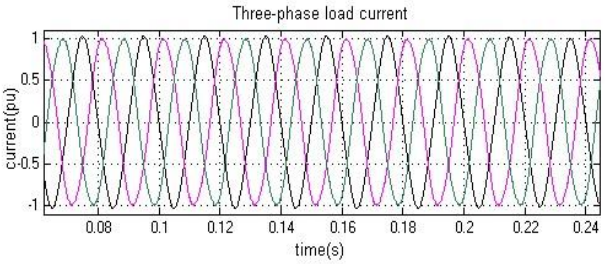
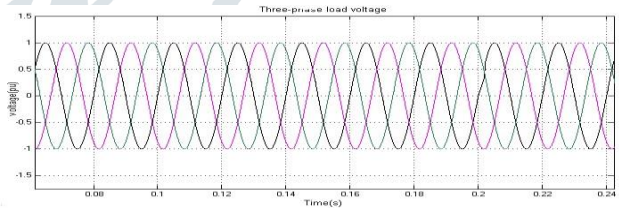


Figure: System response due to 3-phase 60% voltage sag with +28° phase jump (non-linear load)



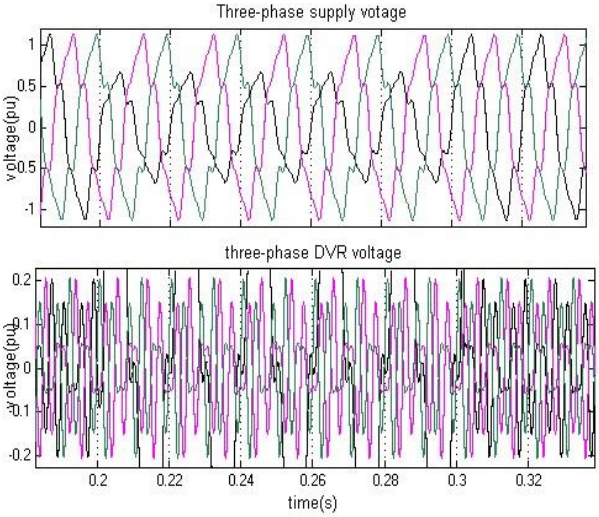


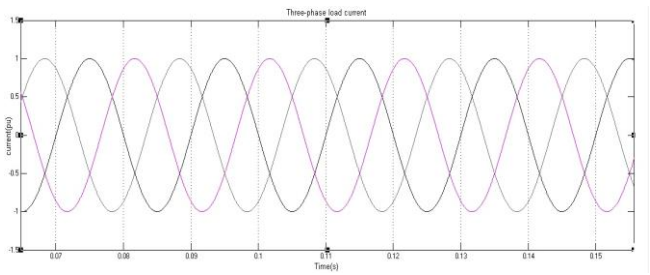
Figure7: System response due to 3-phase 60% voltage sag at +28° phase jump (non-linear load)

The distorted voltage can be obtained at 5th and 7th harmonics are with respect to the supply voltage. The value of the 5th type harmonics is 12.5% and 7th type harmonics is 8.52% of the supply voltage. The THD of the supply voltage is 15.2% in linear as well as in non linear loads whereas the THD of the load voltage is 0.4% and 0.5% for linear and non-linear loads respectively. This shows that the DVR has the ability to minimize the 5th and 7th harmonics of the supply voltage. Figs.10 and 11. Shows simultaneous steady-state harmonics and voltage sag compensation capabilities of the DVR taking account of linear and non-linear loads for 60% 3-phase voltage sag with +28°phase jump.The magnitudes of the 5th and 7th type harmonics are 12.5 and 8.52% of the supply phase voltage which are kept static during the voltage sag to take it as worst-case scenario respectively. From table1 the DVR has the ability to reduce harmonics and also the 3- phase voltage sag. It can be seen from Figs. 7, 9 and 11 that the THD of the load current is 4.2% with non-linear load. The THD of the load current can be reduced by adding an inductor in series

Table1: THD values at different loads at voltage sag conditions

Linear Load			Non-Linear Load		
S.No	Voltage	THD (In %)	S.No	Voltage	THD (In %)
1	Supply Voltage	22.22	1	Supply Voltage	22.22
2	Load Voltage	1.2	2	Load Voltage	2.1

with the non-linear load. Figs. 10and 11show, respectively, simultaneous steady state harmonics and voltage Sag compensation capabilities of the DVR with linear and non-linear loads for 50% single-phase voltage sags at +28°phase jump.



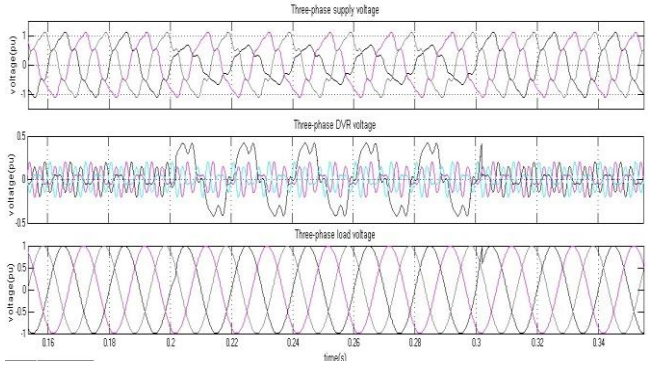
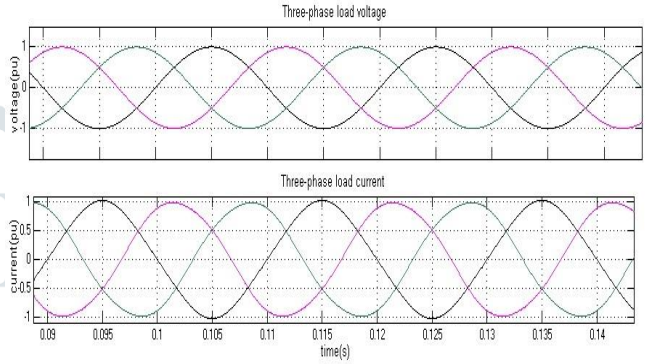


Figure8: steady-state harmonics compensation (linear load)



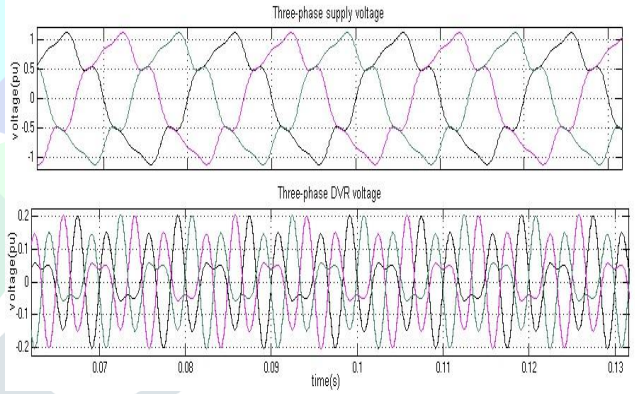
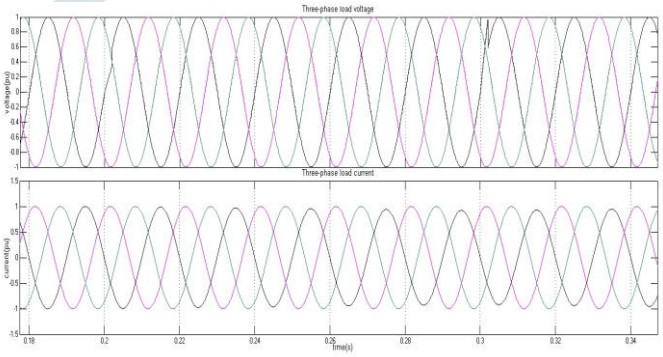


Figure 9: steady-state harmonics compensation (non-linear load)



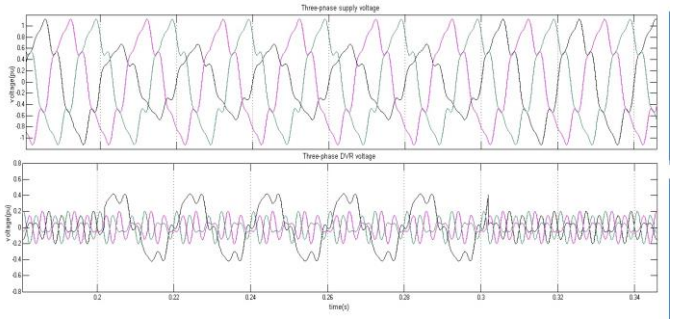


Figure10:3 -phase 60% voltage sag at +28°phase jump (linear load) and harmonic compensation

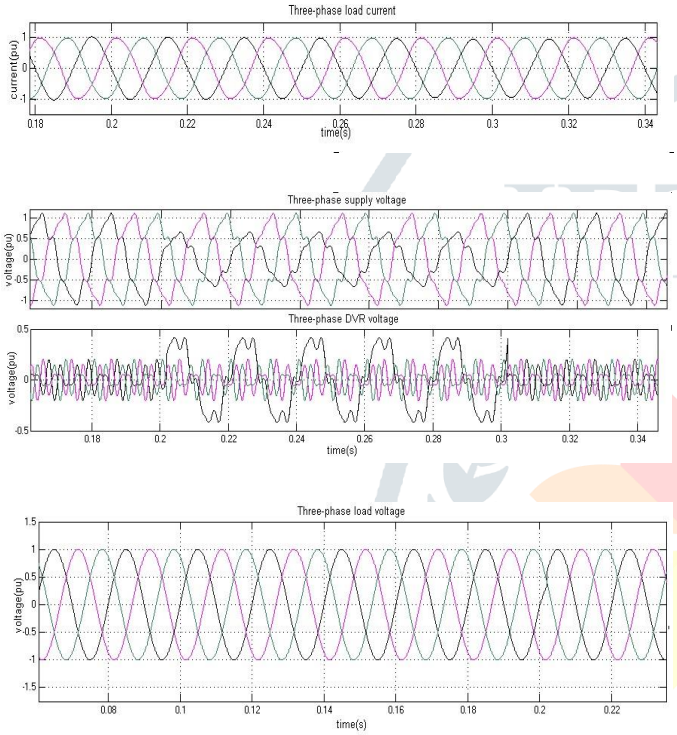
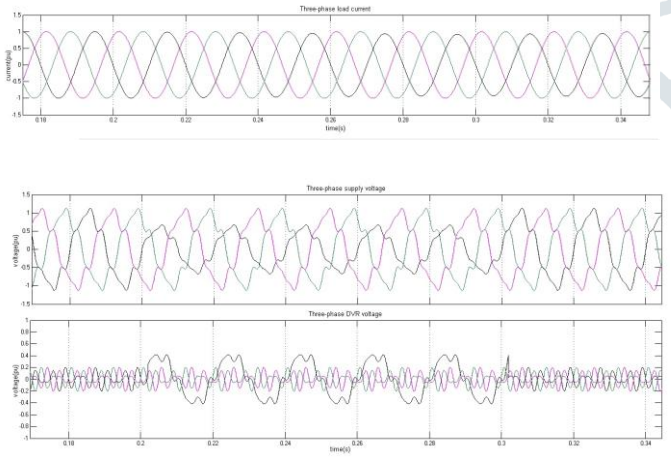


Figure11: *3-phase 60% voltage sag at +28°phase jump (non-linear load) and harmonic compensation*



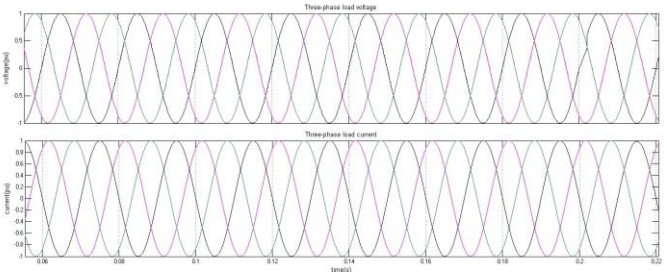


Figure 12: Single-*phase 50% voltage sag at +28°phase jump (linear load) and harmonic compensation*

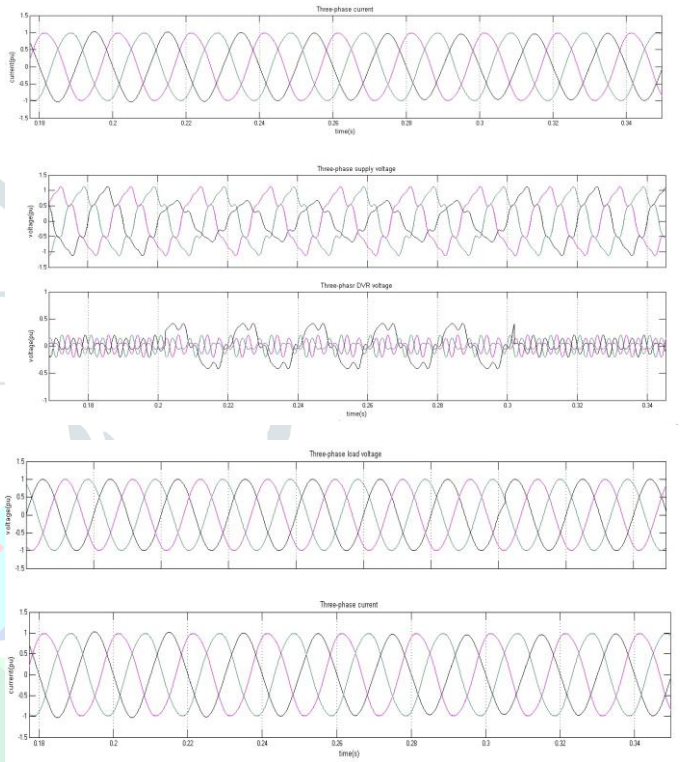


Figure13: *single -phase 50% voltage sag at +28°phase jump (non-linear load) and harmonic compensation*

The simulation test is done and the components are designed depends on the case 50% single-phase voltage sag condition. Based From Figs. 12and 13 observed that the dc voltage of the shunt rectifier V_{dc1} and the output dc voltage of the dc-to-dc step up converter V_{dc2} had fewer fluctuations.

5.CONCLUSION

This work has recommended a DVR that can be used not only reduce deep voltage sags but also to reduce Steady state harmonics simultaneously. A hysteresis voltage control method is adopted for harmonic compensation to the DVR. It shows that the shunt rectifier and the dc-to-dc step up converter needs higher dc capacitor size at higher power factor loads. Besides, it shows that when the depth of the voltage sag increases, the capacity of dc capacitors of shunt rectifier and the dc-to dc step up converter and also the capacity of the inductor of the dc to dc step up converter have to increase. Time domain simulations of the DVR, under distinct conditions including distorted supply voltage and distorted

voltage sags, have analyzed the performance of the recommended DVR.

6. REFERENCES

[1] WOODLY N.H., SUNDRAM A., COULTIER B., MORRIIS D.: 'Dynamic voltage restorer exposition project experience'. Presented at the Proce. 12th Confe. Electr. Power Supply Inds., Pattaiya, Thailaand, 1998).

[2] WOODLY N.H., MORGAAN L., SUNDRAM A.: 'Experience with An inverter fed dynamic voltage restorer', *IEEE* Transc. Power Delive. 1999, 14, (2), pp. 549–559

[3] NIEELSEN J.G., BLABJERG F.: 'A detailed comparison system topologies to dynamic voltage restorers', *IEEE* Transc. Ind. Appli., 2005, 41, (5), pp.1271–1280

[4] NIELSEN J.G., BLAABJERG F., MOHAN N.: 'Control strategy to dynamic voltage restorer reducing voltage sags with phase jumps'. Proce. *IEEE* APEC'01, 2001, volm. 2, pp. 1267–1373

[5] WEI LII Y., MAHENDAV., BLAABJERG., CHIANNG LOHP.: 'A robust control technique for medium-voltage-level dvr implementation', *IEEE* Transc. Ind. Electron., 2007, 54, (4), pp. 2249–2361

7. APPPENDIX

1. Power supply: V_{sL-L}=415V,f=50Hz
2. Dc-to-dc step up converter: Ldc =12 mH, C_{dc} =30 mF;
   DC voltage control: K_p =0:06, K_i = 0:9. D_{max} = 0.8 and D_{min} =0.15.
3. Series transformer: 240 Vphase/240Vphase, r1= r_2=0.004pu, x1=x2=0.08 Pu
4. Shunt transformer: 240V_{phase}/120V_{phase}, r_1 =r_2 =0.004 Pu, x1 = x2 = 0.08 Pu
5. DC link capacitor: C_{fdc}= 200 mF
6. Sensitive loads
   Linear load: R_L =10.78 V, X_L =0.808 V.
   Non-linear load: R_{Ldc}=15V, C_{Ldc}=2000mF.
7. RC-AC filter: R_{fac}=1V,C_{fac}=50 mF