Single Stage Switched Capacitor Based Multilevel Inverter for Photovoltaic Application

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Abstract: A two-stage switched-capacitor based multilevel inverter possesses a drawback such that switches in the second stage (i.e. H-bridge) endure higher voltage stress. To resolve this problem, this letter proposes a single-stage switched-capacitor module (S^3CM) topology for cascaded multilevel inverter which ensures the peak inverse voltage across all switches within the dc source voltage. Nine voltage levels can be generated with only one dc source and two incorporated capacitors. Hence, the numbers of isolated dc sources are significantly reduced compared to cascaded H-bridge. In addition, voltage boosting gain of two is achieved. A comparative analysis against the recent topology reveals that the proposed S^3CM topology achieves switch count reduction. The operation of the proposed topology is validated through circuit analysis followed by experimental results of a single module (9level) prototype.

I. INTRODUCTION

Renewable energy technologies are clean sources of energy that have a much lower environmental impact than conventional energy technologies. Renewable energy will not run out ever. Other sources of energy are finite and will someday be depleted. Among the variable renewable energy sources solar energy has higher potential than other energy sources. Hence in this paper the photovoltaic system is used. Solar cells convert sunlight directly into electricity. They are made of semiconducting materials similar to those used in computer chips. When sunlight is absorbed by these materials, the solar energy knocks electrons loose from their atoms, allowing the electrons to flow through the material to produce electricity. This process of converting light (photons) to electricity (voltage) is called the photovoltaic (PV) effect .we use inverter now days to improve the DC power into AC power. The key function of the inverter is the switching frequency. To convert dc signal into an ac signal we require fast switching of DC signal giving us multiple levels. But it has more harmonic distortion to overcome that the cascaded H-bridge topology is used. Cascaded H-bridge (CHB) multilevel inverter (MLI) is ubiquitous in high-voltage applications due to its inherent modularity [1]. Alternatively, there are recent attempts to replace H-bridge by establishing module topologies [3]which is capable of generating more voltage levels with reduced switch count A two-stage switched-capacitor based multilevel inverter possesses a drawback such that switches in the second stage (i.e. H-bridge) endure higher voltage stress. To resolve this problem, this letter proposes a single-stage switched-capacitor module (S3CM) topology for cascaded multilevel inverter [3] which ensures the peak inverse voltage across all switches within the dc source voltage. There is a different type of topologies are introduced, they are SCM in is a two-stage topology consisting of a switched-capacitor circuit and an H-bridge .Switches in the H-bridge (second stage) have to withstand voltage twice of the input dc source. In case it is used for high-voltage applications, two series-connected switches are required to ensure the PIV of all switches do not exceed dc source voltage (Vdc). In this instance, each SCM is comprised of a diode and a total switch count of 15. The initiative of this work is to establish an alternative topology, termed as single-stage switched-capacitor module (S3CM) which resolved. While at the same time retaining all its benefits. The PIV of all switches in the proposed S3CM are within the dc source voltage, Vdc.

II.THREE LEVEL INVERTER

In three level inverter the pulses for the switches are given by using the PWM technique, the reference and carrier waveforms are compared with each other and generate pulses to the switches .In that the reference signal used as a sinusoidal signal and the carrier signal used as a repeating sequence. These signals are compared using relational operator if the sinusoidal signal amplitude is higher than the carrier the pulses were generated and it is given to the switches S1 and S2. In the next negative half cycle the reference signal is phase shifted to 180 degree and again compared with the carrier signal that generate pulses this pulses are given to the switches S3 and S4 then the load is connected between the H-bridge across this output the voltage measurement is connected this is connected to the output scope.

III.FIVE LEVEL INVERTER

We can cascade the two 3 level inverter, if we give the same voltage to the both inverter it will act as a 5 level inverter, the levels of the inverter is 2VDC ,VDC,0,-VDC,-2VDC. We can give the input by comparing the reference wave and the carrier wave .we can have the 28.42% of harmonic distortion, but according to the IEEE standard we must have harmonic distortion less than 5%.so to overcome this disadvantage we go for 7 level inverter.

IV.SEVEN LEVEL INVERTER

The basic H-Bridge cascaded topology and the operational waveforms. For obtaining a three level output a basic H-Bridge topology requires one DC source along with four MOSFET switches and one balancing capacitors. In-order to obtain consequent levels we need a same set of topology which increases the number of components needed which in turn creates design complexity and increases the cost and number of components used. It is also found that the maximum output voltage cannot exceed the sum of voltage of individual sources which becomes the major setback of this topology. Therefore in an application which requires high output voltage from low voltage level, it needs H-bridge module in addition or step-up transformers. To overcome this proposed configuration is employed**.** We can have the same setup according to the 5 level inverter but we must give the different voltages to the two three level inverter, the levels are **3VDC, 2VDC, VDC, 0,-VDC,-2VDC,-3VDC**

V.PROPOSED S^{3}CM TOPOLOGY

The proposed S3CM topology is able to generate up to nine voltage levels. It is constituted by twelve switches, two capacitors and only one dc source, as depicted in Fig. 1. The number of levels and output voltage can be further increased by cascading multiple (N) modules. It is worth emphasized that the PIV of all switches in the proposed S3CM topology are equivalent to Vdc, with the exception of two switches, i.e. S9 and S10 which blocks only half of the Vdc. With merely low voltage rating switches, it can accomplish output voltage up to twice Vdc. On that account, it does not require series-connected switches when a high-voltage application is considered. A comparative analysis among cascaded MLI with the proposed S3CM, the SCM topology. For fair comparison, voltage stress of all the switches in these topologies are kept within Vdc. Therefore, two series-connected switches must be considered for S5 and S7–S10 for the SCM topology

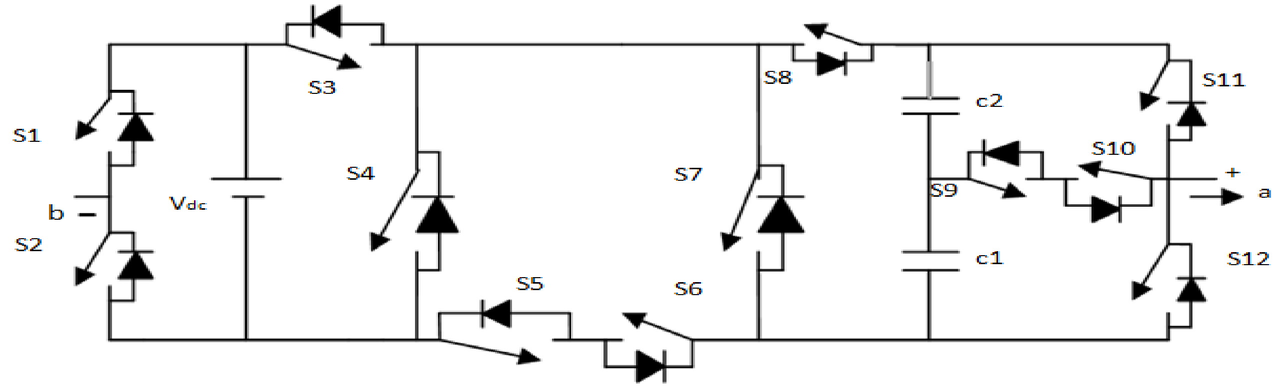

Figure .1 Circuit diagram of 9 level S^{3}CM topology

SWITCHING STATES:

states	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
1	0	1	1	0	1	1	0	1	0	1	0	1
2	0	1	1	0	1	1	0	1	1	1	0	0
3	0	1	1	0	1	1	0	1	1	0	1	0
4	0	1	1	0	1	0	1	0	1	1	0	0
5	0	1	1	0	1	0	1	0	1	0	1	0
6	1	0	1	0	1	1	0	1	1	0	1	0
7	1	0	1	0	1	1	0	1	1	1	0	0
8	1	0	1	0	1	1	0	1	0	1	0	1
9	1	0	0	1	0	1	0	1	0	1	0	1
10	1	0	0	1	0	1	0	1	1	1	0	0

Figure .2 Switching States of 9 level S^{3}CM topology

MODES OF OPERATION

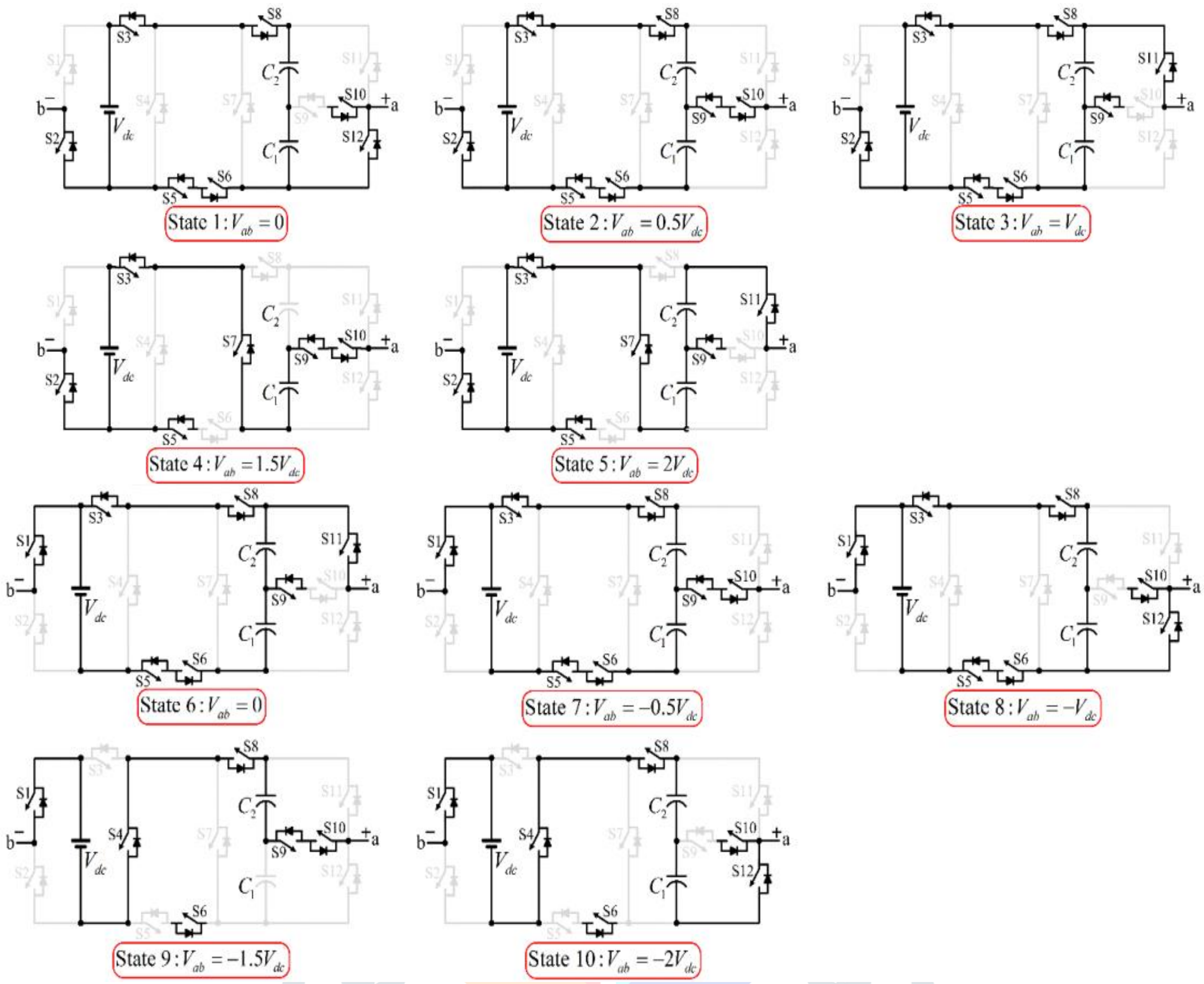

Figure.3. Modes of operation of S^{3}CM method

The figure.3 .shows the modes of operation of the proposed S^{3}CM we can have 10 states from 2 to -2 Vdc.

VI. SIMULATION RESULTS

VI.I THREE-LEVEL INVERER

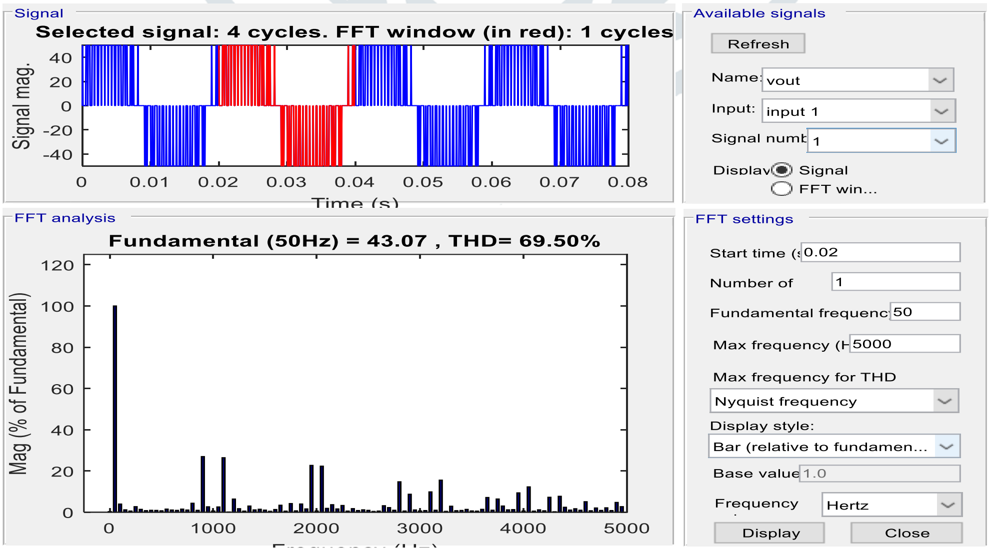

Figure.4.THD analysis of 3-level inverter

According to the IEEE standard the harmonics must be less than 5% but we have 69.52% for overcome this we can go for five level inverter

VI.II FIVE LEVEL INVERTER:-

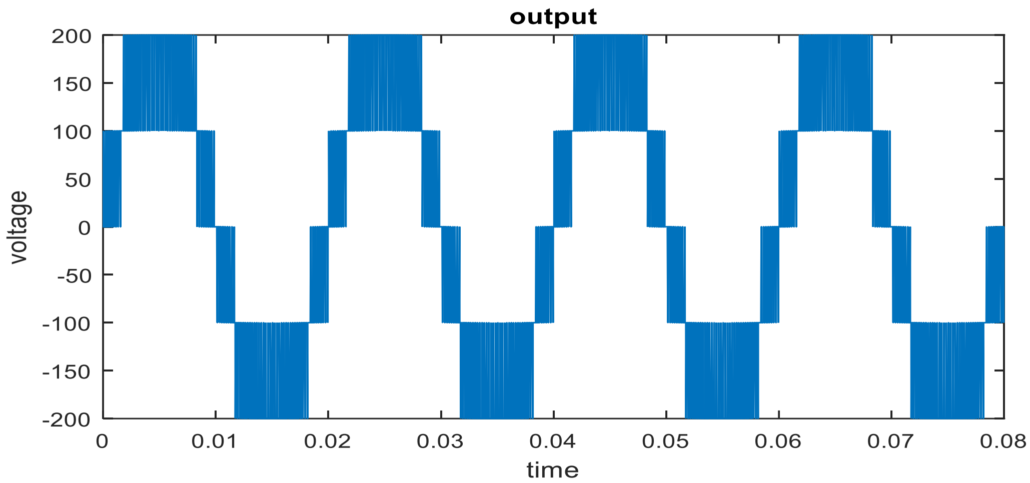

Figure.5.Output waveform

The figure.5 shows the output waveform of the five level inverter we have five levels from 2Vdc to -2Vdc.in x-axis we have time and in y-axis we have voltage

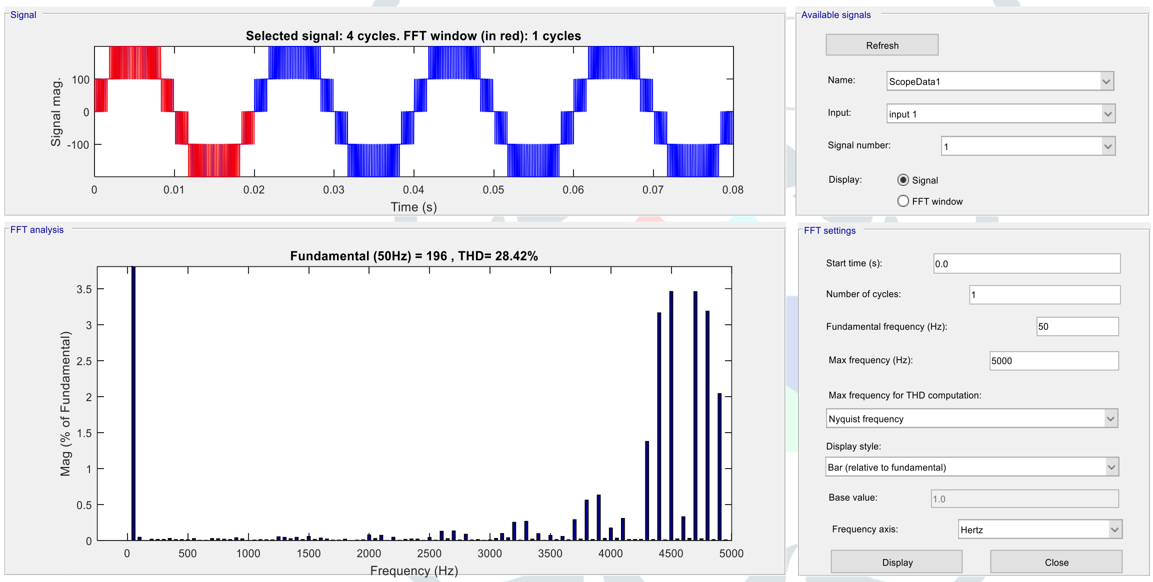

Figure.6.THD analysis

According to the IEEE standard the harmonics must be less than 5% but we have 28.39% for overcome this we can go for seven level inverter

VI.III SEVEN LEVEL INVERTER

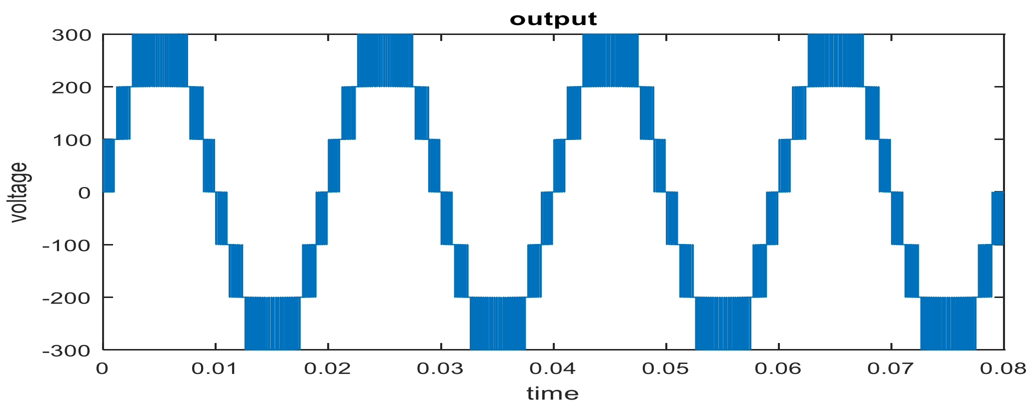

Figure.7.Output waveform

The figure.7 shows the output waveform of the five level inverter we have five levels from 3Vdc to -3Vdc.in x-axis we have time and in y-axis we have voltage

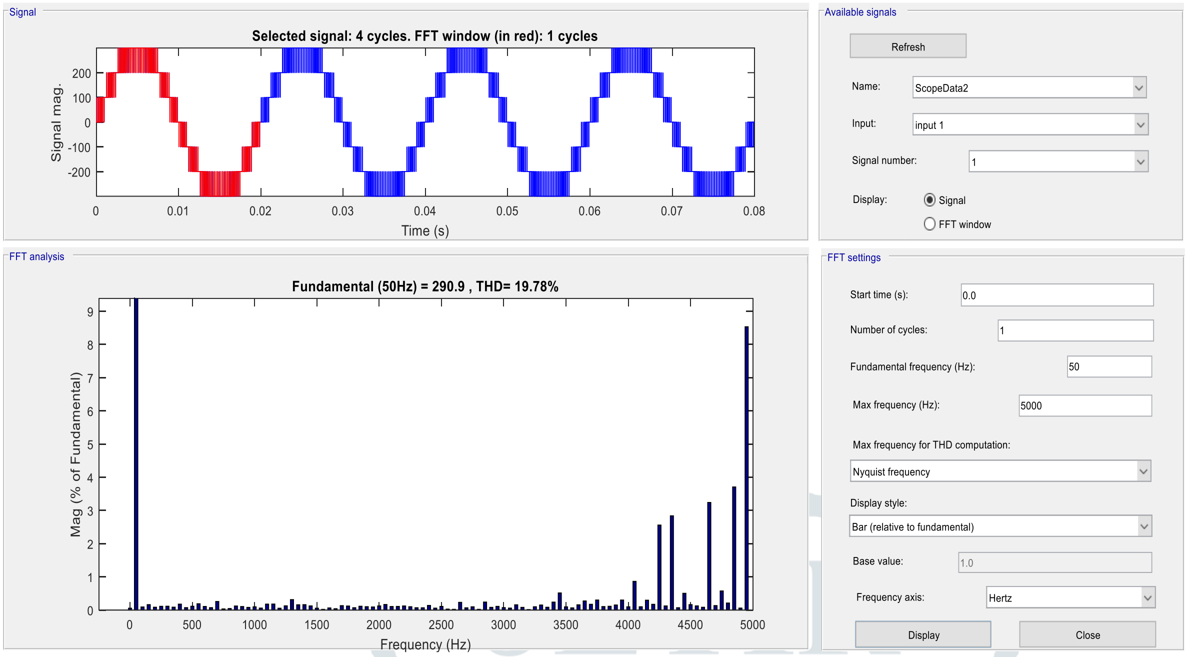

Figure.8.THD analysis

According to the IEEE standard the harmonics must be less than 5% but we have 18.78% for overcome this we can go for nine level inverter

VI.IV PROPOSED S^{3}CM TOPOLOGY

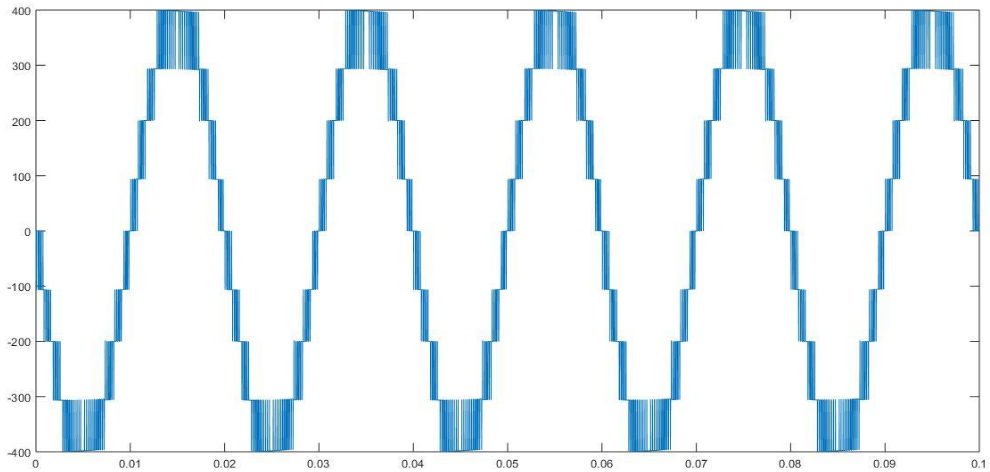

Figure.9.Output waveform

The figure.9 shows the output waveform of the nine level inverter we have five levels from 4Vdc to -4Vdc.in x-axis we have time and in y-axis we have voltage

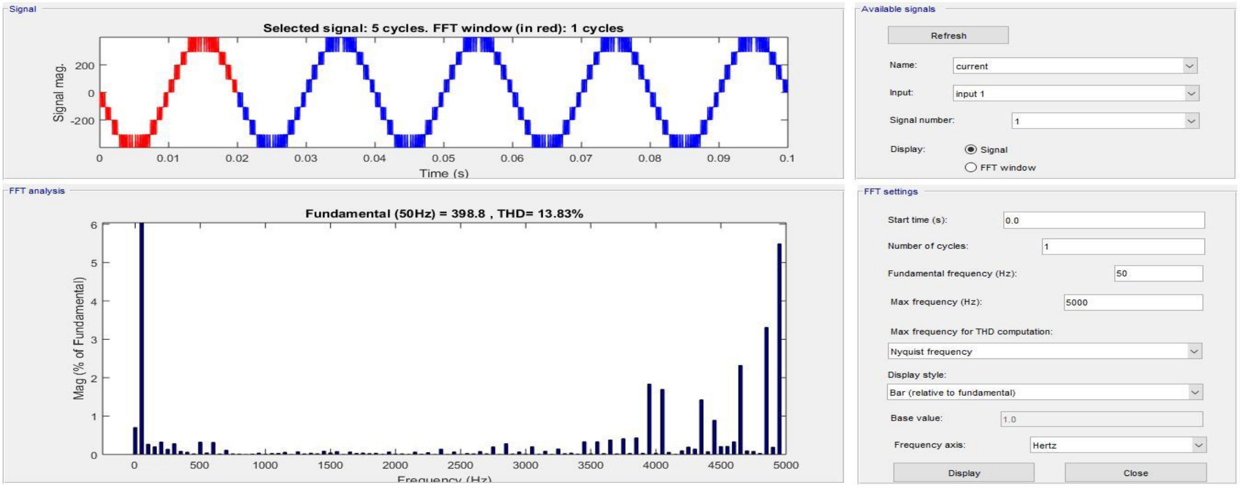

Figure.10.THD analysis

According to the IEEE standard the harmonics must be less than 5% but we have 13.83% in nine level inverter if the input is Vdc ,the output is 2Vdc.

VII CONCLUSION

In this paper, a 9-level inverter module based on single-stage switched-capacitor circuit is established for cascaded MLI. The proposed S3CM topology requires only single dc source with a voltage boosting gain of two. Circuit analysis demonstrated that the voltage stress across all switches is within the dc source voltage. Therefore, it is capable of generating more levels and higher voltages up to twice the dc source by using switches with low voltage rating. Comparative analysis against the recent topology and the H-bridge for cascaded MLI validates its merits of reduced switch count as well as reduced dc source count. The performances of the proposed topology are convincingly validated, with all the results are in good agreement with theoretical analysis. The improvements of the proposed S^3CM topology made it an attractive alternative for high-voltage dc-ac power conversion systems.of all these algorithms can be evaluated in the over modulation zone. Analytical evaluation of harmonic distortion for multilevel inverters can also be carried out. More SVPWM based techniques can be developed for inverter switching at much higher frequencies and hardware implementation can also be done. All the proposed algorithms in this thesis are for time-invariant systems. Therefore, it is recommended to eliminate harmonics for time-variant systems. Further to reduce the switching losses of the inverters, discontinuous pulse width modulation algorithms have to be proposed.

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