Low-Power and Area-Efficient Shift Register Using Pulsed Latches

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Abstract - *This paper covers a range of issues in the design of pulsed latches for low-power applications. First it revisits, extends, and improves the power and delay-performance optimization methodology, attempting to make it more formal and comprehensive. The shift registers with pulsed latches has been proposed for the minimization of delay and the excess leakage in the power. The power dissipation of the clock distribution is taken into account, supported by simulations for multi-bit data path registers. Synchronous logic design is the dominant main stream integrated circuit design methodology. Latches are an inherent building block in any synchronous design. Furthermore flip-flops constitute most of the load on the clock distribution and power networks, which are the main power consuming networks of a synchronous integrated circuit. This could be designed by the conventional latches and the SSASPL based latches for the implementation of the power consumption*

Keyword: Area efficient,Flip flop ,pulsed clock, pulsed latch and shift register

1.INTRODUCTION

➢ **A** shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 16 – mega pixel CMOS image sensor uses 45kbit shift registers.

As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption

The main objective of this project is to reduce the delay and the power in the latches instead of flip flops by using a pulsed clock signals circuit for high memory applications .The shift register solves the problem using the multiple non-overlap delay pulsed clock signal

The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Recently, many methodologies have been introduced for reducing dynamic power for systems-on-chip (SoCs). These methodologies, however, impose restrictive physical constraints which have schedule impact or which are heavily dependent on logic functions such as clock gating.

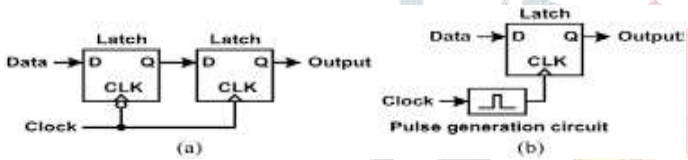
The rest of the paper is organized as follows: Section II describes the architecture of the proposed shift register. Section III presents the measurement results of the fabricated chip. Finally, conclusions are drawn in Section IV.

➢ Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers of transistors into the same size. The more transistors there will be more switching and more power dissipated in the form of heat .

- Though several contributions have been made to the art of single edge triggered flip-flops, a need evidently occurs for a design that further improves the performance of single edge triggered flipflops patterns. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flipflop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flipflop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

2.ARCHITECTURE:

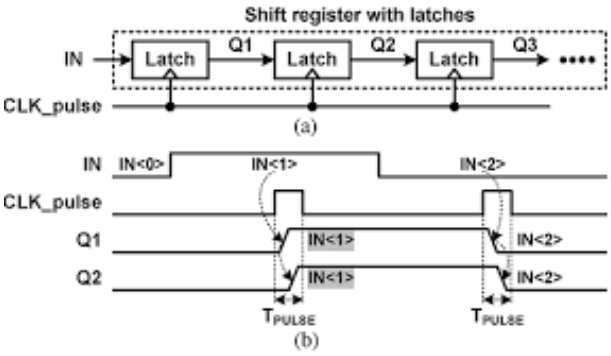
1.1(i)Proposed shift register:



(Fig1.a)Master slave flip flop b.pulsed latch

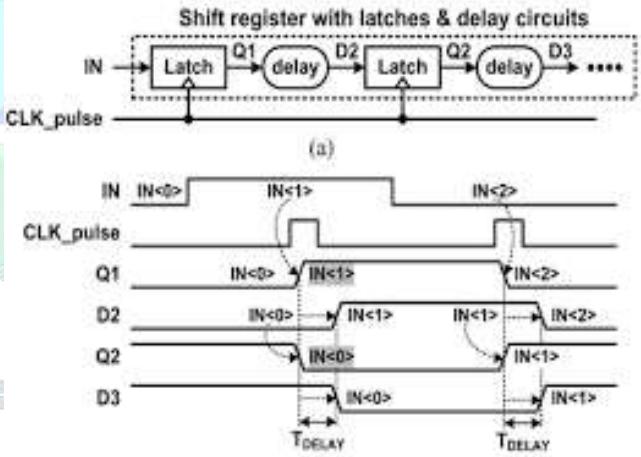
master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b)[6]. All pulsed latches share the pulse generation circuit
for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift register in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.



(Fig2.a) Shift register with latches and a pulsed clock signal (b) waveform

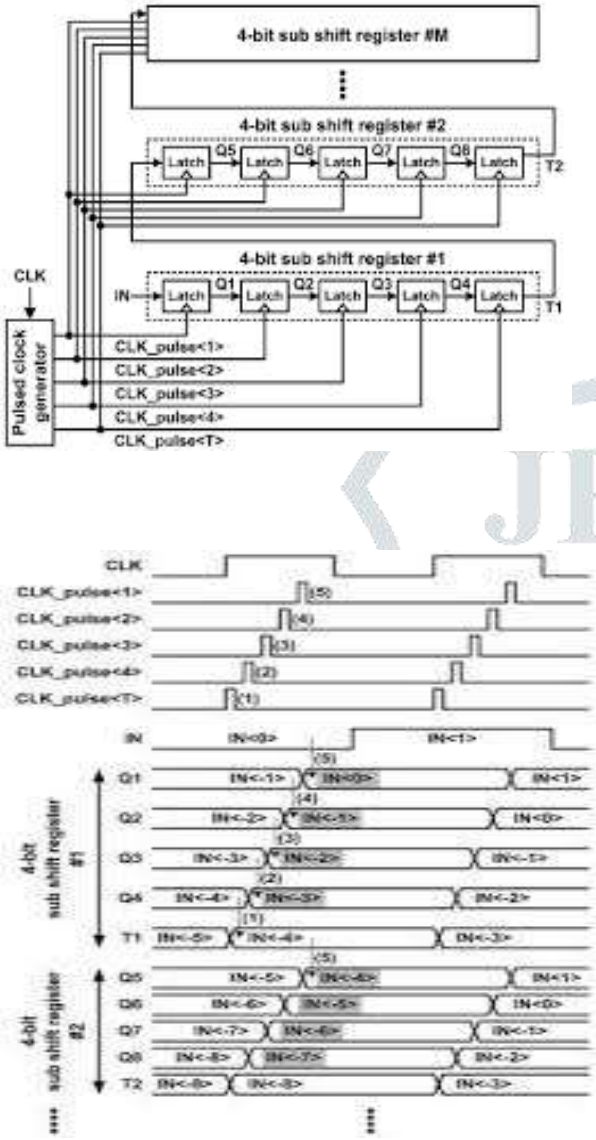
As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. However,the delay circuit cause large area and power overheads.



(Fig3.a) Shift register with latches, delay circuits, and a pulsed clock signal (fig.b) waveforms

Fig. 4(a) shows an example the proposed shift register. The proposed shift register is divided into M sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse⟨1:4⟩ and CLK_pulse⟨T⟩). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift

register #2. Fig. 4(b) shows the operation waveforms in the proposed shift register. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator.



Fig(4.a) Proposed shift register

. (a) Schematic. (b) Waveforms

The sequence of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal CLK_pulse⟨T⟩ updates the latch data T1 from Q4. And then, the pulsed clock signals CLK_pulse⟨1:4⟩ update the four latch data from Q4 to Q1sequentially. The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register. The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches.

In Fig. 5 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals

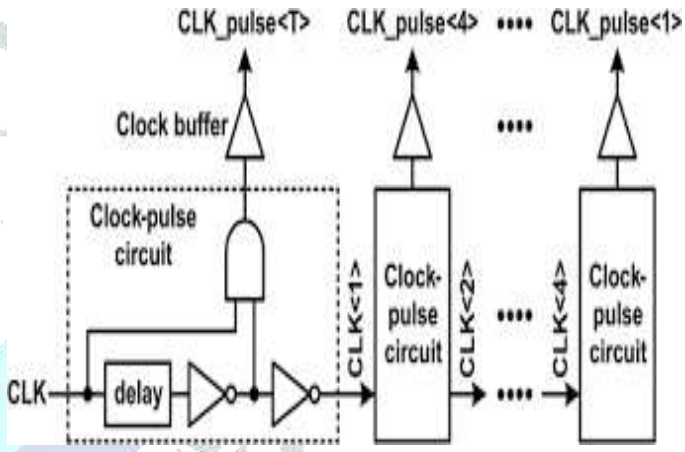


Fig.5 Delay pulsed clock

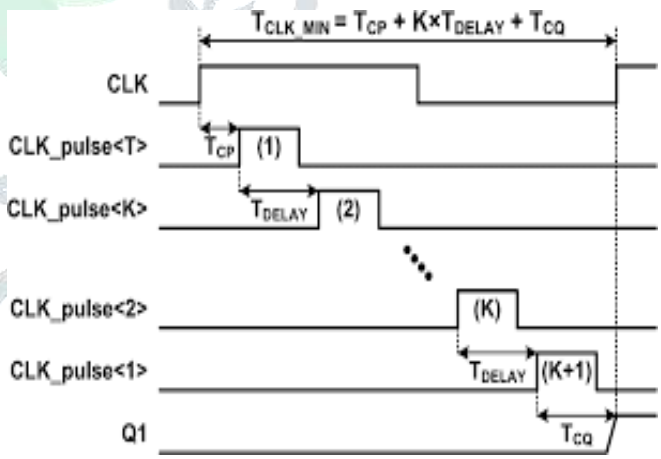


Fig.6Mininmum clock cycle of proposed shift register

The numbers of latches and clock-pulse circuits change accoding to the word length of the sub shift register K . K is selected by considering the area, power consumption, speed. The area optimization can be performed as follows.

As shown in Fig. 6 the minimum clock cycle (Tclk-Min) is Tcp+k*Tdelay+Tcq,where Tcp is the delay from the rising edge of the main clock signal (CLK) to the rising edge of the first pulsed clock signal (CLK_pulse⟨T⟩), tdalay is the delay of two neighbor pulsed clock signals, tcq is the delay from the rising edge of the last pulsed clock signal (CLK_pulse⟨1⟩) to the output signal of the latch Q1. Therefore K must be selected under the maximum number which is determined by the maximum clock frequency of the target application.

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flops. Therefore, the area and power consumption
are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flipflops to reduce the area and power consumption. In chipimplimentation the SSASPL (static differential sense amp shared
pulse latch) in Fig. 7, which is the smallest latch, is selected. The original SSASPL with 9 transistors [6] is modified to the SSASPL with 7 transistors in Fig. 8 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal

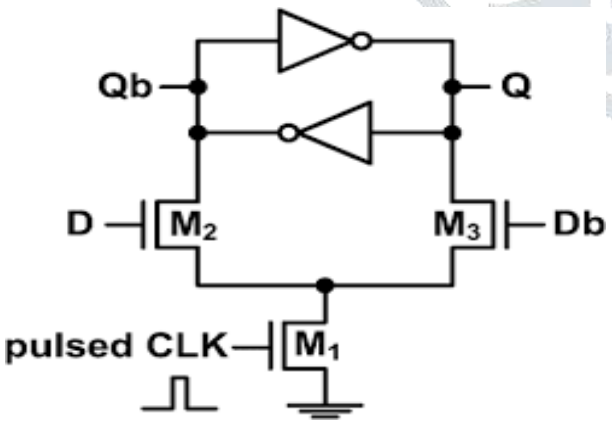


Fig 7. Schematic of the SSASPL

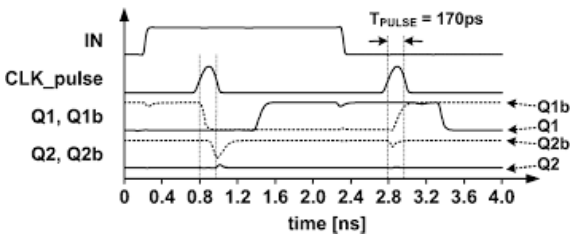


Fig.8Simulation waveforms of a shift register with pulsed latches

The SSASPL updates the data with three NMOS transistors (M1-M3)and it holds the data with four transistors in two cross-coupled inverters. It requires two differential data inputs (D and Db) and a pulsed clock signal. When the pulsed clock signal is high, its data is updated. The node Q or Qb is pulled down to ground according to the input data (D and Db). The pull-down current of the NMOS transistors (M1-M3)must be larger than the pull-up current of the PMOS transistors in the INVERTER.

The SSASPL was implemented and simulated with a 0.18 µM CMOS process at . VDD=1.8V The sizes (W/L) of the three NMOS transistor (M1-M3) are 1µm/0.18µm.the CMOS process at . The sizes (W/L) of the are all 0.5µm/0.18µm . The minimum clock pulse width of the SSASPL to update the data is 62 ps at a typical process simulation (TT) and 54–76 ps at all process corner simulations (FF-SS). The rising and falling times of the clock pulse are approximate 100ps. The clock pulse shape can be degraded due to the wire delay, signal coupling, supply noise. The clock pulse width of 170 ps was selected by adding the timing margin to the minimum clock pulse width at the slowest simulation case.

3.SCHEMATC DAIGRAMs DESIGN IN TANNER SOFTWARE:

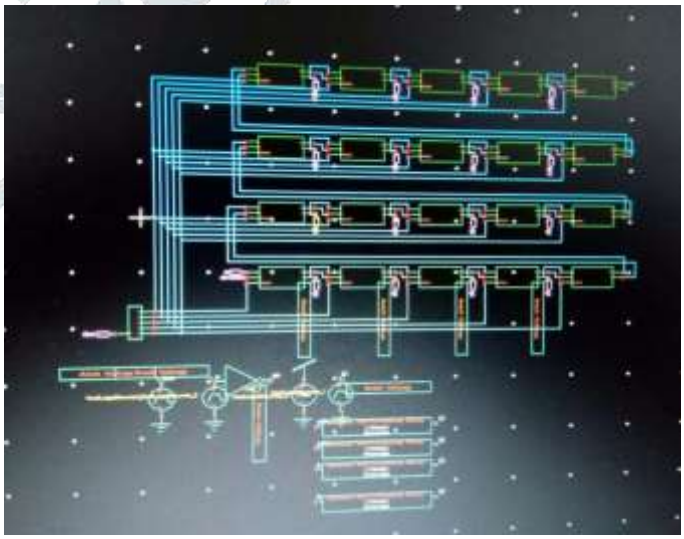


Fig: DESIGN OF PROPOSED SHIFT REGISTER USING LATCHES

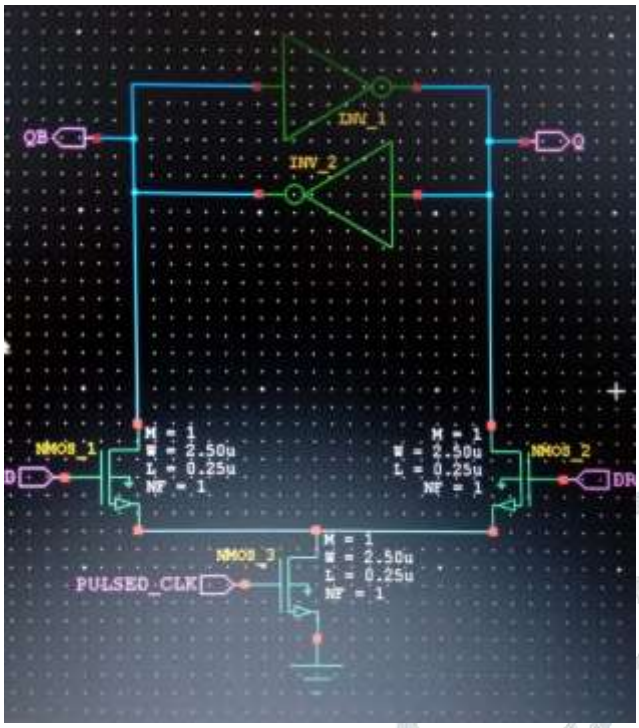


FIG: DESIGN OF SSASPL LATCH

Area optimization: The area optimization can be perform as follows when the circuit areas are normalized with a latch the areas of the latch clock pulsed circuit are 1 and respectively .the total area becomes(αA×(k+1)+N+(1+1/k) .the optimal ($k=\frac{\sqrt{N}}{\alpha a}$) for the minimum area is obtained from th first order differential equation.

Power optimization: The power optimization is similar area optimization the power is consumed mainly in latches and clocked and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and clock circuit

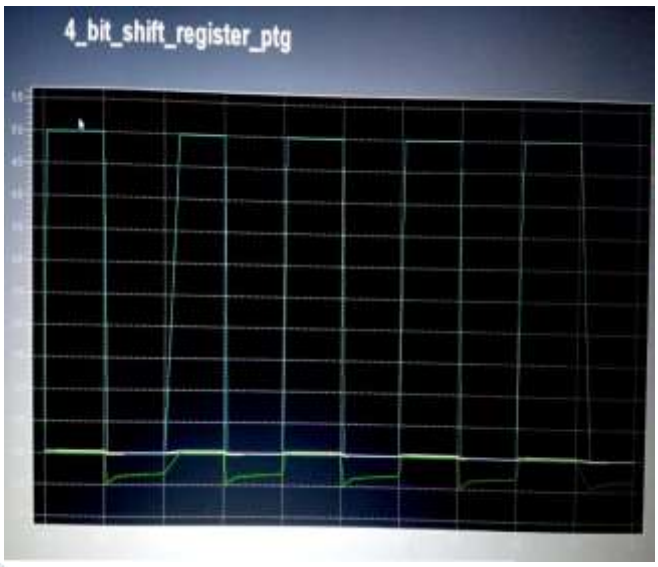


FIG:SIMULATION RESULT

TIMING REPORT:

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* BEGIN NON-GRAPHICAL DATA

Power Results
vdd gnd from time 5e-008 to 1e-008
Average power consumed -> 1.064704e-004 watts
Max power 1.064704e-004 at time 5e-008
Min power 1.064703e-004 at time 1e-008

* END NON-GRAPHICAL DATA

* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

TRAN_Measure_Delay_1 = 5.2500e-008

TRAN_Measure_Delay_2 = 5.2500e-008

TRAN_Measure_Delay_3 = 5.2500e-008

TRAN_Measure_Delay_4 = 5.2500e-008

* END NON-GRAPHICAL DATA
*

* Parsing                          0.06 seconds
* Setup                            0.50 seconds
* DC operating point               0.03 seconds
* Transient Analysis               1.38 seconds
* Overhead                         7.09 seconds
* ---------------------------------------------
* Total                            9.06 seconds

* Simulation completed

* End of T-Spice output file
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Future scope:

SRAM is a type of semiconductor memory which is volatile in nature it performs both read and write operation to store and fetch the data based on the particular address The read and write operations are controlled by the word line. Based on the bit line condition the data in it is stored and consists of a 1bit latch to store the data.

CONCLUSIONS:

This paper proposed a low power and area efficient shift register using pulsed latches the shift register reduces area and power consumption by substituting flip flop with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals as an alternative of a single pulsed clock signal.

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BIOGRAPHIES :

Prof .Dr.Syeda Gauhar Fatima is working as a professor in Dept.of E.C.E,Deccan collegeof engineering and Technology with a teaching experience of 19 years.she has an esteem academic performance in teaching/lecturing in almost all the aspects of analog and digital electronics and communication subjects.she has 34 publications titled to her name with also being coordinator to several technical workshops and has guided several UG level major projects

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