

A Novel Approach for Design of 8-Bit Adder-Subtractor and Comparator Using MGDI Technique

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Abstract: low power efficient digital devices are target of researchers in recent years. This paper proposes the design of a low power high speed, energy efficient full adder, full subtractor, 2 bit comparator using MGDI technique the entire design has been performed in technology the n these digital circuits were compared with traditional CMOS transistors in terms of power dissipation , number of transistors, area ,speed, and delay .the simulation of the proposed design has been carried out in DSCH2 and the layout has been designed in micro wind

Index Terms – GDI CELL, MGDI CELL, Adder-Subtractor, Comparator, Power consumption.

I. INTRODUCTION

In modern time ,three factors-area ,speed ,power consumption are essential for increasing demand of low power and small size in handheld devices like cellular phone ,laptop etc...in past years ,VLSI designers were interested with parameters such as area , speed , reliability and cost. in recent years ,power consumption being set equivalent importance. it has been proved that an increase of 10°c in working temperature of an electronic device causes a 100% increase in the failure rate. Using Traditional CMOS Technology the design of Adder-Subtractor and comparator requires more number of transistors, occupies large area and increase power dissipation. By using MGDI technology for the design of Adder-Subtractor and Comparator reduces the area power dissipation and the transistor count

The current paper is organized into 5 sections. Section 1 gives Introduction. Section 2 gives Description of GDI Technique .Section 3 gives Description of MGDI Technique. Section 4 gives brief Literature Survey. Section 5 gives Design of Adder-Subtractor circuit using MGDI Technique. Section 6 gives Design of 2-bit Comparator using MGDI Technique. Finally the paper is concluded with Section 7.

2. GDI TECHNIQUE

In appearance GDI cell looks similar to CMOS inverter but GDI cell consists of 3 inputs – G (common gate input of PMOS and NMOS), P (input to drain/source of PMOS) and N (input to drain / source of NMOS). Substrates of both PMOS and NMOS are attached to their diffusion P, N to reduce Bulk effect.GDI cell is shown in figure below

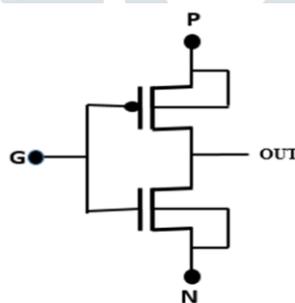


Fig-1: Basic GDI cell

3. MGDI TECHNIQUE

MGDI is a new technique for designing low power digital circuits. This technique is adopted from GDI technique. MGDI technique is used to reduce power dissipation, transistor count and area of digital circuits. MGDI also consists of three input terminals –G, (input of both PMOS and NMOS) P, (input to drain/source of PMOS) and N (input to drain/source of NMOS) except the bulks of PMOS (S_P) and NMOS (S_N) are constantly coupled to V_{dd} and GND, respectively. MGDI cell is shown in figure below.

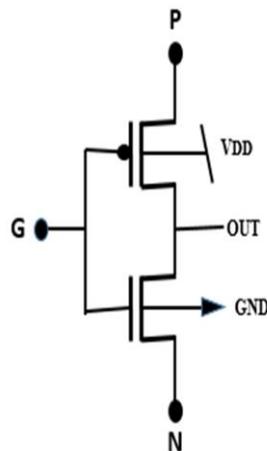


Fig:-2 Basic MGDI cell

The main purpose of using MGDI cell instead of basic CMOS design is to overcome the problems that we are facing in the CMOS design. This arrangement of Mod-GDI cell provides considerable reduction in the gate leakage power compared to static CMOS gate.

4. LITERATURE SURVEY

- Modified-GDI is introduced, earlier GDI can be fabricated only in twin well CMOS process or SOI process to realize a chip, this increases the complexity as well as the cost of fabrication. But MGDI can be fabricated in any standard CMOS fabrication process.
- In the proposed paper the adder circuits is designed in Self resetting logic and the number of transistors in the modified design is reduced. The goal is to obtain a family of adders that could simplify the implementation of fast processing circuit which overcomes the restriction due to the pulses being elongated and shortened as signal traverse the logic stages. The circuits are designed in 120nm processing CMOS processing technology.
- Based on mixed topology full adder based on mixed GDI has been designed. Here GDI full adders are followed by inverters in the long full adder chains to alleviate the problem of signal degradation during propagation through long chain.
- Three low power full adders are designed with full swing AND, OR and XOR gates to alleviate threshold voltage problem which is commonly encountered in Gate Diffusion Input (GDI) logic. The enhanced driving capability also facilitates lower voltage and faster operation which leads to less energy consumption. The performance of the proposed designs is compared with the other full adder designs, namely CMOS, CPL, etc...

5. EXISTING DESIGN OF ADDER-SUBTRACTOR

Adder is a combinational circuit which adds two binary numbers and generate sum and carry as output, whereas subtractor performs the addition of first binary number with 2's complement of second number [40-42]. Figure 1 shows the Block diagram and design of full adder and subtractor circuit using conventional logic gates.

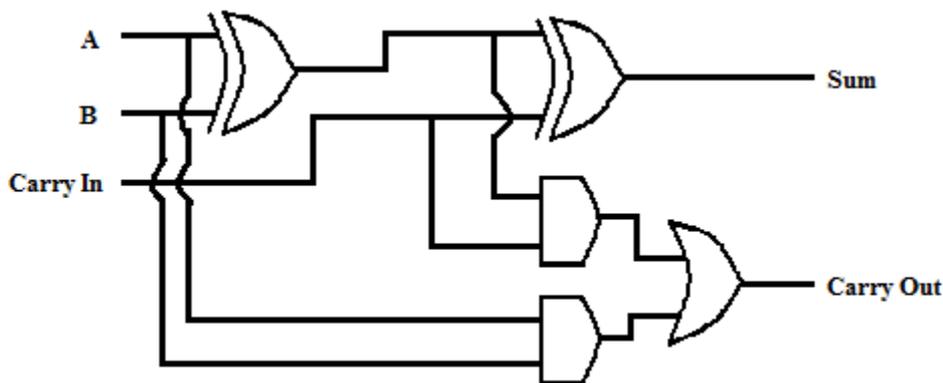
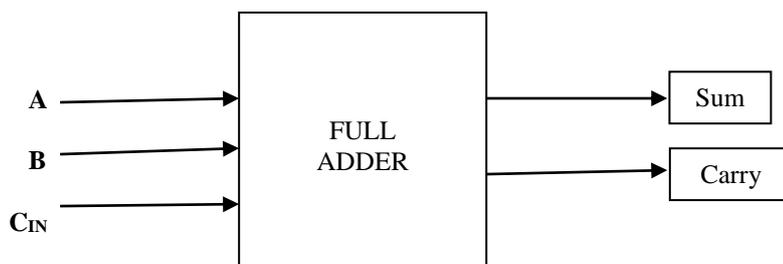


Fig: - Block diagram and Design of Adder-Subtractor using basic Logic gates

The existing design of an 8-bit adder-subtractor circuit is designed by cascading eight full adder circuits and eight exclusive OR gates as shown in figure 2 below. Here exclusive OR gates are connected to full adders to make these work as subtractor circuit with 2's complement method.

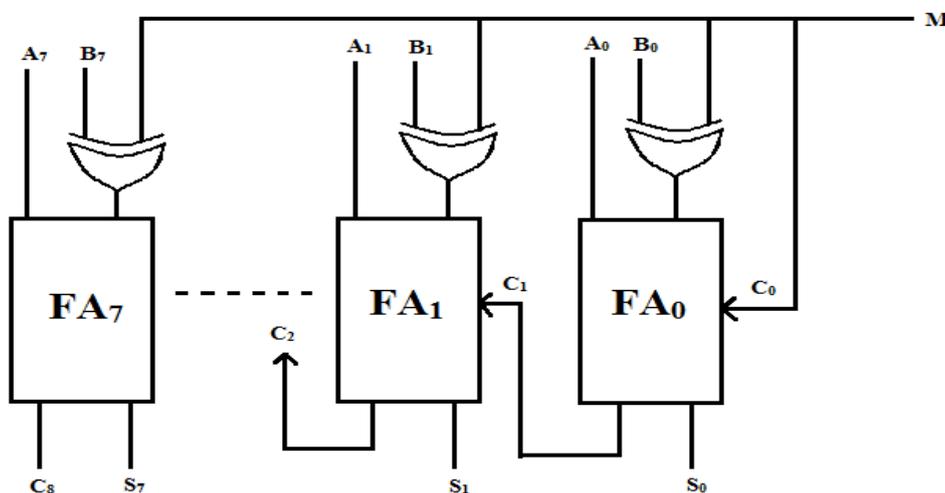


Fig: - A Basic CMOS 8-bit Adder - Subtractor circuit

Here mode bit M derives the working of the circuit as adder or subtractor. When M=0, the digital circuit works as adder add two eight bit binary numbers A(A₇ A₆ A₅ A₄ A₃ A₂ A₁ A₀) and B(B₇ B₆ B₅ B₄ B₃ B₂ B₁ B₀) to give desired sum (C S₇ S₆ S₅ S₄ S₃ S₂ S₁ S₀). Whereas, for M=1, the circuit works as subtractor as full adder circuits will add number A with 2's complement of number B. To design this 8-bit adder subtractor circuit using conventional approach we use AND, OR and XOR gates.

5. PROPOSED DESIGN OF ADDER-SUBTRACTOR USING MGDI TECHNIQUE

In the proposed method we are designing an 8-bit Adder-Subtractor using MGDI Technique .A 1-bit Adder is designed With 8 transistors using MGDI cell as shown in figure. This will reduce the transistor count when compared to CMOS design. The design of 8Transistor Adder is shown below.

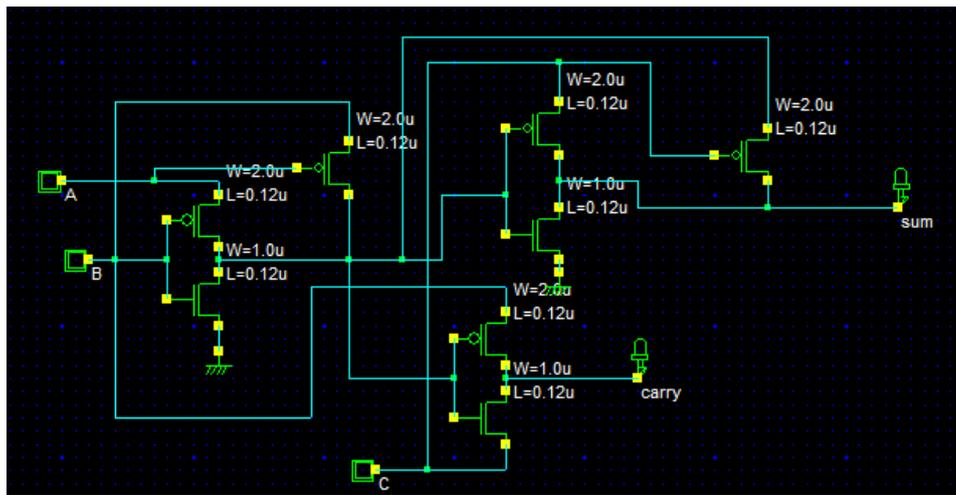


Fig: - Design of 1-bit 8T Adder

The 8-bit Adder-Subtractor circuit using MGDI cell has been designed and the block diagram is shown below

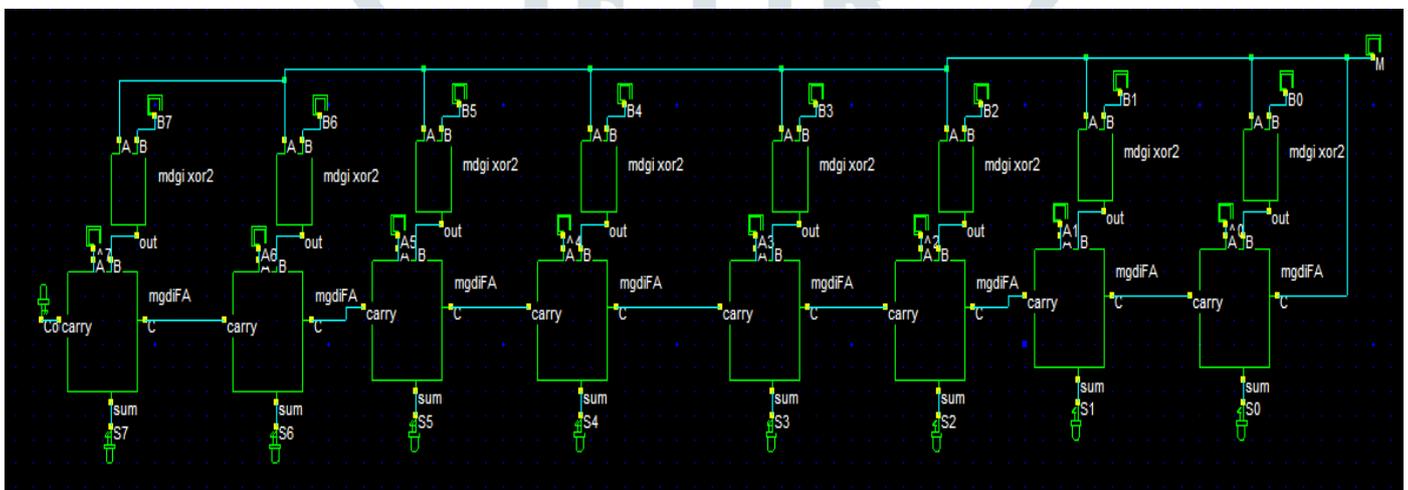
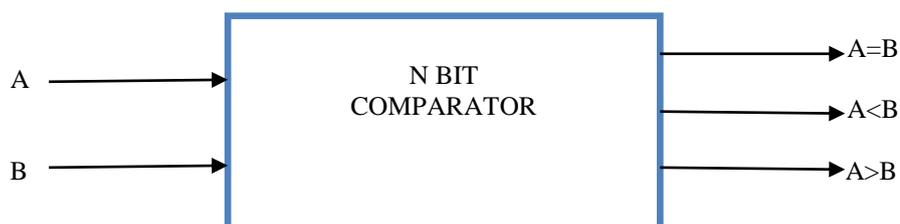


Fig: - Design of 8-bit Adder-Subtractor circuit using MGDI cell

6. EXISTING DESIGN OF A COMPARATOR

The magnitude comparator is a fundamental arithmetic component of digital system. A magnitude comparator is used in Digital Signal Processors (DSP) for data processing, microprocessor for decoding instruction and microcontroller for controlling temperature of furnace in industry. Comparator is a combinational circuit, N bit comparator compares two N bit binary numbers A and B. The block diagram of N bit comparator is follows in fig. It generates three outputs that is denoted by $A=B$ (F_1), $A<B$ (F_2), $A>B$ (F_3).



The design of CMOS 2-bit Comparator is shown below :

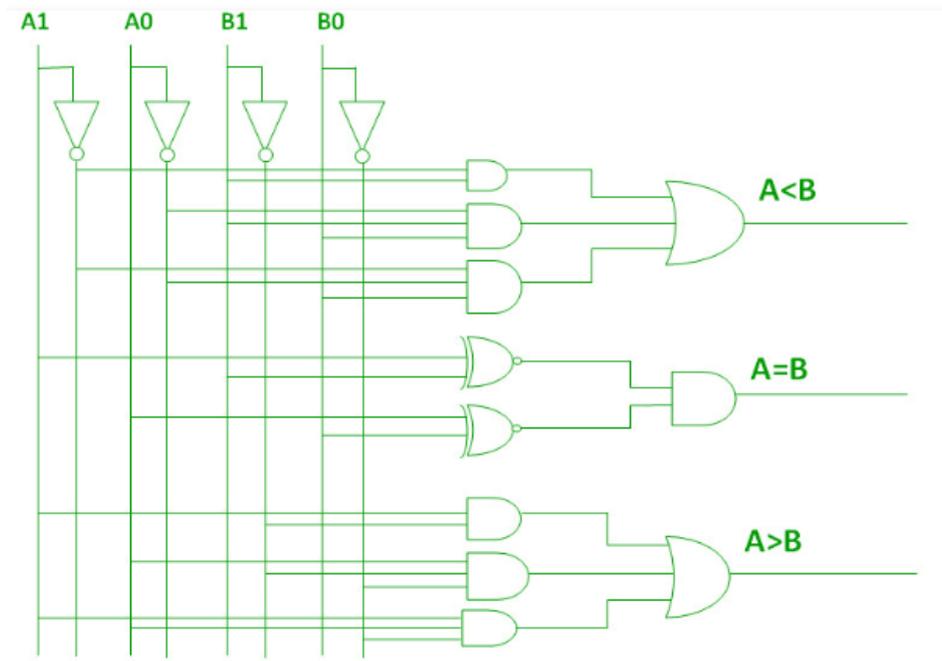


Fig: - 2-bit CMOS Comparator

PROPOSED DESIGN OF 2-BIT COMPARATOR

In this proposed design the 2-bit comparator is designed using MGDI technique which will reduce the transistor count and the power consumption. A transistor level design for 2-bit comparator using MGDI technique is shown below

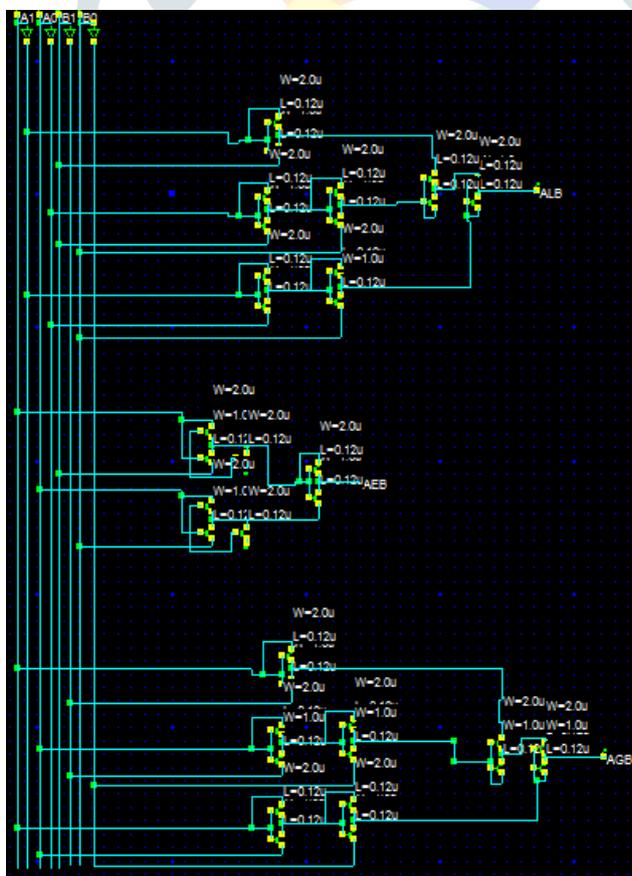


Fig: - 2-bit comparator using MGDI technique

COMPARISON TABLE

SL.NO	TECHNOLOGY	POWER CONSUMPTION	TRANSISTOR COUNT(1bit)	AREA
1	CMOS TECHNOLOGY	0.407mw	58	Width =129um Height = 20um
2	MGDI TECHNOLOGY	0.219mw	8	Width =120um Height = 20um

Fig: - Comparison between CMOS 16-bit Adder- Subtractor and MGDI 16-bit Adder-Subtractor

SL.NO	TECHNOLOGY	POWER CONSUMPTION	TRANSISTOR COUNT(1bit)	AREA
1	CMOS TECHNOLOGY	54.66uw	19	Width =111um Height = 14um
2	MGDI TECHNOLOGY	39.445uw	10	Width = 78um Height = 16um

Fig: - Comparison between CMOS 2-bit Comparator and MGDI 2-bit Comparator

SCHEMATIC DIAGRAMS

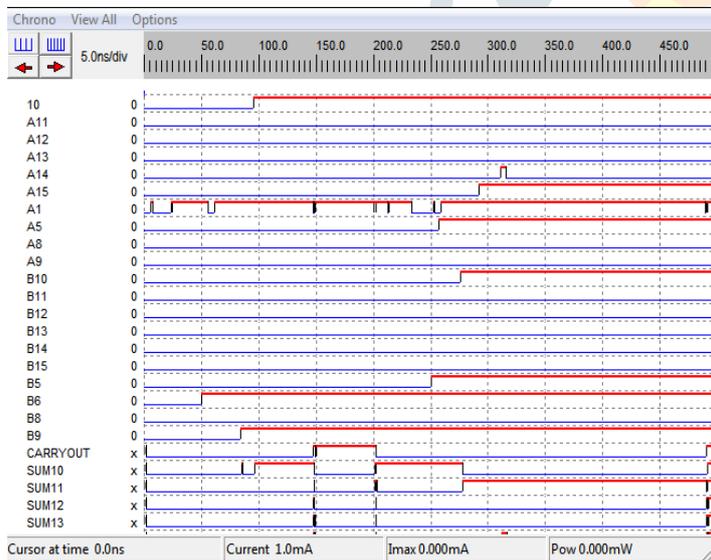


Fig: - schematic of 16-bit Adder- Subtractor using MGDI

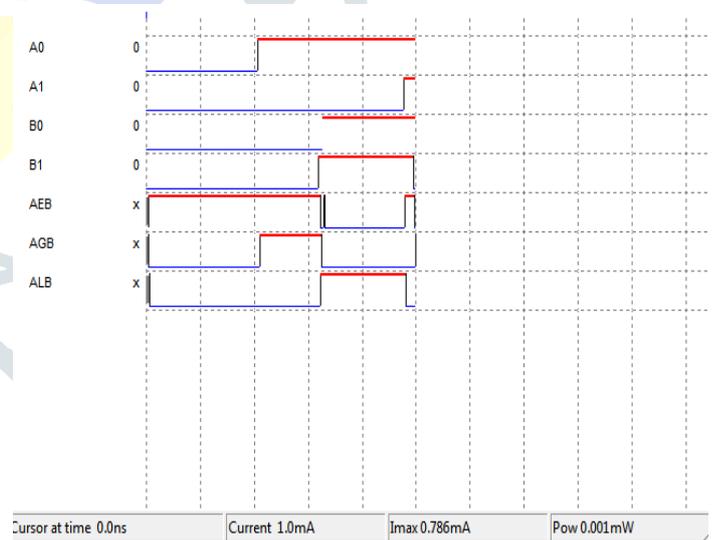


fig: - Schematic of 2-bit comparator using MGDI

CONCLUSION

Based on the work it can be concluded that Modified gate diffusion input technique is considerable while designing low power device.

- As the most basic principle of designing low power is to lessen the transistor count so more transistor can be accommodated in smaller area and as a result the devices which are designed will be more portable. In most of the case it has been observed that MGDI reduces the transistor count to a considerable amount.

- Another factor which effects the low power device is power dissipation which depends on the switching activity, the node capacitance and leakage current . MGDI in most of the cases dissipates less power as compared to another technique.
- Delay is another parameter which depends on the number of transistor in series transistor sizes and inter cell wiring and it is also improved when MGDI technique is used. Hence it can be concluded that MGDI is an appropriate choice while designing low power devices

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