Power Optimization Of Linear Feedback Shift Register(LFSR) For Low Power BIST

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***Abstract*— This paper proposes a low power Linear Feedback Shift Register (LFSR) for Test Pattern Generation (TPG) technique with reducing power dissipation during testing. The correlations between the consecutive patterns are higher during normal mode than during testing. The proposed approach uses the concept of reducing the transitions in the test pattern generated by conventional LFSR. The transition is reduced by increasing the correlation between the successive bits. The simulation result show that the interrupt controller benchmark circuit's testing power is reduced by 46%with respect to the power consumed during the testing carried by conventional LFSR.**

***Keywords*— LFSR, LT-LFSR, BIST , Conventional, Testing,**

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation for VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. Hence it is important aspect to optimize power during testing. **Power optimization** is one of the main challenges.

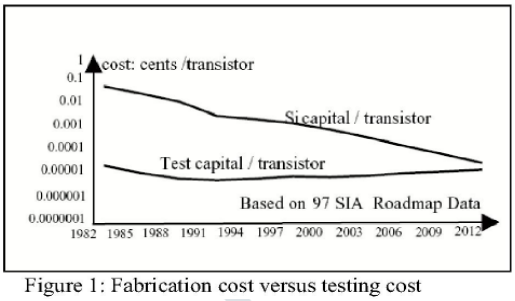

Figure 1: Fabrication cost versus testing cost

This report addresses the problem of testing digital logic circuits. System-On-Chip (SOC) Integrated Circuits (IC's) are designed and manufactured to meet application specific functional requirements. Some examples of applications are camera-on-a-chip, MP3 player, etc. These functional requirements often need to be balanced with the desired IC performance, maximum allowable power consumption and overall packaged and tested IC cost.

II. SOC BACKGROUND

SOC's typically integrate multiple Microprocessors, various types of memories such as SRAM, ROM, Flash, user defined logic, etc. Most SOC's are heavily populated with multiple instances of memory. Also included can be IP macros such as Digital Signal Processors, Analog to digital converters, etc...

Power consumption of the device normally includes power consumed by the core of the chip plus power consumed by the I/O's13. Most SOC die are packaged in multiple substrate packages.

Estimating the IC power budget involves maintaining perspective of several technical and business factors such as process technology, cell design libraries, pin-out and package constraints, logic and IP macro clock domains, cost and time pressures, etc.

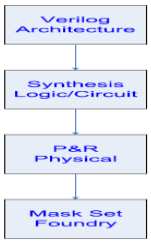

FIG 2 IC

METHODOLOGY

On the other hand EDA tool developers have kept up with their pace on developing advanced tools linking Design for Test and Design for Manufacturing. More than a decade old concept of Design for Test has been extended to Design for Manufacturing.

User-defined Logic is commonly verified using an FPGA before integrating it on the chip. Again it is incumbent upon the SOC design team to include logic for test on the chip to test user defined logic along with the other blocks of the chip.

. SOC suppliers can choose to test the IC at the package level and ignore tests at the wafer and/or die level. This is primarily done to save costs. (SOC cost is the sum of the die, package and test/assembly cost).

III. SOC TEST

As noted in chapter 2 it is imperative to verify the functional and manufacturing viability of the individual IP components before integrating them into the SOC design.

SOC testing is best viewed as an iterative process comprised of a series of tests. Figure 2 shows a test methodology. Either flat or hierarchical approach can be used depending on the complexity of the device. As the complexity of the device increases it is often recommended to test individual components using Scan and/or BIST as opposed to testing the entire design using a flat approach.

Test Approaches are External ATE, Conventional DFT and Embedded test is a natural evolution of the two distinct approaches discussed thus far namely external ATE and DFT. External ATE approach requires a mix of very expensive low/high speed testers with varying bandwidth. One of the key benefits of the embedded test is in the on-chip test data generation which reduces the volume of external patterns and can be customized per the IP block type in the SOC.

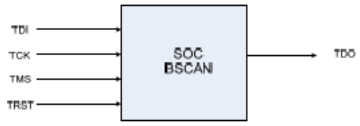

FIG 3 IEEE 1149.1 TAP

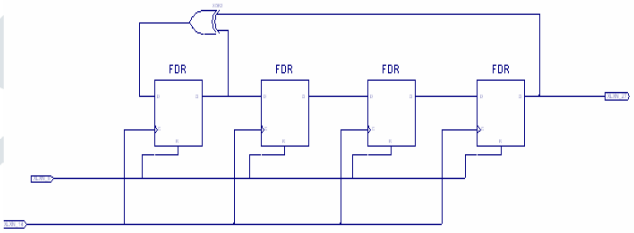

FIG 4 LFSR

Normally the feedback taps are selected such that entire sequence is generated including all zeros and one's. The generation of all zero's pattern requires an additional NOR gate whose inputs are the outputs of all flip-flops in the LFSR. The output of theNOR gate is fed into the input of

the first flip-flop in the circuit as shown in Figure 4.

TABLE 1 : AN EXAMPLE OF LT-LFSR USING A 8-BIT LFSR

# clk	pattern	en1	en2	sel1	sel2	LT-LFSR (S=0)	
1	T^{i}	1	0	1	1	1010	1011
2	T^{i1}	0	0	1	0	1010	1111
3	T^{i2}	0	1	1	1	1010	0101
4	T^{i3}	0	0	0	1	1111	0101
5	T^{i+1}	1	0	1	1	0101	0101
...	...	...		...		...	...

The increased power consumption by the device in the manufacturing test environment therefore can in most cases exceed the maximum power consumption specification of the IC resulting in un-repairable device failures begins with a pattern generated using a conventional LFSR causing significant loss of yield.

IV. LOW POWER TEST PATTERN GENERATION

One way to improve the correlation between the bits of the successive vectors is to avoid frequent transitioning of the logic levels (1 to 0 or 0 to 1) of the primary inputs.

The new approach entails inserting 3 intermediate vectors between every two successive vectors. The total number of signal transitions between these 5 vectors is equal to the total number of signal transitions between the 2 successive vectors generated using the conventional approach. This reduction of signal transition activity in the primary inputs reduces the switching activity inside the design under test and therefore results in reduced power Consumption by the device under test.

The technique of inserting 3 intermediate vectors is achieved by modifying the conventional LFSR circuit with two additional levels of logic between the conventional flip-flop outputs and the low power outputs as shown in Figure 4.1. The first level of hierarchy from the top down includes logic circuit design for propagating either the present or the next state of the flip-flops to the second level of hierarchy. The second level of hierarchy is a multiplexer function that provides for selecting between the two st

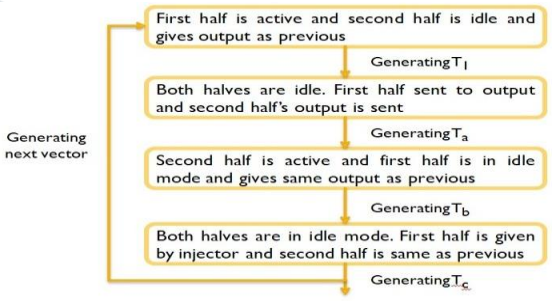

FIG 5 PROPOSED ALGORITHM FOR LOW POWER LFSR

In the simulation environment, the outputs of the flip-flops are loaded with the seed vector. The feedback taps are n selected pertinent to the characteristic polynomial $x^8 + x + 1$. Only 2 inputs pins, namely test enable and clock are required to activate the generation of the pattern as well as simulation of the design circuit. It is also noteworthy here that the intermediate vectors in addition to aiding in reducing the number of transitions can also empirically assist in detecting faults just as good as the conventional LFSR patterns.

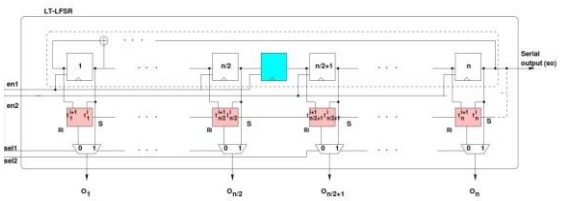

FIG 6 STRUCTURE OF LP-LFSR

The number of LFSR outputs required is driven by the number of test inputs required for circuit under test.

The pattern generation controller which is designed using Verilog as shown in Appendix A can be very easily modified for the required number of LFSR outputs.

V.CONCLUSION

This paper presents a new low-power LFSR to reduce the average and peak power of combinational and sequential circuits during the test mode. It is observed that the total power consumed in modified LFSR is less than the power consumed with normal LFSR and output dynamic power is decreased.

This is with almost no increase in test length to hit a target fault coverage. LT-LFSR significantly reduces the instantaneous power violation compared to the LFSR and thus avoids putting stress on the circuit during test which increases reliability. It is concluded that low power LFSR is very useful for BIST implementation in which the CUT may be Combinational, sequential and memory circuits.

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