Design of 32 bit-bit sliced Multiplier using VHDL

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Abstract : A 32x32 bit using 4-bit bit-sliced rapid Single Flux Quantum (RSFQ) integer multiplier is proposed. The multiplier mainly consists of bit-slice multiplier and kogge stone adder. Quantum technology is implemented for its high speed and low power consumption. As in every digital circuit addition and multiplication are two most essential mathematical operations. With the increase in circuit complexity and hardware cost bit slice approach is used. The results shows that a 32 bit bit slice processing has the least latency at 10Ghz.

IndexTerms - Rapid Single Flux Quantum (RSFQ), Quantum Technology.

I. INTRODUCTION

Superconducting rapid single-flux technology [1] and its energy efficient derivatives is future trending technology usually known for its high speed and low power consumption[2]. Bit-serial processing involves bigger latency in process 32-bit data[1], whereas data processing can cause high hardware price. Therefore, we tend to project the bit-slice process that achieves higher speed than bit serial process and fewer hardware prices than data processing.

Multiplication is one among the fundamental and demanding operations within the computations. In recent years, superconducting[3].RSFQ method is one of the most trending integrated circuit technologies which is specially known for its ease of use. Bit-slice architecture ,where data are divided into several bits each, has faster speed that bit serial architecture and lower hardware cost than parallel architecture[2]

In this paper, we show a design of 32x32 bit 4-bit bit slice integer multiplier. The multiplier proposed in this paper carries out unsigned integer multiplication. It is based on the Wallace multiplication algorithm that we proposed in[3]. We have designed a physical layout with target frequency of 10 GHz using Xilinx ISE 14.7 tool. Simulation results shows the correct operation with frequency of 10 GHz results.

II. 4-BIT WALLACE MULTIPLIER

Each of the 32-bit multiplicand A and multiplier B is splited into eight slices of 4-bit each. The eight pairs of quantity slices are input one by one from the smallest amount vital one. The number performs 32x32bit bit-unsigned number multiplication output one by one from t. The 64-bit final product P is in sixteen 4-bit slices that are output one by one from the smallest amount vital one.

Wallace is the fastest process for multiplication of two digit number.[4] The steps to be followed for the multiplication of two numbers. At the initial steps bit products are generated and in next step reduce the product matrix into row matrix. Whereas bit products are equal to sum of two rows. In the last step the fast adder are used for summing of two resulting rows to generate final products.[5]

The above fig.1 shows the 4-bit Wallace Structure. The generated bit product after the multiplication of 4-bit numbers are fed to the half adder and full adder.[6] If only two bits are to be added then it is given to the half adder and if the three bits are fed at an instant then it is given to the full adder. In this manner whole structure is form for the 4-bit Wallace multiplier. At the output of these fast adder the final 8-bit products are generated.

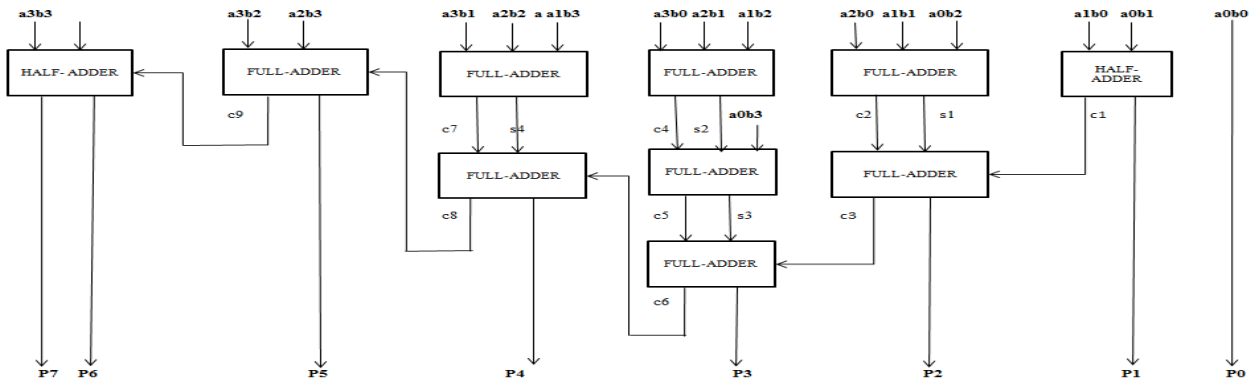

Fig.1: 4-Bit Wallace Block Diagram.

III. IMPLEMENTATION

The multiplier is implemented in VHDL CODES and the simulations results are studied in the Xilinx ISE platform. The first step is to design the 4-bit Wallace multiplier i.e. bit slice multiplier and then in order to implement the 8x8 bit multiplier a adder is designed. The adder used in this multiplier is 8 bit Kogge-Stone adder which is a parallel prefix form of carry look-ahead adder. In same way the 16x16 bit and 32x32 bit multiplier is designed for that 10 bit and 11 bit kogge stone is designed respectively. Each of the 32-bit multiplicand and A(=[a31,a30,….a1,a0]) and multiplier B(=[b31,b30,….b1,b0]) is divided into 8 slices of 4-bit each. The eight pairs of operand slices are input one by one to the multiplier from the least significant one. . The 64 bit product P(=[p63,p62,….p1,p0]) is in sixteen 4-bit slices that are output one by one to the least significant one.

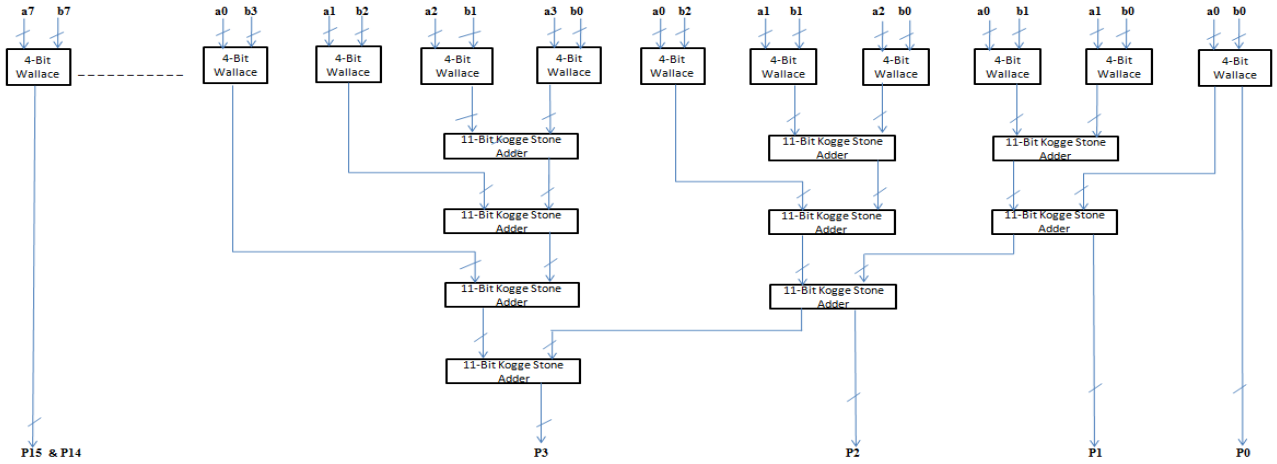

Fig.2: 32-Bit Bit Slice Multiplier

IV. SIMULATIONS

The proposed 32x32 bit 4-bit slice multiplier has been designed. RTL view of the 32-bit multiplier is as shown in fig.3 and internal structure of the 32-bit is as shown in fig.4. The fig.5 shows the simulation results of the designed 32-bit bit slice multiplier in Xilinx ISE design suit. The simulation results shows that multiplier operates correct at 10 GHz.

Fig.3: RTL View of 32-bit multiplier

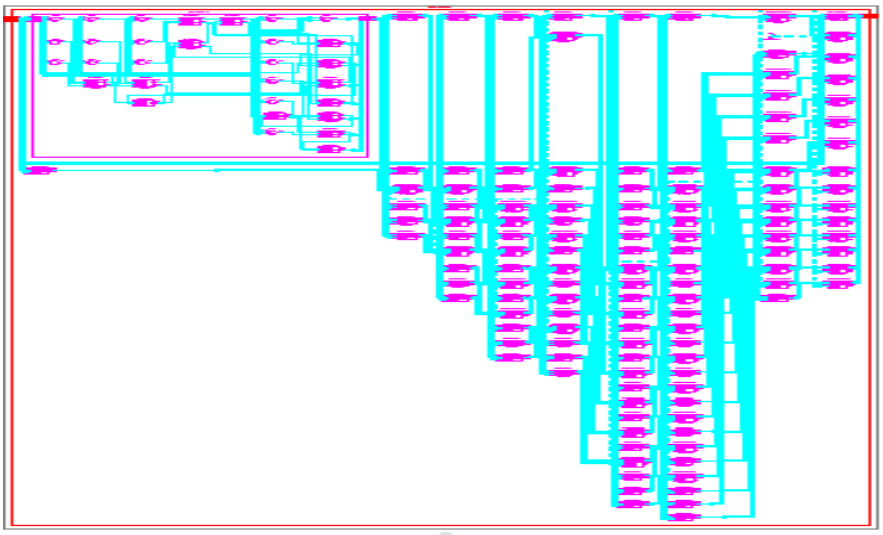

Fig.4: Internal Structure of 32-bit multiplier

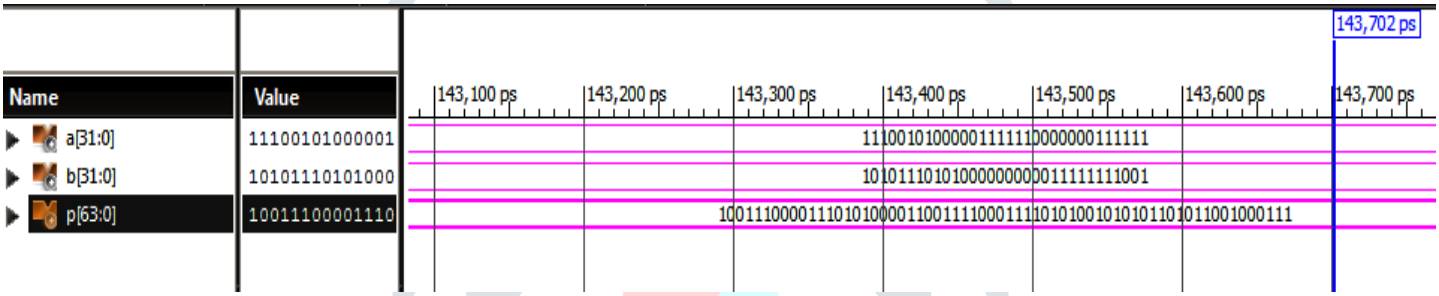

Fig.5: Simulation Result for 32 bit multiplier

V. DISCUSSION

We have design the logic circuits of 4-/8-/16-/32-bit bit-slice integer multiplier. The comparison the proposed integer multiplier is shown in Table I. the latency of the integer multiplier is analyzed by the following formula

$$\text{Latency} = \text{clock delay} + \left(\text{pipeline stages} + \frac{\text{word length}}{\text{slice size}} * 2n^2\right) * \text{clock period} \quad \text{.....[1]}$$

here "clock delay" is defined as the total delay of the cells from clock-in and clock-out. "n" represents the dimension of the matrix.[1]

As shown in Table I, 32-bit bit slice multiplier has the least latency and can achieve the trade off between the hardware cost and at 10 GHz. A 32 x 32 bit 4-bit slice multiplier has been implemented with Xilinx ISE 14.7 tool which has the least latency of 14624.2 ps (=1.4 x 10-5ms) at 10 GHz. The performance of the proposed bit-slice integer multiplier is better than the matrix multiplier.

VI. CONCLUSION

We have studied the 32 x 32 bit 4 bit-slice RSFQ multiplier using a Xilinx ISE 14.7 tool. The results show that 32-bit bit slice processing has the least latency at 10 GHz. It consist of 4464 AND gates,6196 XOR gates, 3329 OR gates. It consist of 52 pipeline stages, a total and latency of 14624.2ps.

Table 1: Comparison

Bit-Slice size	#AND	#XOR	# OR	Kogge stone adder	Wallace Multiplier	Pipeline stages	Clock delay(ps)	Latency @10GHz(ps)
4-Bit	44	21	14	-	7	7	>504.7	>2304.7
8-Bit	224	210	122	3	7	22	>554.8	>5754.8
16-Bit	1004	1206	659	4	7	27	>744.1	>7744.1
32-Bit	4464	6196	3329	9	7	52	>1024	>14624.2

VII. REFERENCES

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