Area Efficient Fixed-Point LMS Adaptive Filter

[1]Harish Kumar K, [2]Dhanasekar S, [3]Jayakumar R, [4]Ajin R
[1]Student, [2] Student, [3] Student, [4]Assistant Professor
[1]Electronics and Communication Engineering,
[1,2,3,4]Prathyusha Engineering College, Tiruvallur, India

Abstract : Some high performance systems like digital signal processors (DSP), microprocessors, FIR filters etc. uses barrel shifters, multipliers, multiplexers, delay elements as key components. Performance of the multiplier determines the system's performance. Multipliers are very slow and also consume most of the area in the system. Hence, optimization of speed and area are major constrains in the design of multiplier. Least Mean Squared (LMS) algorithm benefits as low convolution and coherence of implementation. One main concern in all experimental situations is to develop stemmer that provide faster convergence of the adaptive filter by the instant better filtering performance. A better architecture for the implementation of a DLMS adaptive filter to achieve low adaptation-delay and efficient area, we propose the use of a novel partial product generator and a scheme for optimized balanced pipelining across the time-consuming combinational blocks. This have less area-delay product (ADP) and less energy-delay product (EDP) than the best of the existing systolic structures, on average, for N = 8, 16, 32 and 64.We propose an efficient fixed-point implementation scheme of the proposed architecture, and thereby replacing shift adder tree by carry select adder.

Index Terms **- Adaptive filters, fixed-point arithmetic, least mean square (LMS) algorithm.**

I. INTRODUCTION

The digital signal processing implementations has abundant use of adaptive digital filter. A filter is a device that removes unnecessary signal. Filtering is a type of signal processing that drops noise and error signal [2]. There are different types of filters used in different ways. In that least mean square (LMS) adaptive filter is used to improve the power performance [1],[4]. Adaptive filter is a connection between two signals for real time applications. The structure of an adaptive filter defines how the output signal is calculated from input signal. LMS algorithm is used to reduce a desired filter by detecting the coefficients of the filter that produce the least mean square of the error signal i.e. difference between desired output and original output [2] . The fundamental idea of the LMS filter is to optimize the filter weight by upgrading the filter weights .Two bit multiplication and adder tree is used for pipelined computation to reduce the area and critical path [5]. The previous effort of an delayed LMS adaptive filter is not examined with the fixed point implementation [3],[4]. Formely they made use of FIR filter and weight update blocks as an alternative of error computation block. When collated with FIR filter, LMS adaptive filter is more efficient and also reduces the area and number of delays.

II. EXISTING SYSTEM

The existing work on the DLMS adaptive filter have left discussing about the fixed-point implementation issues such as position of radix point, option of word length, and quantization at several stages of computation, even though they directly affect the convergence performance, predominantly due to the recursive behavior of the LMS algorithm [9]. Each of the algorithm has both advantage and disadvantage with respect to their implementation. So, there is a continual requirement and effort across the signal processing community for improving the current algorithms in terms of improving both performance and reducing the computational complexity.

A. Digital Filter-

A Digital Filter is a structure that performs mathematical tasks. Usually it consists of an analog-to-digital converter to sample the input signal, followed by a microprocessor and some peripheral devices such as memory to store data and filter coefficients and the digital-to-analog converter used to complete the output stage [4]. Program Instructions on the microprocessor implement the digital filter by performing the important mathematical operations on the numbers received from the Analog to Digital converter (ADC) [3]. In numerous high performance applications, an FPGA or ASIC is used instead of a general purpose microprocessor, or a DSP with specific paralleled architecture for filtering.

B. *Adaptive Filter-*

Adaptive filter is a computational device used for mathematical operations, that iteratively shows the relationship between the input/output signals of the adaptive filter [9]. An adaptive filter manually adjusts the filter coefficients according to an adaptive algorithm. The following Fig 1 shows the diagram of a typical adaptive filter.

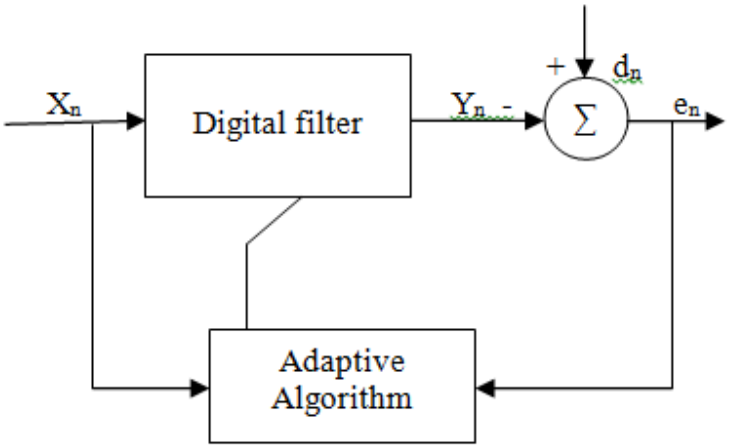

Fig.1 Adaptive Filter

III.ANALYSIS OF DELAYED LMS ADAPTIVE FILTER

The weights of LMS adaptive filter during the *n*th iteration are updated according to the following equations

$$\mathbf{W}_n+1 = \mathbf{w}_n + \mu \cdot e_n \cdot \mathbf{x}_n \quad (1a)$$

where

$$e_n = d_n - y_n \; y_n = \mathbf{w}\mathrm{T}n \cdot \mathbf{x}_n \quad (1b)$$

where the input vector **x***n*, and the weight vector **w***n* at the *n*th iteration are, respectively, given by

$$\mathbf{x}_n = [x_n, x_n-1, \ldots, x_n-N+1]\mathrm{T}$$

$$\mathbf{w}_n = [w_n(0), w_n(1), \ldots, w_n(N-1)]T$$

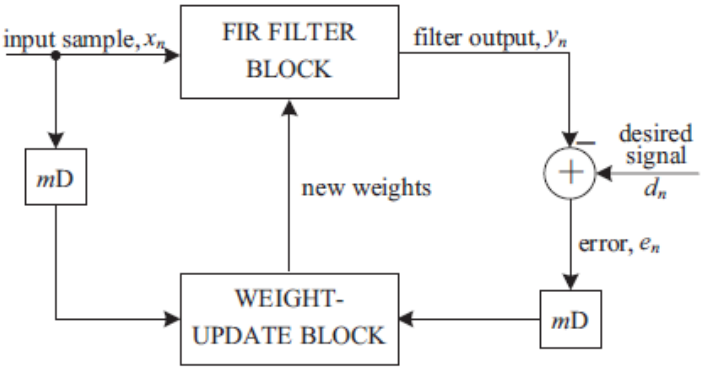

Fig.2. Structure of the conventional delayed LMS adaptive filter.

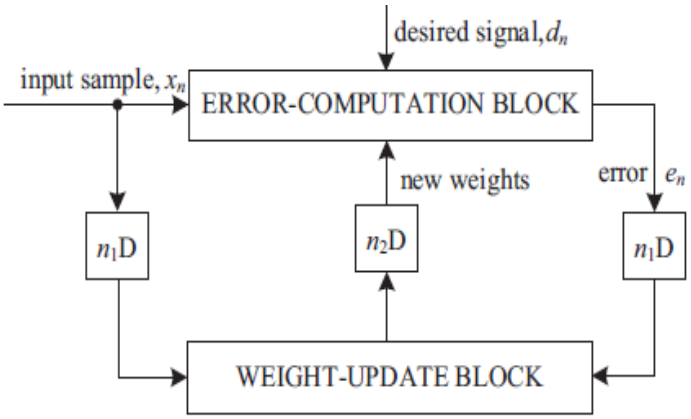

Fig.3. Structure of the modified delayed LMS adaptive filter

d_n is the desired response, y_n is the filter output, and e_n represents the error figured out/calculated during the nth cycle. Î¼ is the step-size, and N is the number of weights used in the LMS filter. In the case of pipelined designs with m pipeline stages ,the error e_n becomes available after m cycles, where m is called the "helpful change delay [2]. The DLMS uses set of computer instructions therefore the delayed error e_n-m ,the error matching up to(n- m)th cycle for updating the current weight instead of the recent-most error. The weight-update equation of DLMS

$$\mathbf{w}_n+1 = \mathbf{w}_n + \mu \cdot e_n-m \cdot \mathbf{x}_n-m. \qquad (2)$$

The block diagram of the DLMS filter is shown in Fig.2, where the helpful change delay of m cycles amounts to the delay introduced by the whole of filter structure consisting of limited unplanned desire response (FIR) filtering and the weight-update process [6]. It is shown in that the helpful change delay of ordinary LMS can be rotten into two parts: one part is the delay introduced by the pipeline stages in FIR filtering, and the other part is due to the delay involved in pipelining the weight update process. Based on such a rotting of delay, the DLMS (able to change and get better) filter can be put into use by a structure shown in Fig. 2. Assuming that the delay of computation of error is n1 cycles, the error figured out/calculated by the structure at the nth cycle is e_n-n1 , which is used with the input samples delayed by n1 cycles to create the weight-increment term. The weight-update equation of the changed DLMS set of computer instructions is given by

$$\mathbf{W}_n+1 = \mathbf{w}_n + \mu \cdot en-n_1 \cdot \mathbf{x}_n-n_1 \qquad (3a)$$

where

$$e_n-n_1 = d_n-n_1 - y_n-n_1 \qquad (3b)$$

and

$$y_n = \mathbf{w}T_n-n_2\, \mathbf{x}_n. \qquad (3c)$$

We see that, during the weight update, the error with n1 delays is used, while the filtering unit uses the weights delayed by n2 cycles. The changed DLMS computer code-related disconnects computations of the error-computation block and the weight-update block and allows us to best pipelining by feedforward cut-set retiming of both these sections separately to the number of pipeline stages and helpful change delay. The filters with different n1 and n2 are for a system identification problem. The 10-tap band-pass filter with sudden (unplanned) desire response

$$h_n = \frac{\sin(w_H(n-4.5))}{\pi(n-4.5)} - \frac{\sin(w_L(n-4.5))}{\pi(n-4.5)}$$

for $n = 0, 1, 2, \ldots, 9$, otherwise $h_n = 0$,W_H and w_L represent the high and low cutoff frequencies of the passband, and are set to $w_H = 0.7\pi$ and $W_L = 0.3\pi$, respectively. The step size μ is set to 0.4. A 16-tap adaptive filter identifies the unknown system with Gaussian random input x_n of zero mean and unit variance [7]. In all cases, outputs of known system are of togetherness power, and contaminated with white Gaussian noise of aˆ'70 dB strength. Fig.4 shows the learning curve of MSE of the error signal e_n by averaging 20 runs for the ordinary LMS filter $(n_1 = 0, n_2 = 0)$ and DLMS adaptive filters with $(n_1 = 5, n_2 = 1)$ and $(n_1 = 7, n_2 = 2)$. It can be seen that, as the total number of delays increases, the coming together is slowed down, while the steady-state MSE remains almost the same in all cases. In this example, the MSE difference between the cases $(n_1 = 5, n_2 = 1)$ and $(n_1 = 7, n_2 = 2)$ after 2000 iterations is less than 1 dB, on average.

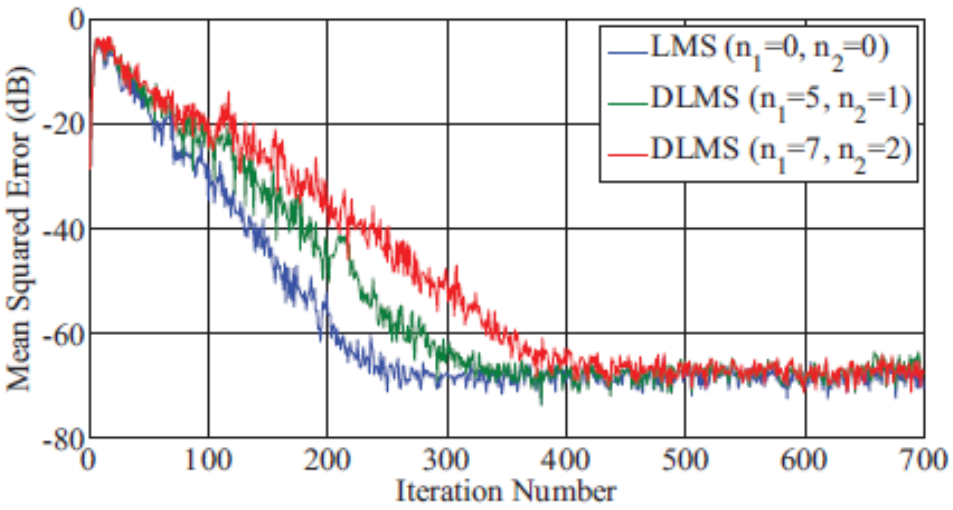

Fig.4 Convergence performance of system identification with LMS and modified DLMS adaptive filters.

III.PROPOSED ARCHITECTURE

As shown in Fig. 3, there are two main computing blocks in the adaptive filter structural design: 1) the error-computation block, and 2) weight-update block. In this Section, we discuss the design strategy of the proposed structure to minimize the adaptation delay in the error-computation block, followed by the weight-update block.

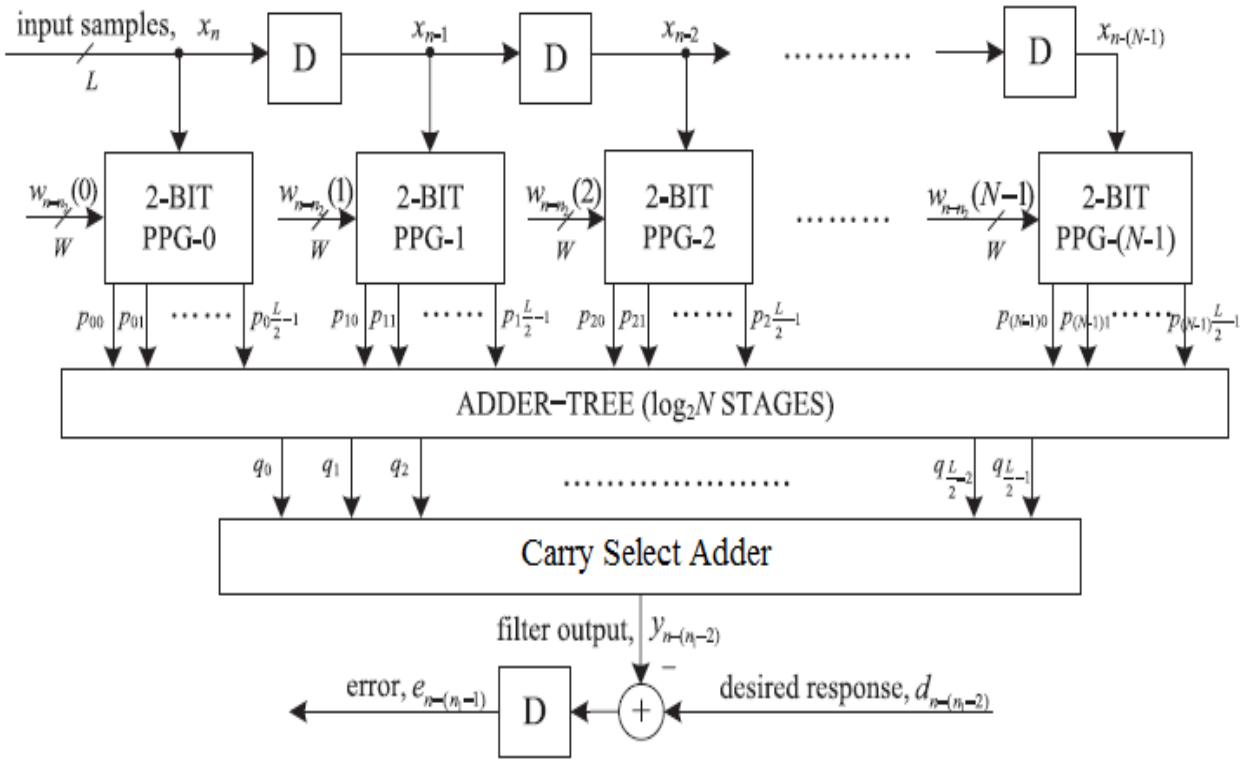

Fig.5 Proposed structure of the error-computation block.

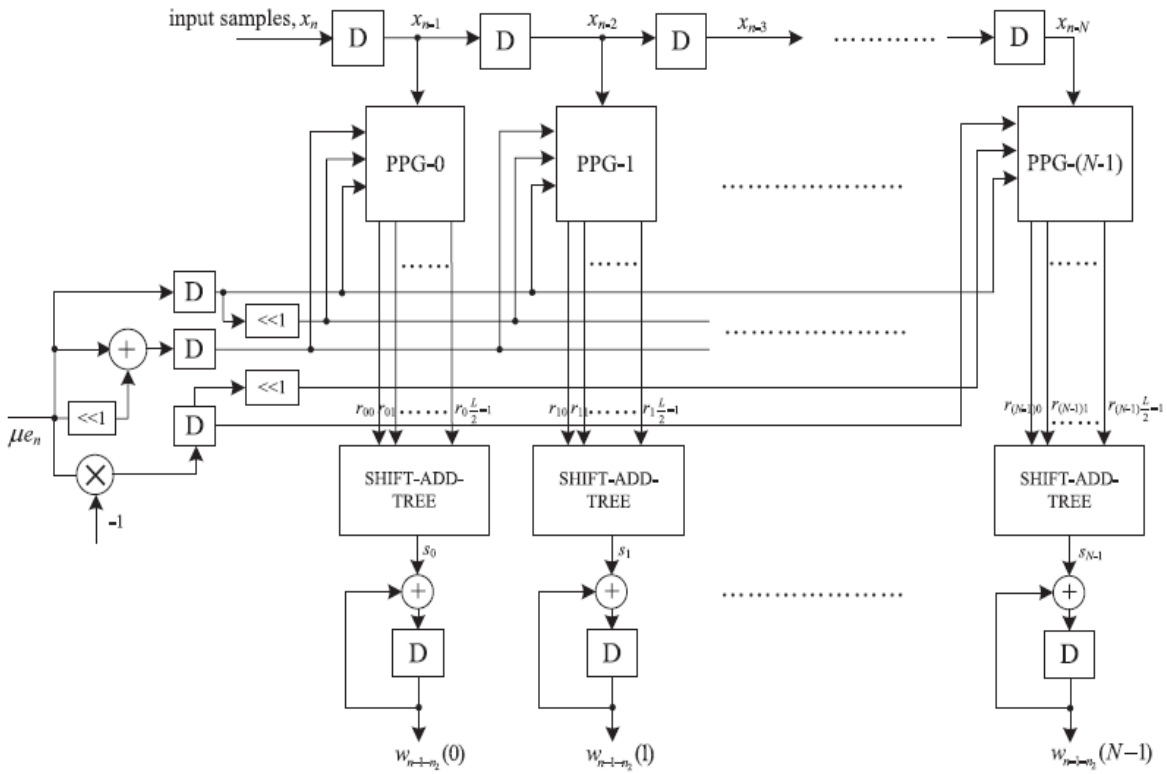

Fig.6 Proposed Structure of Weight Update Block

IV.RESULTS AND DISCUSSION

The delayed LMS filter is designed and simulated using Xilinx ISE. The simulation result as shown in Fig 7.

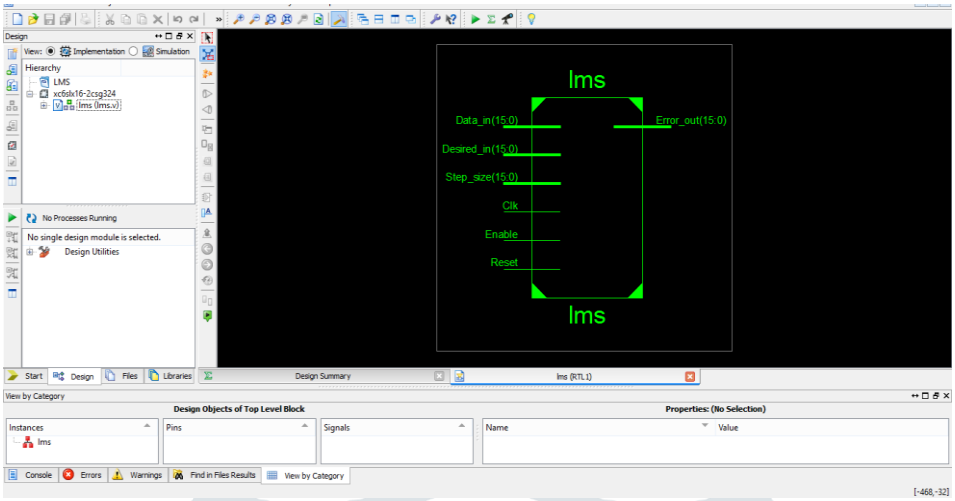

Fig 7 Design of LMS in Xilinx

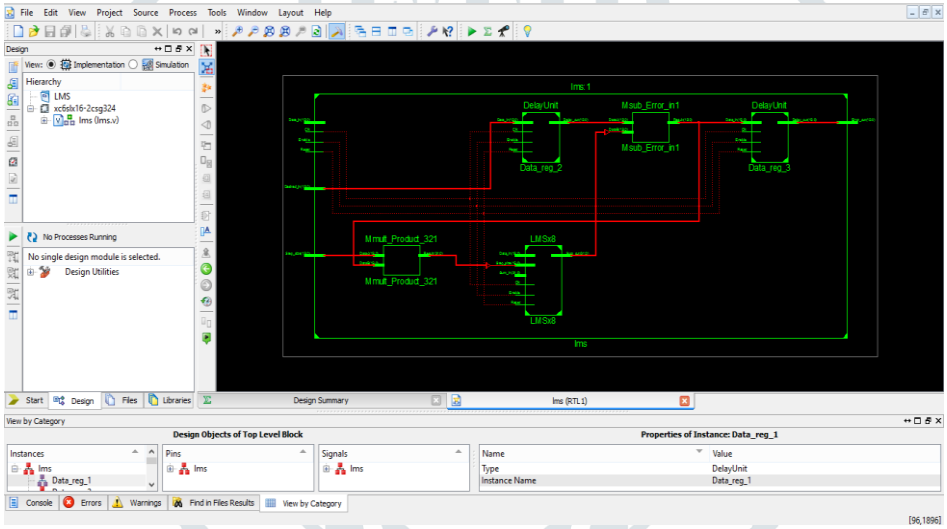

Fig 8 Internal design of LMS in Xilinx

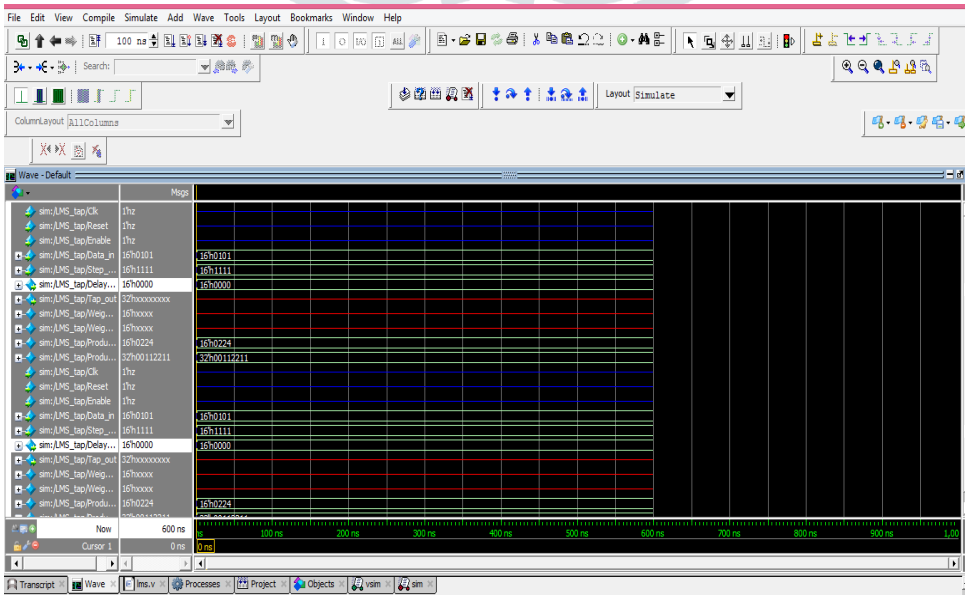

Fig.9 Simulated Output of LMS Adaptive Filter

V CONCLUSION

We propose a better architecture for the implementation of a DLMS adaptive filter to achieve low adaptation-delay and efficient area, we propose the use of a novel partial product generator and a scheme for optimized balanced pipelining across the time-consuming combinational blocks. This have less area-delay product (ADP) and less energy-delay product (EDP) than the best of the existing systolic structures, on average, for N = 8, 16, 32 and 64.We propose an efficient fixed-point implementation scheme of the proposed architecture, and thereby replacing shift adder tree by carry select adder. The main focus of this project has been to increase the quality of services and system capacity. For that purpose low power LMS equalizer are implemented. Its performance is evaluated and tested in FPGA. Compare to the existing system the new proposed system have high speed, low power and area.

VI. REFERENCE

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