# REVIEWOF LOW POWER MULTICYCLE MIPS PROCESSOR USING HDL

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***Abstract:*** With the advent of very large scale design techniques it is possible to fabricate more transistors. The processors are a major information processing element in all electronic circuits. This paper discusses the structure of multi-cycle low power 32-bit multicycle MIPS processor. The MIPS processor will be designed utilizing HDL. Here, we propose the architecture of multi-cycle pipelined 32-bit Microprocessor. Our processor will have no Interlocked Pipeline Stages (MIPS). This processor is a Reduced Instruction Set Computing (RISC) structure based processor. This processor is configured with multiple stages of pipeline. These stages include Instruction Fetch (IF), Instruction Decode and Enroll Fetch (ID), Execution& Address Calculation (EX), Memory Access (MEM) and Write Back (WB) modules. The fundamental components of the processor are CPU, ALU, Program Counter, Control Unit, MUX, Information Memory, Register File, Sign Extension, Instruction Memory.

***Keywords:*** **Microprocessor without Interlocked Pipeline Stages (MIPS), — Reduced Instruction Set Computer (RISC), Complex Instruction Set Computer (CISC), Hardware description languages (HDL), Verilog.**

## I. INTRODUCTION

Microchips and Microcontrollers are generally made in the locale out of two principal PC plans: Complex Direction-Set Computing for example CISC plan and Lessened Instruction Set Computing for example RISC plan.
The possibility of CISC relies upon Instruction Set Engineering (ISA) plan that builds performing further with a couple of bearings utilizing a variable number of operands and an all-inclusive assortment of keeping an eye on modes in various zones in its Instruction Set[1].

Henceforth making them have fluctuating execution time and lengths along these lines absolutely instructing a baffling Control Unit, which possesses a tremendously existent district on the chip?
Differentiated and their CISC basic, RISC processors regularly support a modest course of action of rules.
A demonstrate that contrasts RISC processor and a CISC processor, the quantity of rules in a RISC Processor is low while the quantity of comprehensively helpful registers, watching out for modes, settled heading length and burden store configuration is more this, along these lines, energizes the execution of rules to be finished in a short range as such achieving higher as a rule execution.

The MIPS is a RISC based chip structure that was made by MIPS Computer Systems Inc.
Structure of MIPS RISC chip fuses, fixed length bearings, clear decoded rule organize, memory gets to limited to load and store headings, the designed control unit, a tremendous all around helpful enlist record, likewise, exercises executing inside the registers of the chip.

### 1.1 The inspirations to have the far reaching heading set are:

1. CISC systems are puzzling as the designing and the rules are changed by the development and subsequently, there is an essential for progressively number of rules and thusly will have many watching out for modes.
2. The guideline limit of any microchip is to bring the data and procedure it. The chip in that limit doesn't have any course of action for memory i.e., memory is external. As procedure needs to get to data from a memory or from I/O peripherals there is a requirement for more headings..

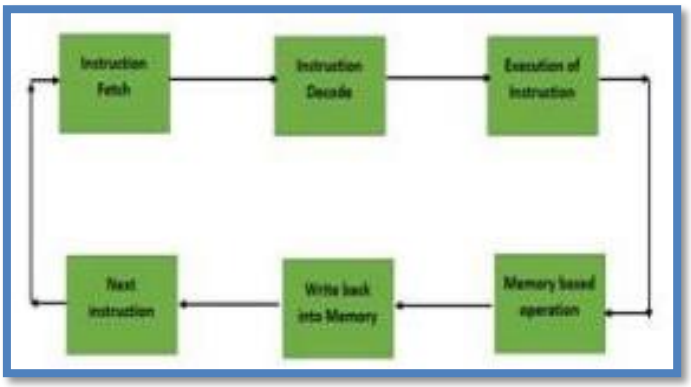


**Figure1: Flowchart showing the multi-cycle MIPS operations**

The Multi-cycle MIPS executes each course by apportioning into various advances. These methods have showed up in the edge of a flowchart in figure[2].

The underlying two phases for example the bringing of the rule and the deciphering of bearings proceed as before for all sort of headings. After the deciphering step the execution occurs as demonstrated by the opcode regard. The processor has been planned for a total of 18 rules.

## II. LITERATURE SURVEY

A lot of research papers have been published on 8-bit RISC processor configuration.. The proposed processor has a harvard architecture. The prominent component of proposed processor is pipelining, used for upgrading execution, with the ultimate objective that on each clock cycle one guideline will be executed. Another basic component is thatguideline set contains only 34 headings, which is exceptionally fundamental, easy to learn and smaller. The proposed processor has 8-bit ALU, Two 8-bit I/O ports, sequential in/sequential out ports, Eight 8-bituniversally valuable registers, 4-bit flag enroll and need based three vectored meddles. Another favorable position of the proposed processor is that it can execute programs with up to 262,144guidelines in length, to such an extent, to the point that any appropriate ventures can be fitted into it[3]. The proposed processor is physically kept an eye on Xilinx Kintex 7 Starter Board FPGA with 0.0517µsguideline cycle. This paper demonstrates the framework and execution of a low power five-organize parallel pipelined structure of aMIPS-64 flawless CPU. The diverse squares in corporate the data way, control rationale ,information and program memories. Danger recognition and data sending units have been incorporated for beneficial use of the pipeline.An balanced structure is suggested that promptsnoteworthy control decline by diminishing undesirable changes. Verilog setup tookafter by amalgamation on to Xilinx Kintex 7 FPGAwas wrapped up. On-chip appropriated memory ofKintex 7 was used for the data and theprogram memory usage"shaikafroz et al, "execution of risc-based.

Engineering for low power applications"2013 referenced a Reduced Instruction Set compiler (RISC) is a microchip that had been structured toperform a little arrangement of guidelines, with the point of expanding the general speed of the processor alongside decreasing the power devouring while at the same time executing the guidance. Additionally presented the RISC engineering adheres to the rationality that one guidance ought to be played out each cycle. Their work displays the structure and execution of a 32 bit RISC delicate center processor proposed for PC engineering acquaintance considered with be a viable answer for PC perception. The possibility of this task was to make a microchip as a structure obstruct in VHDL than later effectively can be incorporated into a bigger plan[4].

Priyavrat Bhardwaj et al "plan Simulation of a 32-bit risc based mips processor utilizing verilog" 2016, this examination paper presents structure & reenactment of a superior five phase pipelined 32-bit Microprocessor without Interlocked Pipeline Stages (MIPS),which is a Reduced Instruction Set Computing (RISC) design based processor. This processor was structured with5 periods of pipeline specifically Instruction Fetch (IF), Instruction Decode& Register Fetch (ID), Execution& Address Calculation (EX), Memory Access (MEM) and Write Back (WB) modules. The structuring of this processor is created utilizing the Hardware Description Language (HDL) - Verilog in ModelSim test system. The incomparable point of this paper is to build up the RTL rationale configuration utilizing Xilinx instrument.

Mohammad zaid et al" structure and Application of risc processor" 2017, This paper introduces the plan of multi-cycle 32-bit Reduced Instruction Set Computer (RISC) processor for better execution and higher speed of activity, The processor is fit for executing increasingly number of guidelines with basic structure and less basic way delay. The planned processor was reproduced and orchestrated utilizing Xilinx 14.7 ISE structure suite. The processor executes every single guidance in more than one cycle that is the reason the term multi-cycle.

## III. MICROPROCESSOR WITHOUT INTERLOCKED PIPELINE STAGE (MIPS)

MIPS is a RISC based processor which comprises of 32 registers.. The initial 6-bits speak to the opcode esteem. The opcode esteem chooses which kind of guidance is to be executed.[5] There are three sort of directions designs that are upheld by the MIPS relying upon the estimation of the opcode in particular:

• R-type Instructions

• J-type Instructions

• Immediate sort Instructions

The key important parameter of our processor is its optimized pipelining. Pipelining is an implementation technique in which multiple instructions are overlapped in execution. The five- stage pipelined CPU allows overlapping execution of multiple instructions. Although an instruction takes five clock cycle to pass through the pipeline, a new instruction can enter the pipeline during every clock cycle[5]. Under ideal circumstances, the pipelined CPU can produce a result in every clock cycle. Because in a pipelined CPU there are multiple operations in each clock cycle, we must save the temporary results in each pipeline stage into pipeline registers for use in the follow-up stages. We have five stages: IF, ID, EXE, MEM, and WB. The PC can be considered as the first pipeline register at the beginning of the first stage. We name the other pipeline registers as IF/ID, ID/EXE, EXE/MEM, and MEM/WB in sequence. In order to understand in depth how the pipelined CPU works, we will show the circuits that are required in each pipeline stage of a baseline CPU.Figure 1 demonstrates a square graph with the four state components: the program counter, register document, and guidance and information memories.[2]

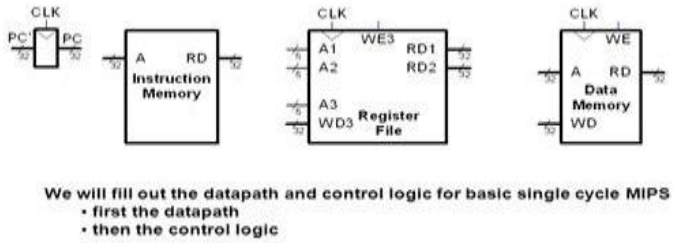


**Figure 2. State elements of MIPS processor**

The Dashed lines show 32-bit information transports and 5-bit address transports on the register document. The program counter is an exceptionally straightforward 32-bit register. The yield of program counter, PC, focuses to the present guidance while the info, PC', demonstrates the location of the following instruction[2].

## IV. MULTI-CYCLE MIPS

The circuit in the Instruction Fetch Stage (IF) stage are shown in Figure 3. Also, looking at the first clock cycle in Figure 1(b), the first lw instruction is being fetched. In the IF stage, there is an instruction memory module and an adder between two pipeline registers[6]. The left most pipeline register is the PC; it holds 100. In the end of the first cycle (at the rising edge of clk), the instruction fetched from instruction memory is written into the IF/ID register. Meanwhile, the output of the adder (PC + 4, the next PC) is written into PC.

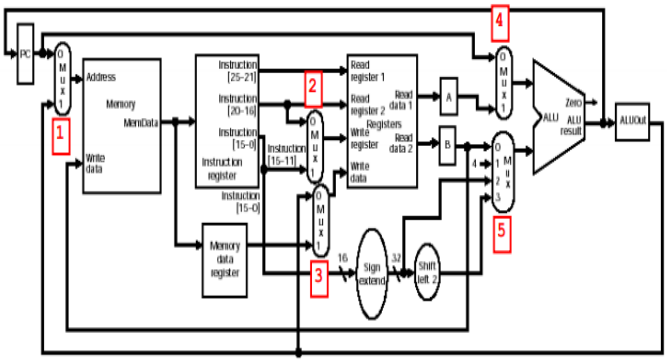


**Figure 3. Complete Multi-cycle MIPS datapath**

In the second cycle, the first instruction entered the ID stage. There are two jobs in the second cycle: to decode the first instruction in the ID stage, and to fetch the second instruction in the IF stage. The two instructions are shown on the top of the figures: the first instruction is in the ID stage, and the second instruction is in the IF stage. The first instruction in the ID stage comes from the IF/ID register. Two operands are read from the register file (Regfile in the figure) based on rs and rt, although the lw instruction does not use the operand in the register rt. The immediate (imm) is sign- extended into 32 bits. The regrt signal is used in the ID stage that selects the destination register number; all others must be written into the ID/EXE register for later use. At the end of the second cycle, all the data and control signals, except for regrt, in the ID stage are written into the ID/EXE register. At the same time, the PC and the IF/ID register are also updated.

**Conclusion:**

In the paper we aim to design a Low Power 32-bit multicycle MIPS processor by utilizing Xilinx ISE and Altera Quartus EDA tools. Key low power strategies like clock gating and grey encoding will be applied to the proposed architecture.

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