# REVIEW OF PROPOSED HIGH-EFFICIENCY VIDEO CODING (HEVC) STANDARD

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*Abstract:* The objective of this paper is to provide a review of the recent development in HEVC standard with integer DCT with summaries of technological advancement. In this paper, we discuss Integer discrete cosine transform (DCT) of High-Efficiency Video Coding HEVC for video compression. It uses 2D DCT from 4x4 to 32x32 transform with higher precision as compared to h.264/AVC. In this paper, we propose an area efficient and energy efficient VLSI architecture of HEVC. We propose a new efficient Constant Matrix Multiplication scheme (CMM) can be used to find parallel architecture for 1d integer DCT having different length of 4-pt., 8-pt., 16-pt. and 32-pt. with the throughput of 32 DCT coefficient per cycle with respect to transform size. The above architecture reduces the complexity of implementation with slightly effect on the coding performance so we purpose efficient structure with low power called 'Power Efficient Structure' for full parallel implementation of 2D DCT from the synthesis result. It shows that propose architecture involves less area-delay product (ADP) and less energy per sample (EPS) compare to direct implementation of the reference algorithm for integer DCT. Larger transform requires more computation per coefficient and they contain a non-zero coefficient due to this larger transform can be more energy efficient the proposed architecture is found to support UHD which is one of the applications of HEVC

*Keywords* - **Discrete cosine transforms (DCT), Integer DCT, H.265, High-Efficiency Video Coding (HEVC), and Video Coding.**

## I. INTRODUCTION

HEVC stands for High-Efficiency Video Coding (H.265) is the new one latest video coding standard defined by the International Telecommunication Union/ Telecommunication (ITU-T) and ISO (International Standard Organization)/IEC Moving Picture Expert Group (MPEG) working together in a team known as Joint Collaborative Team on Video Coding (JCT-VC) and a first edition of the HEVC to be finalized in 2013. HEVC standard supports different types of applications included different ranges uses with enhancing color format support, video coding. HEVC standard will become MPEG-H Part-2(In ISO/IEC) then ITU-T is considered as ITU-T Recommendation H.265. The ITU-T developed standard named as H.261 and H.263, ISO/IES developed MPEG-1 and MPEG-4, two organization jointly developed H.262/MPEG-2 and H.264/MPEG-4 Advanced Video Coding (AVC) standard. HEVC provides a bit rate reduction up to 50% less as compare to H.264/AVC standard for the video quality.

AVC stands for Advanced Video Coding (H.264) is the video coding standard has been approved by ITU-T Recommendation H.264 by ISO/IEC. AVC is widely used for, transmission of a TV signal with Standard Definition(SD) as well as High Definition (HD) over satellite, cable network, and the storage of high-quality video signal. JVT that is Joint Video Team has to finalize new video coding standard name as H.264/AVC in March 2003.

HEVC standard has been designed and particularly focus on two key issues: 1.increase in video resolution, and 2. Increase in use of parallel processing architecture. With all past ITU-T and ISO/IEC video coding standard, only in HEVC standard bit-stream structure and their syntax is standardized. The mapping is also done in the HEVC standard, that the mapping is defined by the meaning of syntax element and at the decoder side, by decoding process the output getting into bit-stream form. The limitations of the HEVC implementation to specific applications like balancing compression ratio, implementation hardware cost, time to market, and other consideration. HEVC standard is designed for achieving multiple factors; including coding efficiency, transport system and data loss, as well as parallel hardware implementation architecture.

In video compression or image compression, the discrete cosine transform (DCT) plays a very important role related to complexity integer DCT have been studied. The discrete transform is used to convert an image or video into the frequency domain from a special domain. Simply DCT matrix is with floating point and Integer DCT matrix is with fixed point, hence circuit complexity of Integer DCT is less as compare to normal DCT. From this main difference, the HEVC is widely used in the multimedia application, where Integer DCT is included. H.265/HEVC is the latest and modified standard replace by H.264/AVC. Real-time implementation can be done on HEVC for integer DCT. DCT matrix decomposes into sub-matrix by using a lifting scheme where multiplication operation avoided. Multiplier-less multiple constant multiplication (MCM) technique used for 4-pt and 8-pt DCT matrix. And sharing matrix techniques used for 16-pt and 32-pt DCT matrix. Butterfly operation technique has been implemented by the matrix element. A new structure called as Standard Unified Structure (SUS) used for forwarding as well as inverse transform during matrix operation.

DCT is floating point and integer DCT is a fixed point when the circuit complexity of DCT is greater than integer DCT. In recent techniques, HECV is widely used in a multimedia application where included integer DCT.

Application and Design Features:

1. Cable modem, DSL, broadcast over cable, satellite, terrestrial, etc.
2. Highly storage on optical and magnetic devices, DVD, etc.
3. Ethernet, LAN, wireless and mobile network, DSL, modems, etc.
4. Video on Demand, conversational services on ISDN, cable modem, LAN, DSL, wireless network, etc.
5. MMS over ISDN, LAN, wireless and wireless mobile network, etc.

HEVC supports DCT of Different size such as 4, 8, 16 and 32 points. From these different lengths of DCT, the architecture becomes more flexible enough for computation of DCT of any lengths. Constant Matrix Multiplication (CMM) and MCM techniques are the solutions to computing the different length of integer DCT. We have design architecture for 1D and 2D integer DCT for HEVC of any length with the same throughput of transform size. The proposed architecture supports ultrahigh-definition (UHD) which is one of the useful applications of HEVC.

HEVC DESCRIPTION HEVC was produced double compression giving double the pressure productivity as compared with past standard, H.264/AVC. In fact, the pressure productivity comes about change upon the kind of substance and the encoder settings. At normal customer video determination bit rates, HEVC is commonly ready to caught video twice as productively as AVC. Types of compressions there are two types of compressions:-

1. Lossless compression: if the decompressed image is the same replica of the input image compression, and there is no loss in information. Digitally identical to the original image only achieve a modest amount of compression. Lossless compression gives less compression gives a compression ratio because we cannot get the quality compressed image. It involves compressing data when decompressed data will be an exact replica of the original data. This is the case when binary data such as executable are compressed.

2. Lossy compression: Decompressed image is not an actual match of the input image, that compression is known as lossy compression. During lossy image compression, some information is lost. Lossy compression is given higher compression ration so that it is widely used to compressed multimedia data (video, still image), especially in applications such as streaming media and internet telephony.

## II.LITERATURE REVIEW

2.1 Promod Kumar Meher and Sang Yoon Park [1] describes an efficient constant matrix multiplication scheme. MCM architecture is highly consistent with having less area-delay product and less energy consumption than direct implementation for integer DCT matrix. For computing the integer DCT lengths, they proposed a new architecture to derive a reusable architecture for integer DCT. This latest techniques can be used to derive parallel architecture for 1-D integer DCT for different lengths of 4, 8, 16, 32 DCT matrix of a transform. Ahmed proposed a new scheme for the DCT matrix by using a lifting scheme that converted DCT matrix into sub-matrix without using the multiplication method. Shen describes a new scheme that is multiplication multiple constant multiplications (MMCM) for only 4-pt and 8-pt DCT matrix and by using sharing techniques only for 16-pt and 32-pt DCT. Chen proposed a new technique for DCT factorization by using butterfly operation. This operation can be implemented by using shifters, adders, and multiplexors.

Budagavi proposed a DCT matrix structure for matrix decomposition by using forward as well as inverse transform. Modified design for DCT matrix is based on Constant Matrix Multiplication (CMM) but MCM provide solutions for matrix lengths. Integer IDCT can be solved in the same manner as like forward integer IDCT by using MCM techniques. Also, they proposed a power efficient structure to find 2D-DCT by implementing folded and full parallel implementation. The full parallel architecture is more powerful than folded architecture because its complexity and throughput double for fill parallel design also required less energy per cycle. Next algorithm is Bit- pruning algorithm with achieves two factors that are area-delay-product (ADP) and energy-per-sample (EPS) for integer DCT of different length 4, 8, 16, 32 points. This pruning scheme is more effective for the higher length of integer DCT. MCM technique is useful because it requires lee area-delay product and less energy consumption. It reduces area and power complexity for DCT matrix.

2.2 WU Junqin and LI Yanli [2] describe a new type of integer DCT transforming radix. This new type of integer DCT transformation radix can be improved by changing its matrix feeling rule by without any change in the attributes of the integer DCT transform matrix. Also, we studied the fast algorithm, which requires addition and shift operation. So that it can be implemented by fast algorithm and multiplication operation can be avoided.

The second algorithm is the Butterfly algorithm in DCT with considering the 8 point matrix. It is required that it is converted from floating DCT into integer DCT and we need to round off the transform constant terms of the butterfly algorithm. Integer DCT transform is reversible that is forward to transform and inverse transform with 2D DCT. 1D DCT of integer DCT is expressed in one-dimensional column vector with forward and reverse transform. For 8-pt. 1D integer DCT with FFT algorithm, get a quick result within 3 steps of butterfly operation. So in this paper, a fast algorithm exists in the inverse transform of integer DCT achieving by butterfly algorithm. Multiplication operation of transform and inverse transform which can be achieved by multiplication integer DCT fast algorithm. Variant integer DCT transform with particular value for reducing the complexity of compression with improving its performance. By using this fast algorithm integer DCT increases their accuracy. The algorithm is work for reversible transform video transform operation.

2.3Ying Jui Chen [3] describes the Walsh-Hadamard Transform (WHT) and lifting scheme to implement the integer DCT. Bin-DCT is next algorithm to implement integer DCT. This Bin-DCT concept related to the concept of integer lifting scheme, directly it shows that DCT based on WHT and integer lifting scheme. The work of WHT is to lift the transform in a symmetric way. A

novel algorithm is proposed for integer DCT which is related to WHT. DCT Kernel is block-diagonal in WHT is the connector in between DCT and WHT. Lifting mechanism scheme avoids floating point multiplication and this multiplication used by given bits of the transform. This lifting scheme is working only on shifting operation and addition operation. Lossless DCT techniques (LDCT) techniques are the product of both upper and lower triangular matrix having once in all diagonals. A fast algorithm is KLT for natural images, which can be a type of AR random process. Also used integer DCT is the reversible type of DCT.

This paper proposed two scheme Walsh-Hadamard Transform and lifting scheme which is suitable for source coding and communication. Integer DCT is a low level of power consumption. Shifting operation and addition operation is reduces from the Novel algorithm of DCT. Integer DCT is reversible and this reversibility is made possible by lifting scheme. This lifting scheme uses only shifts and addition operation to reduce power consumption and to enable fast consumption.

2.4The author Mohamed Haggag [4] proposed the 1-D Fast integer transform algorithm of the DCT matrix for HEVC. This 1-D integer transform algorithm is developed by based on the symmetric property of the integer transform matrix with matrix operation. The method of dyadic symmetric modified method is used to develop a 1-D fast integer transform algorithm. The aim of this technique is to reduce the complexity of the given algorithm which is implemented in addition and avoid the multiplication operation. We required the combination of Modified Integer Transform and Dyadic symmetry to get the 1-D fast integer transform algorithm. This paper compares the complexity of the algorithm and the transformation quality of 2 algorithms. From this algorithm we able for PSNR on different test sequence. Also, they achieve a better result in HVS than the original algorithm. The proposed algorithm on the transformation matrix this matrix considers as a whole symmetric, and symmetric matrix avoid transformation matrix by the output is in the similar product of transformation matrix multiplied by its transpose matrix.

This algorithm is getting by developing and modifying the position of a matrix element with matrix values. The main advantage of this algorithm is to reduce the computational complexity of the matrix algorithm. The computation complexity referred to as the number of addition and shifts operation with maintaining the error in between the matrix algorithm. Transformation quality of the algorithm is improved by these new techniques PSNR achieves higher values. The proposed algorithm is multiplication free original algorithm which is less complex and given algorithm is multiplication free. This fast algorithm is suitable for quality demanding video coding.

2.5EL. Ansari [5] proposes for integer DCT, proposed new efficient VLSI architecture of HEVC. Ruhan proposed new algorithm i.e. fast hardware architecture for a 4-pt inverse DCT transform for HEVC standard. This technique reduces the number of 1-D DCT calculation in the 2-D IDCT process. Darji and Makwana use a multiplier-less DCT for 1-D DCT VLSI architecture. The addition operation and shift operation is reduced by using CSD-CSE algorithm. In this algorithm, the multiplication operation is completely avoided. Wenjun Zhan proposed a technique of a multiplier-less pipelined architecture base in VLSI for integer 2-D DCT for all HEVC standard. Instead of the multiplication operation, they use addition and shift operation.

Paris Kitsos designed 2-D DCT by using VHDL architecture. They use multiple ROM in this architecture. First design uses two ROM with particular operating frequency and with four Rom operating at a particular frequency. In additional work, the number of different authors proposed hardware for the inverse integer DCT for both AVC and HEVC standard. For the addition and shift operation we proposed and accelerator. Multiplication operation replaces by processing element factor and this operation supports all the matrix element coefficient of integer DCT. In the processing element (PE) architecture the multiplication operation is replaced by a shift and addition operation. Multiplication operation avoided so that DSPs can't use in HEVC. The new efficient Hardware architecture is designed for HEVC by using 2-D integer DCT transform.

They can find 2-d integer DCT by using one block 1-D DCT and one transpose memory. Multiplication operation avoided and instead of multiplication operation we use shift and addition operation. By using entropy coding and filters it increases computational complexity with good performance compare to previous standard H.264/AVC. Accelerating is described in VHDL language by using shift and addition operation in reducing the area of hardware.

2.6Trang Thi Thu Do [6] proposes butterfly structure we developed an algorithm of high- throughput and low-cost hardware for HEVC standard. By using this butterfly structure we minimize critical path lengths than among algorithms. Also, we used the same method to find the minimal critical path length for its multiple constant multiplications and consume small sources as compared to 1-D transform algorithm. With shorter critical path it required a less of addition and shift operation. The second algorithm is called as multiplier-less multiple constant multiplications (MMCM) achieves a shorter critical path with using a small number of addition and shifts operations.

The overall designs of transforms included with even and odd parts block like Partial Butterfly (PB) implementation in the HEVC. Software MMCM algorithm replaces with addition and shifts operation by reducing the operation count instead of the multiplication operation. MMCM and sparse matrix method we decompose the transform using butterfly structure. The algorithm achieves shorter critical path with less number of addition and shifts operation. Shorter critical path consumes less time with the faster speed with high throughput. Hardware design algorithm increases throughput compared to other algorithms.

2.7Mohamed Asan Basiri [7] proposed an efficient VLSI architecture which is used in HEVC for Integer DCT. The proposed 1D architecture is used to design 2D folded and parallel design and with this proposed N-point 1D-Integer DCT architecture include with signed carry save adder tree based with multiplier unit. The proposed 1-D architecture is used to perform 2-point Integer DCT in a parallel way. The discrete transform with considering any transform is used to change the signal representation from one domain to a special domain. This conversion is used for reducing the complexity of a specific digital signal processing application. From many transform techniques, the complexity of the DCT circuit is greater and complicated than Integer DCT,

because of the DCT matrix with floating point and Integer DCT matrix with a fixed point. So that in recent days in the multimedia application the Integer DCT is widely used. Folded design and parallel design are design by using 1D DCT architecture.

I suppose we are taking a 4x4 matrix, it shows that 4x4 2D Integer DCT during row process, a row of the 4x4 matrix is 1D transform and result stored in the buffer in same form of 4x4 row pattern. The procedure will be same for column process, 4x4 column buffer matrixes are 1D transformed and result in getting in 2D transformed value. Folded 2D Integer DCT architecture it has only 1D Integer DCT unit, for both row and column operation. The operation depends upon select line if select=0, then it will perform row operation and for select=1 it will perform column operation. In parallel 2D Integer DCT architecture, there are two 1D Integer DCT units used to perform row and column operations. And the transform buffer is used to stored row value to find the column value. The main difference between parallel and folded architecture is that the area requirement and number of clock cycles. Parallel architecture has a greater number of clock cycles. This paper proposed parallel architecture can be used in the application, where high throughput is the main goal.

2.8 MADHURI and J. KUMAR [8] proposed 2D-DCT hardware architecture for HEVC in FPGA platforms. The architecture supports the different size of DCT including 4x4, 8x8, and 16 x 16, 32x32 matrix element. In this paper author used basic DCT algorithm used in image/video coding and signal processing applications. For fixed-point matrix element, integer values are chosen for transform matrix. By using two 1D-DCT we design a 2D-DCT matrix. First, the 1D-DCT is applied to an individual row of input data and another 1D-DCT is applied to the result which is getting from first 1D-DCT. Transpose buffer is connected in between two 1D-DCT. 2D-DCT involves matrix multiplication method. Multiplication is implemented on DSP block or either inside FPGA. But LUT has a slower operation because of long wire routing with different locations of LUT components. So instead of LUT, DSP block is selected for implementing multiplication, hardware efficiency, and its operating frequency. The proposed 2D-DCT algorithm, 2D-DCT is decomposed into two 1D-DCT.

Frist the input data is read row by row, and then the result is stored in BRAM. Note that the output of the matrix will transpose before saving into two columns of a BRAM. If we want to increase the efficiency of hardware, DSP blocks are suitable for matrix multiplication. DCT transform used even-odd decomposition method because it gives drastic result in a reduction in multiplication and addition method when compared with direct multiplication method. For DCT, butterfly transform can be used in many times, with a maximum number of butterfly transforms requires less number of multipliers. This proposed 2D-DCT architecture is generic and also it has no limit of fabrication for different technology. This fabrication technology leads to higher clock frequency and shorter propagation delay. Blocks are power efficient in high definition video coding application (e.g. HEVC). The proposed architecture has a great advantage in hardware cost, operating frequency, and throughput.

2.9The author Mirino Jhno [9] proposed signed bit matrix based transform algorithm to compress a bit stream of an image or video. The algorithm for hardware implementation of Integer DCT for HEVC categorized into two ways.

A. .Key feature of Integer DCT for HEVC.

B. Hardware-oriented Algorithm.

A. Key features of Integer DCT for HEVC: HEVC having an N-point Integer DCT can be reduced by a butterfly technique using an (N/2) point DCT and a matrix-vector product of (N/2) x (N/2) matrix.

B. Hardware-oriented Algorithm**:** Elements execution requires multiplication and addition operation where multiplication (N/2) and addition (N/2) are the quantity of augmentation. Within this augmentation, subtraction of (N/2) points DCT is done individually. Base on the 2D-DCT method, hardware algorithm for DCT computed for 8, 16, 32-point DCT coefficient also computed formula.

The second algorithm is a signed bit matrix based transform algorithm.

1. Bit-plane decomposition of integer transforms.

For reducing the bit width of any information, for that reduction, we proposed a bit disintegration calculation that changes frame into SBT network. Basically, the SBT network is created in frame-word declination. STB frame-work contains 0 and +1/-1 components. The design change with STB can work all and more beneficially for low piece width computation. The frame-work circuit is proposed for SBT to decreases the number of the adder. The function determines bit-plane disintegration from an NxN with complete number change grid to SBT frameworks. For more STB, more adders are required. Apply proposed SBT calculation, to change grid circuit, the SBT framework circuit is studied and the information is change with the circuit of SBT but individually. SBT network has straightforward components that width of the bit with yield information and transition information decreases.

### C. ACKNOWLEDGMENT

In this paper, we studied different reference paper with different algorithm related to HEVC and present as a review of the recent proposals for HEVC standardization projects. We had seen that many compression improvements are developed by increasing adaptability. The new feature of integer DCT, new transform design have the highest throughput for video codec getting higher resolution videos. The architecture for Integer DCT that is computed the DCT with different lengths of 4, 8, 16, 32 point DCT matrix. From the above techniques, the latest techniques called multiplier-less multiple constant multiplication algorithms are useful because it involves less area complexity and less energy consumption.

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