DESIGN AND IMPLEMENTATION OF LOW POWER AND LOW GLITCH FLIP-FLOPS

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Abstract: In This Paper presents novel designs of static dual-edge triggered (DET) flip-flops that exhibit unique circuit behavior owing to the use of C-elements. Five novel DET flip-flops are presented including two high-performance designs and designs that improve upon common Latch-MUX DET flip-flops so that none of their internal circuit nodes follow changes in the input signal. A common characteristic of the presented flip-flops is their low energy dissipation due to glitches at the input. Novel DET flip-flops are compared to existing DET flip-flops using simulation in a high performance 180 nm CMOS technology and the simulation results done on HSPICE Soft Ware. Finally compare the existing and proposed results in terms of delay and power consumption, design of master slave dual edge triggered flip-flop.

Index Terms - **HSPICE Tool, Micro-wind and Digital schematic.**

I. INTRODUCTION

DUAL EDGE triggered (DET) flip-flops achieve the same data rate as single edge triggered (SET) flip-flops at half the clock frequency, which can lead to reduced power dissipation of synchronous logic circuits [1], [2]. The cost of this reduction is higher circuit complexity of DET flip-flops which usually have more transistors and more internal nodes than SET flip-flops. A common DET flip-flop design called the Latch-MUX DET flip-flop [1], [9] has two input latches multiplexed to one output. The two latches are level-triggered by opposite clock levels so that there is always a transparent latch that follows every change at the input. As a result of this transparency, glitches at the input have an adverse effect on the flip-flop's power dissipation. It was estimated in [2] that Latch MUX DET flip- flops dissipate less power than SET flip-flops only when glitches are rare. Other DET flip-flop designs include pulsed DET flip-flops [1], [3], [4]. Generally, a pulsed DET flip- flop works by making its output latch transparent to the input signal after every clock edge for a short time interval that is sufficient to reliably latch the input value. Power dissipation of these flip-flops is less dependent on input signal transitions in between the clock edges at the cost of increased power dissipation due to clock activity.

This paper presents novel static DET flip-flop designs that use C-elements. The paper consists of five sections. Section II presents five novel DET designs including the low-glitch-power LG_C flip- flop, implicit-pulsed IP_C flip-flop, floating-node FN_C flip-flop, and two high-performance conditional- toggle CT_C and CTF_C flip-flops. Section III describes simulation setup and the comparison methodology that is used to compare the presented flip-flops against each other and against six previously reported DET flip-flop designs. Section IV presents and discusses the results of extensive Monte Carlo and voltage scaling simulations.
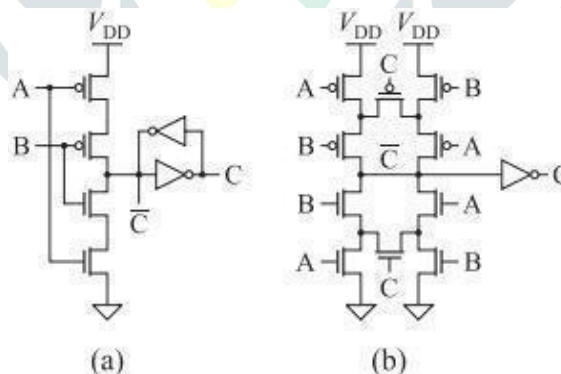

Fig. 1 Transistor-level implementations of a C-element (a) The weak- feedback. (b) The symmetric [6] implementations.

A C-element, introduced in [5], is normally a three-terminal device with two inputs and one output. When all of its inputs are the same, the output switches to the value of the inputs; when the inputs are not the same, the previous output value is preserved. This device acts as a latch which can be set and reset with appropriate combinations of signal levels at the input. The two transistor-level implementations of C-elements that are used in this paper are shown in Fig. 1. Other implementations have been considered but have not been found to improve on performance, power, or circuit size when compared to the implementations in Fig. 1. C-elements and variations of their circuit topologies are the building blocks of the novel DET flip- flops presented below.

II. LITERATURE SURVEY

Increasing circuit speed is certain to remain the major goal in the future logic design evolution. Predictions in technology and performance scaling [1] indicate that the technology itself is not likely to provide required performance improvement, thus a portion of the performance is expected from circuit design innovations. More specifically, the timing overhead of the storage elements is supposed to decrease from today's roughly three fan-out-of-four delays (3 FO4) to about 1.5 FO4. In addition, innovations in clocking subsystem are needed to reduce its power consumption relative to the total power. The break-up of high-performance processor power consumption shows about 30%– 50% power spent for clocking only, in high-performance

processors, [2], [3]. These innovations are particularly important as the power consumption of high-end systems grows exponentially over time, with less and less efficient heat removal and no apparent technology solution in the near future.

Frequency scaling involves additional difficulties if the clock frequency continues to follow the trend predicted by the roadmap for the following years (3–5 GHz). With clock period reduced to 200 ps, the importance of clock uncertainties will increase, and complex multiple-phase clocking will become impractical due to increasingly large timing uncertainties and power consumption.

In order to save on clocking power, dual-edge triggered (DET) clocking strategy uses DET storage elements (DETSE) that capture the value of the input after both rising and falling clock transitions. Otherwise, DETSE is nontransparent, i.e., it holds the captured value at the output. Thus, the DET clocking strategy provides a one-time solution to the frequency scaling by retaining the data throughput of single-edge triggered (SET) clocking at halved clock frequency. However, in order to fully exploit the power savings in the clock distribution network, this approach must ensure that the delay and energy consumption of DETSE must be comparable to those of SET storage elements (SETSE). Furthermore, use of both clock edges to synchronize the operation makes timing sensitive to clock duty cycle and increases clock uncertainties generated by the clock distribution system. DET systems have been studied in the past decade [4]–[8]. However, the emphasis of virtually all previously published papers was on the circuit design of the storage elements. The consistent definition of timing and energy metrics was lacking, as well as an estimate of the effect that a dual-edge clocking has on a system power, which is a basis for a fair comparison between DET and SET strategies.

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. During recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data. Power dissipation is an important parameter in the design of VLSI circuits, and the clock network is responsible for a substantial part of it (up to 50%). When the supply voltage is decreased the speed of the logic circuits might be diminished due to reduction in effective input voltage to the transistors.

Mostly without accurate power prognostication and enhance tools the design for low power issues can't be overcome . So calculate the power dissipation in digital circuit it necessary to use certain tools during the design to meet the power constraints to avoid the costly redesign effort. Edge triggered flip-flops are most used synchronous digital circuits. D-type flip-flop's is the basic building blocks in modern VLSI systems and it showing benefaction a important part of the total power dissipation in digital system[12]. In synchronous VLSI circuits the total clock related power consumption is done by the power consumption in the clock circuits, clock buffers, and the flip-flops [3]. There are many factors where the Power consumption is dependent, as $P = \alpha\ C\ f$ [5] here the power is proportional to the square of the voltage.

To reduce power consumption the voltage scaling is the most effective way. Also voltage scaling is associated with threshold voltage scaling which can be creating leakage power to increase exponentially. By using double-edge triggered flip-flops (DCETFFs), the clock frequency can be significantly reduced ideally, cut in half while preservative the rate of data processing. The DCETFF design is valuable saving energy both on the distribution network (by halving the frequency) and flip-flops. It is preferable to reduce circuits' clock loads by minimizing the number of clocked transistors.

III. EXISTING TECHNIQUES

Extensive simulations have been performed to compare the five presented DET flip-flops against each other and also against six previously reported DET flip-flop designs. Two versions of the novel FN_C flip-flop have been considered: The version presented in Fig. 10 and the version with the symmetric C-element of Fig. 1(b) replacing the weak-feedback output C-element. The latter version is denoted as FN_C (sym) in the comparison. For a fair comparison, all flip-flops include input, output, and clock buffering.

Fig. 2 shows transistor-level schematic diagrams of the six previously reported DET flip-flop designs that are considered in this paper for comparison. The designs are as follows: LM, described in [9], is a variant of a common Latch MUX DET design; EP is a variant of the common Explicit-Pulsed DET flip-flop that was introduced in [4]. LM_C is a Latch-MUX design, introduced in [7], that uses a C-element at the output to perform the function of a MUX. TSP, presented in [10], is the True-Single-Phase Clock DET flip-flop design that follows the Latch-MUX approach but does not use the inverted clock signal. CP, introduced in [1], is the Conditional Precharge DET flip-flop. f) IP, described in [3], is the Implicit-Pulsed DET flip-flop.

The flip-flops were implemented in the 28 nm GF 28HPP CMOS technology. Implementations were optimized for minimum energy-delay product. For the optimization step, the delay metric was the maximum CK-Q delay because it is straightforward to measure. Optimizations were performed by the simulation tool in an automated fashion: The tool varied transistor sizes within the specified bounds and chose the best sizes for each flip-flop after a number of iterations. The search bounds were chosen so that resultant designs would meet recommended design rules most of the time. Weak transistors were allowed to use minimum width rather than the recommended minimum width as it would otherwise result in poor circuit performance.

Simulations were performed on schematic designs. Conservative estimates of layout parasitic were included in the simulation models at both the optimization and final simulation stages. These estimates were provided by one of the features of the design kit: The kit can automatically include its own estimation of the RC parasitic interconnect network into schematic simulation models. Parasitic extraction and post layout simulations were also performed on selected designs and were compared to schematic simulations that used automatic estimation of parasitic. Post-layout simulations showed that the kit's estimates for small designs are often conservative and that compact circuits often perform slightly faster in post-layout simulations than in schematic simulations with the automatic parasitic network estimation turned on.

The simulation test bench that is used in this comparison is very similar to the ones used in [3], [11], [12]. The Q output of a simulated flip-flop is connected to a load of four symmetric inverters with their n-type transistors sized at minimum recommended width. The generated data and clock signals are connected to the flip-flop's inputs through two inverters. The clock frequency is 1 GHz, which results in a 0.5 ns cycle time. Most of the measurements relating to energy and delays were taken from Monte Carlo simulations with full global and local process variations enabled. The simulation junction temperature was set to 70 ∘C. For each flip-flop, 2000 Monte Carlo points were simulated. Variations for a number of metrics are reported as coefficients of variation (CV). The CV input, output, and clock buffering. The flip-flops are (a) LM [9], (b) EP [4], (c) LM_C [7], (d) TSP [10], (e) CP [1], and (f) IP [3]. is also known as the relative standard deviation (RSD) which is defined as the ratio between standard deviation (SD) and mean. In this technology, simulation models make somewhat conservative assumptions about sources of variation when performing Monte Carlo analysis on schematic designs. Variations in physical implementations are expected to be lower than the ones reported from these simulations.
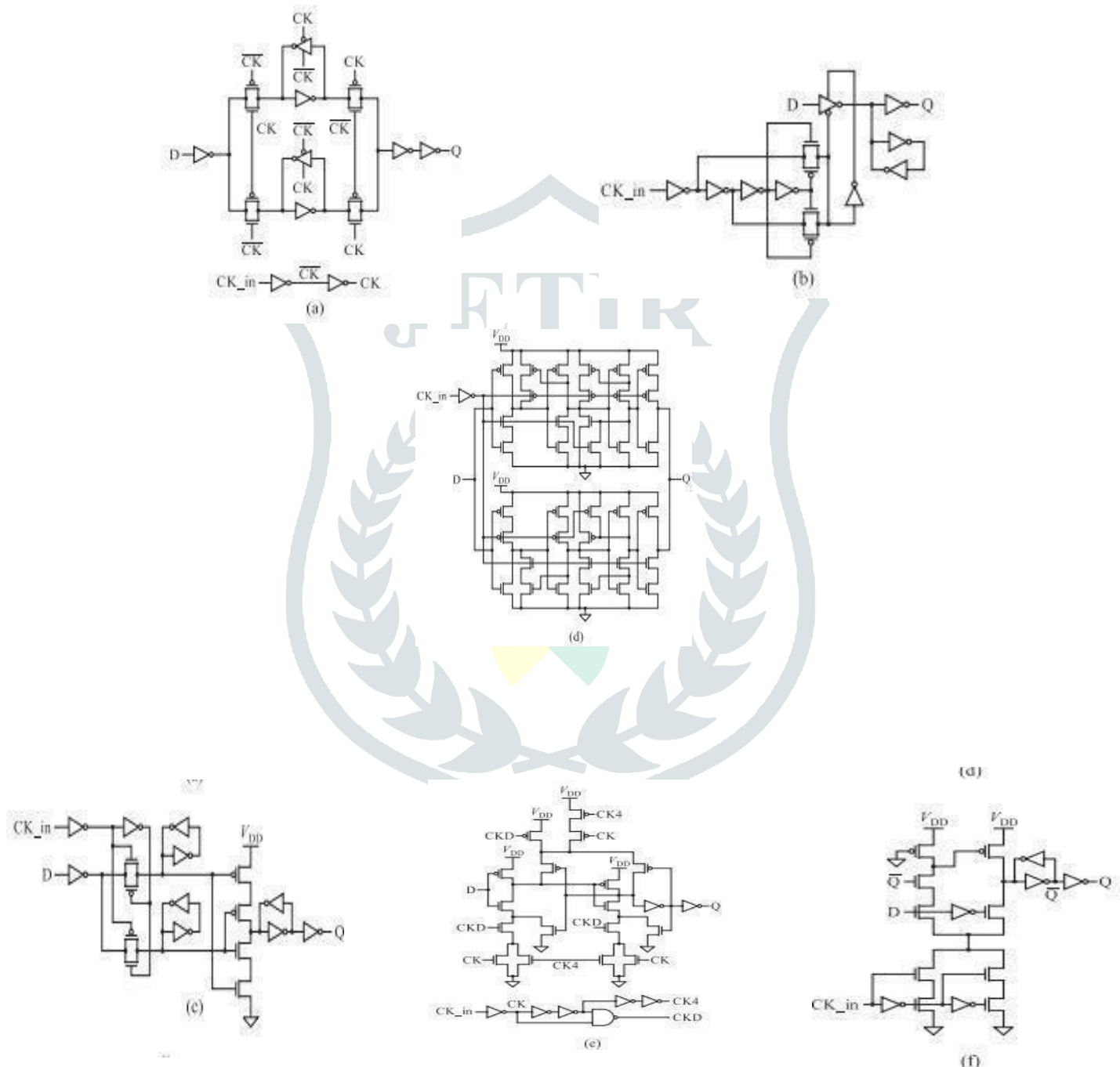

Fig. 2 Transistor-level schematic diagrams of the six previous DET flip-flop designs that are considered in this paper for comparison with the presented novel DET flip-flops. All circuits include input, output, and clock buffering. The flip-flops are (a) LM [9], (b) EP [4], (c) LM_C [7], (d) TSP [10], (e) CP [1], and (f) IP [3].

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The following parameters were evaluated from Monte Carlo simulations.

- Power at 10%, 50%, and 100% switching activities P0.1, P0.5, and P1 respectively.

- Power-delay products PDP0.1, PDP0.5, and PDP1 for each of the three power values with the delay being the D-Q delay.

- Maximum CK-Q delay tcq.

- Worst-case minimum D-Q delay tdq.

The power is measured from the calculated E(t) curve of the total dissipated energy versus simulation time. This curve is computed by integrating simulated power supply, data input, and clock input currents for each simulated flip-flop in the following way:

E (t) = VDD

$$\times \int \left[I_{DD} + \frac{1}{2} \left(I_D + |I_D| + I_{CK\_in} + |I_{CK\_in}| \right) \right] dt. \quad (1)$$

In (1), the power supply current is integrated along with the positive currents flowing into the flip- flop's D and CK_in inputs. Currents flowing out of the flip-flop's inputs are discarded. These negative currents are either the result of a weak feedback inverter working against the D input driver, in which case the current is supplied by the flip-flop and is thus already included in IDD, or are the result of a driver sinking the voltage at the input's parasitic capacitance, in which case this energy was already counted when the driver previously charged this capacitance with a positive current.

Part of the measured energy is dissipated outside the flip- flop's circuit. This includes energies dissipated by the input drivers on driving the flip-flop's inputs and the energy dissipated by the flip- flop on driving the output load. Although the latter depends solely on the size of the load, the comparison is fair in that the load is the same for all flip-flops. The CK-Q delay is measured as the maximum delay between the CK and Q transitions for the four possible cases of CK and Q. For each case, the D transition happens sufficiently early so as not to affect the timing of the Q transition.

The D-Q delay of a flip-flop is generally considered to be a more important metric than just the CK- Q delay [13]: Some flip-flops (e.g., the EP design) allow input changes to be captured well after a clock transition whereas others do not. In this sense, the D-Q delay is the time the flip-flop takes out of the clock cycle. Thus, the D-Q delay is used for PDP calculations in this paper. For every Monte Carlo point, multiple simulations were performed in order to measure the worst-case minimum D-Q delay for that point. There are four possible cases of CK and Q transitions. For each case, a parametric sweep is run with the sweep variable being the timing of the D transition relative to the CK transition. The minimum D-Q delay is found for each of the four cases. For every Monte Carlo point, the worstcase minimum D-Q delay is then the maximum of these four minimums. Fig. 17 illustrates this procedure for a particular Monte Carlo point of the LM flip-flop. For illustration purposes, the step in the D-CK transition sweep variable was set to 0.04 ps. In final simulations, the step was set to 1.25 ps to reduce the number of simulations. For this example, the difference in delays measured with 0.04 ps and 1.25 ps resolutions of the D-CK sweep variable is less than 0.06 ps. Such a small difference is due to the steepness of D-Q vs. D-CK curves reducing to 0 around their minimums

Independent simulations were performed to measure the hold time th of the flip-flops for the typical process corner. For each flip-flop, for all four cases of CK and Q transitions, th was measured as the minimum amount of time D needs to be unchanged after a clock transition so as not to result in the flip-flop failing to latch the correct value, increase the CK-Q delay by more than 40%, or result in a glitch of more than half the VDD voltage. Timings of D transitions were swept with a 0.05 ps step to record the hold time values with a 0.1 ps precision. A separate set of simulations were performed to assess the impact of glitches on the flip-flops' power dissipation. In these simulations, the Q output is steady across clock cycles. The Q-to-Q and Q-to-Q transitions for one glitch are introduced at the D input in between clock transitions. The total dissipated energy is then recorded after the next clock transition including the energy of restoration of the flip-flop's internal states. Energy dissipation due to one and three glitches is measured. The energies are denoted as G1 and G3 respectively. The recorded numbers are averages for the four possible cases of CK and Q. All energy measurements include leakage currents. More precise leakage simulations were performed using dedicated IDDQ models that are provided with the technology kit. The result is reported as IDDQ. The results are averaged across eight cases of D, Q, and CK. The reported values include leakage through D and CK_in inputs and exclude the leakage through the Q output.

IV. PROPOSED TECHNIQUES

The DET flip flop proposed in [1] is exposed in Fig. 3. This flip-flop is basically a Master Slave flip-flop structure. having two data paths. The upper data path consists of a Single Edge Triggered flip- flop implemented using transmission gates. This works on positive edge. The lower data path consists of a negative edge triggered flip-flop implemented using transmission gates. Both the data paths have feedback loops connected such that, whenever the clock is stopped, the logic level at the output is retained. This flip flop has 20 transistors. In these 20 transistors, 10 transistors are clocked transistors.
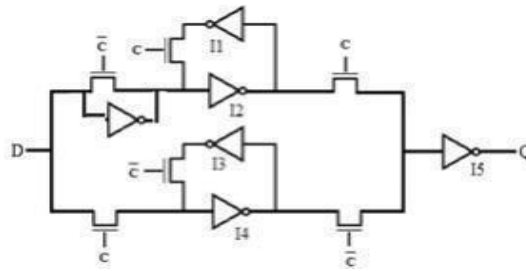
Fig.3: Proposed DEFET in

DET flip-flop proposed in [2] is shown in figure 4. This flip flop is similar to Fig. 1 except that feedback has been changed. On rising edge the upper data path is triggered and on falling edge lower data path is triggered. In the Fig. 4 an inverter and a PMOS transistor are used to hold the logic level when the Transmission gate is closed. When the data value high, the inverter is switch the signal to low, so will be make the PMOS transistor which pull the data up to the high. When value of data is low then the inverter Fig. Fig. 4 Proposed DEFET switch the signal to high, which will isolate the data from VDD and keep the value low.
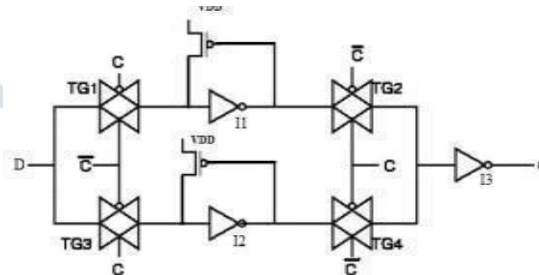
For high output, this type of flip-flop is give static functionality since a PMOS transistor connected to VDD is used in the feedback network, but the static functionality for low output is not provided by this flip-flop. That will make the circuit to behaving like a dynamic circuit.

The proposed Double Edge Triggered Flip-Flop (DCETFF) design is exposed in Fig. 19. The contractual unit of flip-flop is a Master Slave flip flop which consists of two data paths. The proposed flip-flop's operation is same to that of figure 1, but number of clocked transistors is reduced from 10 to 6 by replacing the transmission gates by using n-type pass transistors. The designed circuit using 6 clocked transistors and total 10 transistors. Inverter shown in figure is made by using sub-circuit design. Also W/L ratio is adjusted for making the transistors working in saturation region. Basically, n- type pass transistors give weak high but in figure 3, the n-type pass transistors is followed by an inverter, which results in strongly high. So the proposed DCETFF is free from threshold voltage loss problem of pass transistors in Fig. 5. Therefore the feedback network of Gig. 1 is distorted by replacing
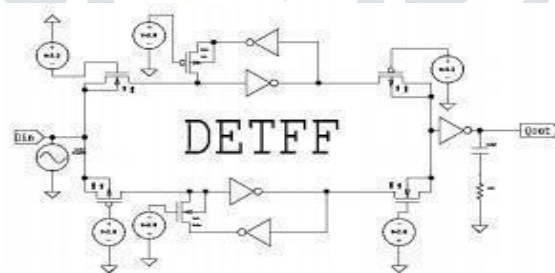

the p-type pass transistor by n-type pass transistor since; the area incurred by NMOS is less than that of PMOS transistor in order to compensate the mobility constraint of NMOS and PMOS transistors. Thus the proposed Design has become more efficient in terms of area, power and speed which showing better performance compare to conformist designs.
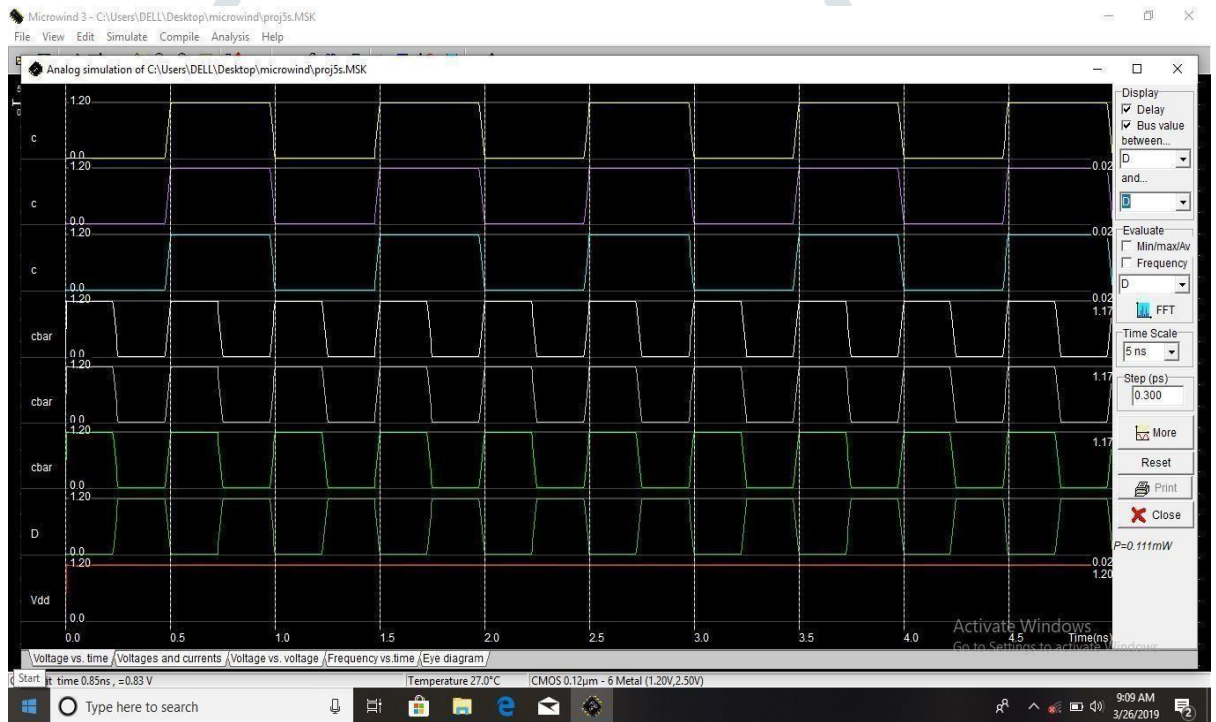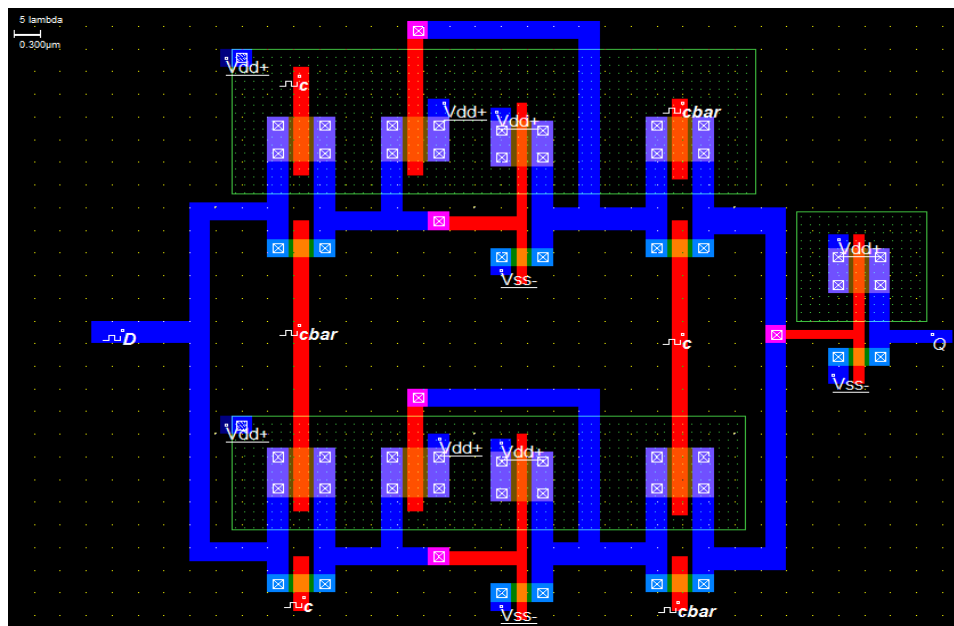
Fig. 5 Proposed DCETFF

V. RESULTS

Fig. 6 Layout for Proposed Technique

Fig. 7 PROPOSED OUTPUT

Table 1 Comparison of performance of Existing and Proposed Technique

PARAMETERS	EXISTING METHOD	PROPOSED METHOD
Voltage	1.8000	1.8000
Current	-236.0294u	-2.4366u
Power	424.8529u	4.3859u
Power Description	424.8529u watts	4.3859u watts

VI. CONCLUSION

Five novel DET flip-flop designs have been presented. The new designs were compared to previous DET flip-flops using simulation in the 28 nm GF 28HPP CMOS technology. The novel LG_C design and its derivatives were shown to significantly improve on Latch-MUX DET flip-flop designs in the area of energy dissipation due to glitches at the input, which makes them useful for designs with large logic depth that are prone to glitching. The novel CT_C and CTF_C designs can be used in high- performance scenarios as they were found to have superior power and power-delay products during periods of high switching activity. Extensive Monte Carlo simulations were carried out to demonstrate that the novel flip-flops are robust under process variations. The new FN_C design was found to be one of designs least susceptible to process variations. Voltage scaling simulations were performed that show that the performance of the presented flip-flops scales very similarly to that of previous DET flip-flops. The DCET flip-flops are simulated with different clock frequencies ranging from 1MHz to 10GHz. Simulation results show that the proposed DCETFF has improvement of 65.61% in terms of average power when compared with DCETFF2. The proposed design also has an improvement of 65.61% and 25.85% in terms of power delay product (PDP) as compared to DCETFF1 and DCETFF2 respectively. The proposed design has minimum average power and lowest PDP than existing designs.

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