Implementation of logic gates using quantum dot cell automata

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Abstract: Quantum-dot cellular automata (QCA) are one of the most promising emerging Nano electronic paradigms used for designing computers and very large-scale integration circuits. Many applications can tolerate the errors and imprecision of digital systems; thus, approximate computing is widely used in such cases. Exclusive OR (XOR) gates are among the major gates, based on which other gates could be developed. A three-input XOR gate is considered to be a basic gate in designing compressors as one of the most important parts of the arithmetic logic unit. Several studies have focused on the accuracy of XOR gate in the QCA technology. However, using approximation in designing XOR gates remains a significant concern in this regard. To the best of our knowledge, the present study is the first to introduce a novel three-input approximate XOR gate. This gate is utilized in designing approximate 4-2 compressors for reducing circuit complexity, which can be achieved by the minimum number of the gates It is a fundamental building block in many circuits, such as adders, comparators, parity checkers, multipliers, error detectors and another kind of circuits as well. In this paper, a new low-complexity single layer XOR gate is presented in QCA technology. Implementation of the gate is based on explicit interaction cell. Hence, it is not required any special equation or technique in its construction. Overall results show that the proposed gate performs better in a case of previous XOR designs.

Index Terms **– QCA Technique, Compressors, Quantum computing.**

I. INTRODUCTION

A cellular automaton (CA) is a discrete dynamical system consisting of a uniform (finite or infinite) grid of cells. Each cell can be in only one of a finite number of states at a discrete time. As time moves forward, the state of each cell in the grid is determined by a transformation rule that factors in its previous state and the states of the immediately adjacent cells (the cell's "neighborhood"). The most well-known example of a cellular automaton is John Horton Conway's "Game of Life", which he described in 1970

In recent years, the complementary metal-oxide- semiconductor (CMOS) technology has been shown to have high power consumption and current leakage. Further- more, it has been associated with numerous problems in making CMOS circuits smaller; such examples are various physical phenomena, the specific mass of each element, and quantum effects that disrupt the normal function of transistors. With this background in mind, researchers have been attempting to develop small-scale technologies with low power consumption and current leakage. Quantum-dot cellular automata (QCA) are an emerging nano electronic technology, which have recently been reported to have a more efficient performance. Although designing QCA circuits is far more challenging than the CMOS technology, there has been growing interest in the simple structure of these circuits, as well as the variety of the methods used for their design and manufacturing. Design of the novel approximate XOR gates has been presented. It also describes the simulation parameters used to verify the design of the proposed model and the evaluation of the results. The proposed models have been verified by their application in designing approximate compressors, and conclusions have been drawn.

Any device designed to represent data and perform computation, regardless of the physics principles it exploits and materials used to build it, must have two fundamental properties: distinguish ability and conditional change of state, the latter implying the former. This means that such a device must have barriers that make it possible to distinguish between states, and that it must have the ability to control these barriers to perform conditional change of state. For example, in a digital electronic system, transistors play the role of such controllable energy barriers, making it extremely practical to perform computing with them.

The major objective of this work is to evaluate and explore the existing 4-2 adder compressor with the modified approach with a focused goal on 4-2 adder compressor performance in addition to less delay, spatial area reduction. The designing of existing and proposed 4-2 adder compressor and results is noted by utilizing the Q- CAD tool. Predominantly less delay in addition to the reduce the number of quantum cells is the main intention of this work. Furthermore, the design is made in such a way it must reliable as well as should have less in complexity. Since aless number of quantum cells are put into operation in the small area and the delay is reduced. The modified architecture of 4-2 compressor circuit is designed using Q-CAD tool and corresponding layout are obtained.

A QCA cell consists of four quantum dots and two electrons, which can move freely among the dots. The electrons are placed at the maximum possible distance from each other due to the Coulomb repulsive force, so that the stable states occur when the electrons fill the dots diagonally. As shown in Fig. 1, these stable states are called polarizations. Two polarizations of +1 and −1 demonstrate the logical values of one and zero, respectively.

Nowadays, the enormous increase in the number of transistors in a single chip, furthermore the reduction of the size of the transistors is an essential challenge for the design of the integrated circuits and in the VLSI technology. The problem is that in this CMOS technology, the size reduction of the transistors is limited and almost impossible beyond 10 nm since it can introduce the abnormal quantum Behavior at the nano-metric scale. In order to overcome this problem, and to obtain high density, the speed with low power consumption Craig Lent and al introduced a new paradigm of the architecture of calculation. This paradigm rises from a series of developments carried out in the years 1980, on the study of systems to a low emerging number of electrons of new capacities in epitaxy allowing the manufacture of gas 2D of electrons by GaAs/AlGaAs. This paradigm is quantum-dot cellular automata (QCA) technology. A number of advantages stem from this new technology. The first is the use of the fundamental states of elementary cells to encode information (Computing with the ground state). As in CMOS technology,

maintaining the ground state requires no external energy input, and is relatively stable. This stability of the ground state can, therefore, be used as memory since once prepared, the cell remains in principle in the ground state indefinitely. A second advantage is that the communication between adjacent cells made by Coulomb repulsion. Inside the automaton, it is not the loads, but the information itself that moves. This eliminates the need to individually control each of the internal elementary cells. This also implies that the energy is supplied to the elementary input cells only and the system, being no longer in its fundamental state, relaxes to the latter. Then the result can be read out. This operation allows a minimum of energy to perform the calculations and minimizes the connections to the cells inside the QCA. Considering that a QCA is composed of only a few input bits for several tens of internal cells, the energy efficiency of a device of this type becomes substantial. QCA technology also has the most advantages in terms of density (1012 devices/cm2), frequency or speed (Range of Terahertz) and especially in terms of energy dissipation (100 W/cm2). At this last term, several works have been carried out on the calculation of the dissipation in various operating regimes.

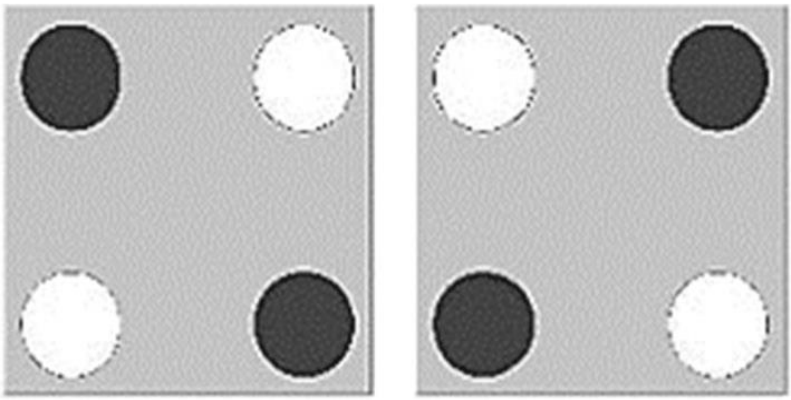

Fig. 1 Two stable states of basic QCA cell (cell on the right: logical one, cell on the left: logical zero)

II. LITERATURE SURVEY

P. Douglas Tougaw and Craig S. Lent Department of Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556 (Received 28 July 1993; accepted for publication 26 October 1993) We examine the possible implementation of logic devices using coupled quantum dot cells. Each quantum cell contains two electrons which interact Coulom bically with neighboring cells. The charge distribution in each cell tends to align along one of two perpendicular axes, which allows the encoding of binary information using the state of the cell. The state of each cell is affected in a very nonlinear way by the states of its neighbors. A line of these cells can be used to transmit binary information. We use these cells to design inverters, programmable logic gates, dedicated AND and OR gates, and non-interfering wire crossings. Complex arrays are simulated which implement the exclusive-OR function and a single-bit full adder.

NURIDDINSAFOEV, JIN-SEONG LEE, JUN-CHEOL JEON Department of Computer Engineering, Kumoh National Institute of Technology, Gumi, Korea. The exclusive-OR(XOR) function is extensively used in microprocessors. It is a fundamental building block in many circuits, such as adders, comparators, parity checkers, multipliers, error detectors and another kind of circuits as well. In this paper, a new low-complexity single layer XOR gate is presented in QCA technology. Implementation of the gate is based on explicit interaction cell. Hence, it is not required any special equation or technique in its construction. Overall results show that the proposed gate performs better in a case of previous XOR designs. The proposed design can be effectively realized in any more complex circuits, such as arithmetic and logic unit of QCA microprocessors.

Dharmendra Kumar, Debasis Mitra Department of Information Technology National Institute of Technology. Bhargab B. Bhattacharya Advanced Computing and Microelectronics Unit Indian Statistical Institute. India Abstract Design paradigms of logic circuits with Quantum-dot Cellular Automata (QCA) have been extensively studied in the recent past. Unfortunately, due to the lack of mature fabrication support, QCA-based circuits often suffer from various types of manufacturing defects and variations, and therefore, are unreliable and error-prone. QCA-based Exclusive-OR (XOR) gates are frequently used in the construction of several computing subsystems such as adders, linear feedback shift registers, parity generators and checkers. However, none of the existing designs for QCA XOR gates have considered the issue of ensuring fault-tolerance. Simulation results also show that these designs can hardly tolerate any fault. We investigate the applicability of various existing fault-tolerant schemes such as triple modular redundancy (TMR), NAND multiplexing, and majority multiplexing in the context of practical realization of QCA XOR gate. Our investigations reveal that these techniques incur prohibitively large area and delay and hence, they are unsuitable for practical scenarios. We propose here realistic designs of QCA XOR gates (in terms of area and delay) with significantly high fault-tolerance against all types of cell misplacement defects such as cell omission, cell displacement, cell misalignment and extra/additional cell deposition. Furthermore, the absence of any crossing in the proposed designs facilitates low-cost fabrication of such systems.

III. EXISTING LOGIC GATE DESIGNING

QCA Designer is a layout and simulation tool for Quantum-Dot Cellular Automata developed at the ATIPS laboratory at the University of Calgary. Many of QCA Designer features can be intuitively discovered without the aid of a manual. This manual will be brief and to the point. Although still a relatively new area of research, nanotechnology has attracted many of the top researchers around the world. Much of the new interest in nanotechnology is a result of the significant increase in capability of fabrication.

The leading semiconductor industry analysis groups such as the International Roadmap for Semiconductors (ITRS) report a significant acceleration in the increase of fabrication capability. The ITRS has changed its prediction of the physical gate

length of MOS transistors by 2005 from 60nm in 1999 to 32nm in 2000. Many researchers see this as an opportunity to begin research in nanotechnology that they may not have considered earlier.

As a result, many new technologies for computing have emerged recently. As well, many researchers predict the possibility of a significant slowdown in the advancement of MOS technology at Nano-scales. At such scale quantum phenomena can no longer be simply averaged out and quantum effects begin to take control of transistor function. Many nanotechnology researchers feel that these problems will not result in a slowdown of advancement in electronics but rather in an opportunity for novel technologies. To date, CMOS circuits have a monopoly on the microelectronics industry, and most are quite comfortable with this well-established technology. Some of the technologies with most potential are Quantum-dot cellular automata (QCA), resonant tunneling diodes, and carbon Nano-tubes.

One of the two fundamental building blocks of each QCA circuit is the inverter. Fig. 1 (on the left) shows the basic QCA inverter gate. In this gate, the signal enters from the left and divides into two QCA wires, which will merge eventually. Complement of the entered signal is calculated at the merge time and released to the right. In fact, as a result of the Coulomb force, the stable state of the output in this structure is the complement of the input.

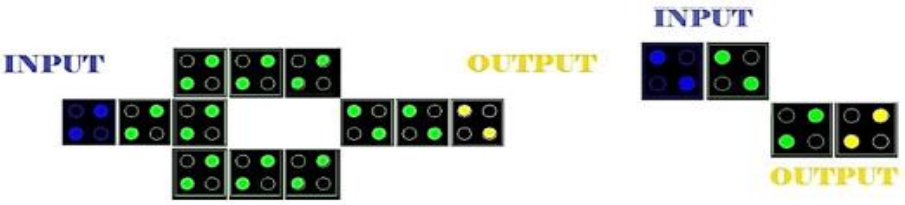

Fig. 1 layout design of not gate

Another fundamental building block of a QCA circuit is the majority gate. Due to the programming capability of this block, the gate can be used to design various structures. The three-input majority gate consists of three inputs, an output, and a work cell. The work cell will be polarized based on the majority polarizations of the cells, as well as the repulsive force among the three input cells

Logical function of this gate is presented as follows.

$$M(A,B,C) = AB + AC + BC$$

According to the logical function of the majority gate, if the constant value of −1 (representing logical zero) is assigned to the input cell *C*, it will function as the two-input AND gate

$$M(A, B, 0) = AB + (A)(0) + (B)(0) = AB$$

Additionally, if the constant value of +1 (representing logical one) is assigned to the input *C*, it will function as the two-input OR gate $M(A, B, 1) = AB + (A)(1) + (B)(1) = A + B$ Each QCA circuit is controlled by the clock mechanism. Synchronization of the majority gate is achieved when all the input signals are applied to the circuit at the same clock zone.

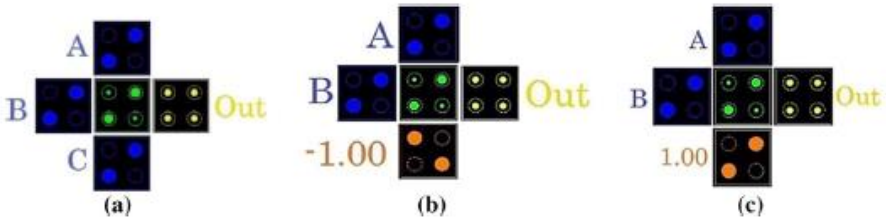

Fig. 2 (a) three-input majority gate in QCA, (b) two-input AND gate in QCA, (c) two-input OR gate in QCA

Approximate computing is a method of computing, the results of which are not accurate. Inaccurate computing leads to further simplified designs, and simplifying the circuits causes their higher performance. Despite an acceptable loss in the precision, other parameters of the circuit can improve, such as the delay, area, and critical path. Loss of accuracy is considered acceptable in numerous applications to decrease the time of producing output result (e.g. machine vision,machine learning, big data analysis, web-based search, and multimedia). However, accurate models and algorithms are not always efficient in the mentioned applications. As these applications are fault-tolerant, it is acceptable for them.

Exclusive OR (XOR) gate is a digital logic gate, the results of which are accurate in the presence of only one accurate input to the gate. If both inputs are accurate (or inaccurate), the results of XOR gate are incorrect. XOR gates have been used in complex functions, such as comparators and compressor. The standard XOR function developed by AND, OR, and NOT gates in the QCA technology is depicted in Fig 5.3Three-input XOR gate in the QCA has other designs with accurate function as well. In this regard, being et a. Proposed a precise three-input model, and the simulation of the proposed gate consists of three three-input majority gates, an inverter, and two two-input XOR gates

$$\text{XOR}(A, B, C) = M[M(\text{NOT}(\text{XOR}(A, B), C, 0), M(\text{XOR}(A, B), C, 1), 1)]$$

Moreover, Shin et al. proposed another design of an accurate three-input XOR gate in the QCA. As is shown in Fig.5.5 this gate consists of three three-input majority gates, two inverters, and two two-input XOR gates.

$$\text{XOR}(A, B, C) = M[M(\text{XOR}(A, B), \text{NOT}(C), 0), M(\text{NOT}(\text{XOR}(A, B), C, 0)$$

In 2014, Navi et al. proposed a design of a three-input XOR gate based on a full adder, in which the output sum of a full adder was used as the output of the XOR gate. This design consists of a three-input majority gate, a five-input majority gate, and an inverter. As is depicted in Fig.5.4(b), the mentioned design has fewer gates compared to the previous models, while the delay and number of cells are also less than the other three-input XOR gate designs In 2016, Kumarand Bhattacharya presented a fault tolerant three-input XOR gate. As can be seen in the schematic view in Fig.5.3, this model consists of three input majority gates and two NOT gates.

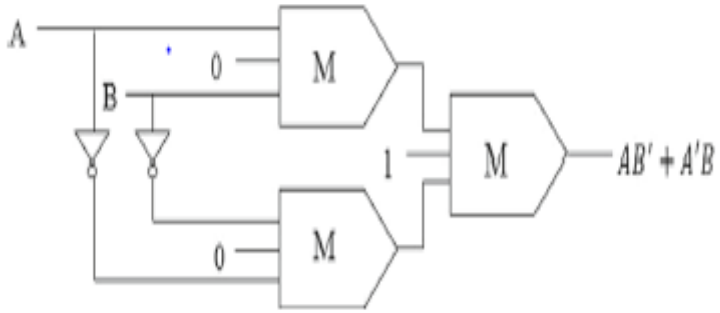

Fig. 3 QCA diagram of three input accurate XOR gate

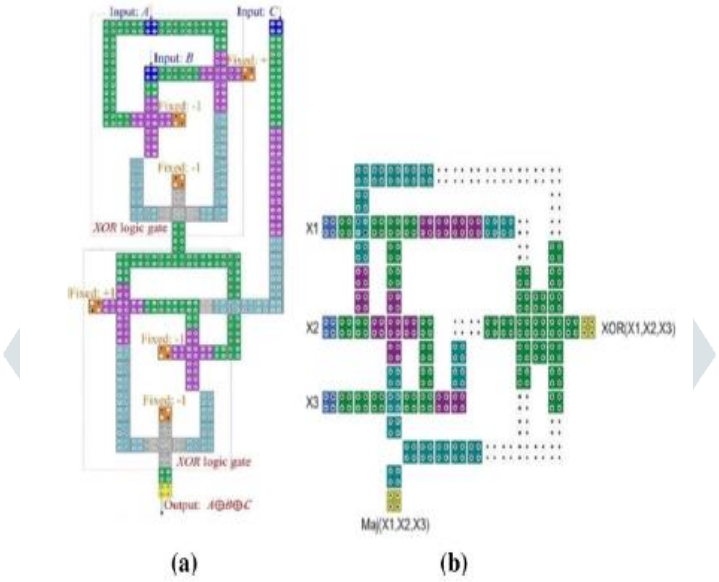

Fig. 3 three input accurate xor gates a)beigh at el b)navi at el

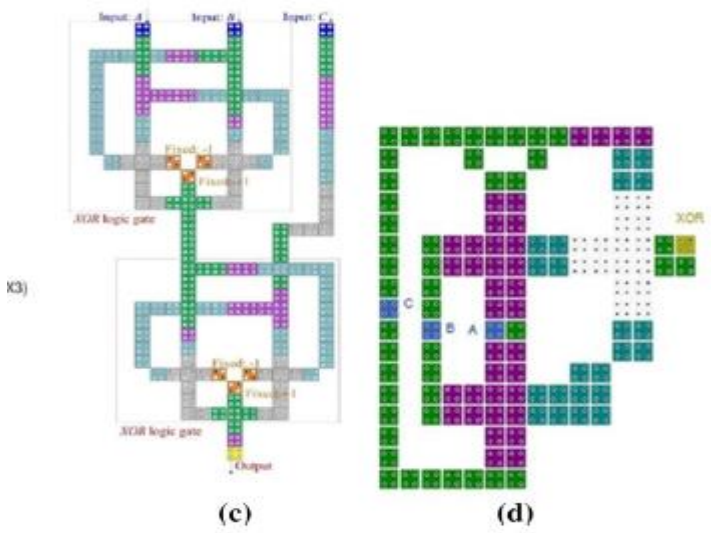

Fig. 4 a)shin at el b)bhattacharya

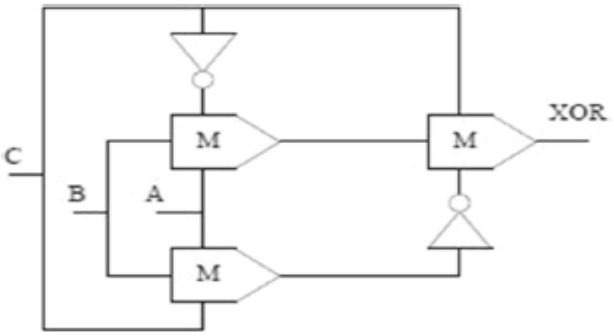

Fig. 5 schematic view of fault tolerant three input xor gate

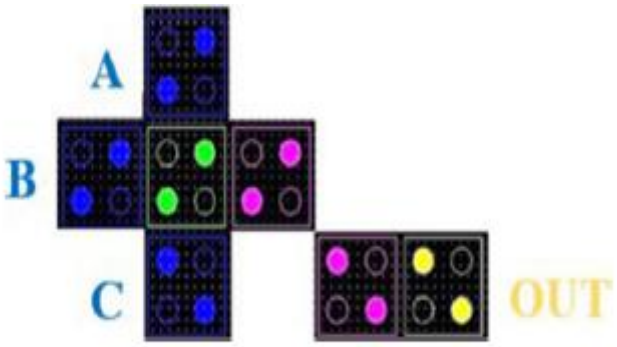

Fig. 6 QCA diagram of three input approximate xor gate

Circuit delay is associated with the complexity of a circuit in certain aspects. Maximum delay occurs as the longest path from the input to the output (i.e., critical path) contains more cells. Lower delay in the critical path indicates the lower cost function with this background in mind, the QCA cost function could be presented, as follows:

Cost = Area × Delay × Complexity, the area is determined in μm2, the delay is based on the clock cycle, and the complexity is based on the number of cells. In the current research, the proposed approximate three input XOR consisted of seven cells, three of which were the inputs and one was the output. According to the simulation results, delay of the circuit was 0.75 clock cycle, and the area was calculated to be 0.01μm2. Furthermore, the cost function was calculated for the design, and the cost of the proposed model was calculated to be 0.0525. The approximate five-input XOR consists of 10 cells, in which there are five input cells and one output cell. According to the simulation results, delay of the circuit is 0.25 clock cycle, and occupied area is 0.006μm2, using proposed approximate XOR gates in compressors, Compressors are widely used in computer arithmetic, especially in the arithmetic logic units (ALUs). An *n*-2 compressor receives n input bits and produces two output bits. The common structure for compression is 3-2, which is known as a full adder (FA). An FA has two inputs and one input carry, and as a result, it produces an output, which is the sum of the inputs and a carry output. The sum of the inputs and output carry are calculated based on, respectively.

$$\text{Sum} = \text{XOR}\ (A, B, C)$$
$$\text{Carry} = \text{OR}\ (\text{AND}(\text{XOR}(A, B), C), \text{AND}\ (\text{NOT}\ (\text{XOR}(A, B)), A)) \quad (10)$$

As is clearly seen in, the sum of the three inputs is equal to their XOR. The approximate three-input XOR can be used to build an approximate FA. The truth table of an exact 3-2 compressor as can be seen, there are two inaccurate outputs from eight different inputs. Moreover, the output carry of the approximate 3-2 compressor has no difference with the exact compressor. Therefore, the error rate of the carry is 0%, which is considered to be optimal. The schematic view and QCA design of the approximate FA based on the proposed approximate three-input XOR.

In order to produce the sum of the inputs, an approximate XOR gate with 25% error rate should be used. The required time for producing the sum is 0.75 clock cycle. In addition, the carry is produced in the previous clock zone since it can be built by the output of, there are two approaches to implement a 4-2 compressor. Typically, the implementation of a 4-2 compressor uses two FA blocks. In order to design an approximate 4-2 compressor,

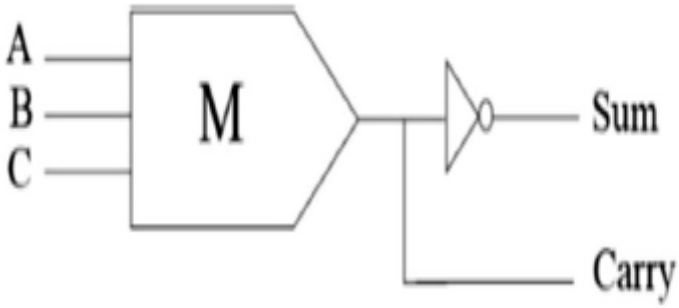

Fig. 7 schematic view of three input approximate xor gate

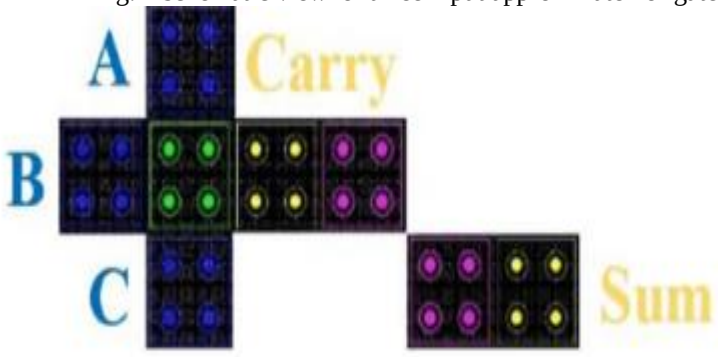

Fig. 10 QCA design of proposed approximate three input xor gate

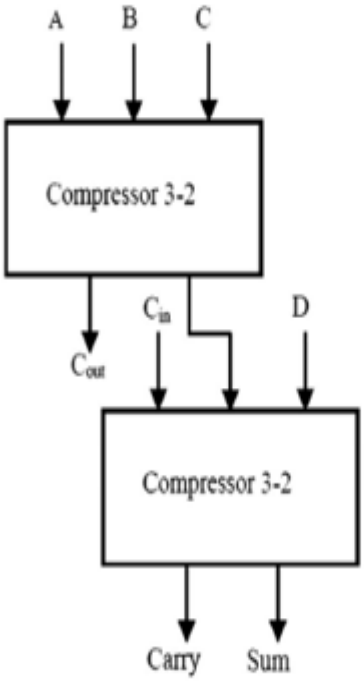

Fig. 11 Block diagram of 4-2 compresser based on 3-2 compressers

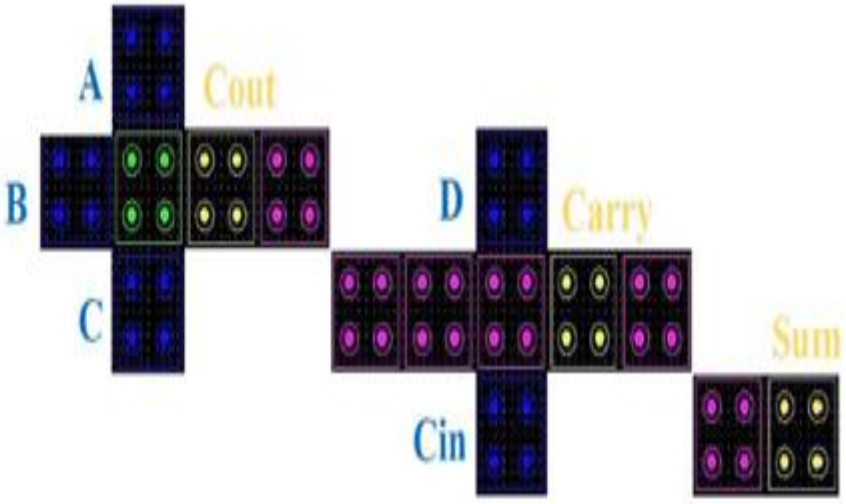

Fig. 12 QCA design of 4-2 compressor based on 3-2 compressor

The Cout is produced in clock zero, the carry is produced after 0.5 clock cycle, and the sum of the inputs is produced with 0.75 clock cycle delay. The truth table of the approximate 4-2 compressor based on the proposed approximate 3-2 compressor is demonstrated in Table 4.

A	B	C	D	C_{in}	Exact 4-2 compressor			Approximate 4-2 compressor using proposed approximate compressor 3-2					
					Sum	Carry	Cout	Sum		Carry		Cout	
0	0	0	0	0	0	0	0	1	×	0	✓	0	✓
0	0	0	0	1	1	0	0	0	×	1	×	0	✓
0	0	0	1	0	1	0	0	0	×	1	×	0	✓
0	0	0	1	1	0	0	1	0	✓	1	×	0	×
0	0	1	0	0	1	0	0	1	✓	0	✓	0	✓
0	0	1	0	1	0	0	1	0	✓	1	×	0	×
0	0	1	1	0	0	0	1	0	✓	1	×	0	×
0	0	1	1	1	1	0	1	0	×	1	×	0	×
0	1	0	0	0	1	0	0	1	✓	0	✓	0	✓
0	1	0	0	1	0	1	0	0	✓	1	✓	0	✓
0	1	0	1	0	0	1	0	0	✓	1	✓	0	✓
0	1	0	1	1	1	0	1	0	×	1	×	0	×
0	1	1	0	0	0	1	0	1	×	0	×	1	×

Table 1 truth table of approximate 4-2 compressor based on approximate 3-2 compressor

A	B	C	D	C_{in}	Exact 4-2 compressor			Approximate 4-2 compressor using proposed approximate compressor 3-2					
					Sum	Carry	Cout	Sum		Carry		Cout	
0	1	1	0	1	1	0	1	1	✓	0	✓	1	✓
0	1	1	1	0	1	0	1	1	✓	0	✓	1	✓
0	1	1	1	1	0	1	1	0	✓	1	✓	1	✓
1	0	0	0	0	1	0	0	1	✓	0	✓	0	✓
1	0	0	0	1	0	1	0	0	✓	1	✓	0	✓
1	0	0	1	0	0	1	0	0	✓	1	✓	0	✓
1	0	0	1	1	1	0	1	0	×	1	×	0	×
1	0	1	0	0	0	1	0	1	✓	0	×	1	×
1	0	1	0	1	1	0	1	1	×	0	✓	1	✓
1	0	1	1	0	1	0	1	1	×	0	✓	1	✓
1	0	1	1	1	0	1	1	0	×	1	✓	1	✓
1	1	0	0	0	0	1	0	1	×	0	×	1	×
1	1	0	0	1	1	1	0	1	✓	0	×	1	×
1	1	0	1	0	1	1	0	1	✓	0	×	1	×
1	1	0	1	1	0	1	1	0	✓	1	✓	1	✓
1	1	1	0	0	1	1	0	1	✓	0	×	1	×
1	1	1	0	1	0	1	1	1	×	0	×	1	✓
1	1	1	1	0	0	1	1	1	×	0	×	1	✓
1	1	1	1	1	1	1	1	0	×	1	✓	1	✓

Table 2 truth table of approximate 4-2 compressor based on 3-2 compressor

The proposed design for the approximate 3-2 compressors used to produce the sum of the inputs and carry bit. Out of 32 different inputs for the sum, there are 14 incorrect answers compared to the accurate design, which indicates an error rate of 43.75%. According to the information in Table 4, the output carry of the approximate 4-2 compressor differs from the exact one in 16 answers, which indicates an error rate of 50%. For the output Cout, there are 12 different answers compared to the exact model, which indicates an error rate of 37.5% [30–37]. Propagation of error can be noted clearly in the cascaded approximate 3-2 compressor. Simulation results are illustrated in Fig. 16. As is shown in Fig. 12, the delay of the circuit is 0.75 clock cycle with the area of 0.03μm2. Quantum cost function of the proposed approximate 4-2 compressor using the

IV. IMPLEMENTATION OF PROPOSED METHOD

The XOR operation with three inputs is an inherent element in designing several digital computing subsystems, such as adders and compressors. Approximate XOR gates can be used in designing approximate compressors with lower delay and number of cells. These approximate designs are associated with lower complexity for fault-tolerant applications In the present study a three-input approximate XOR gat has been proposed using a three-input majority gate and an inverter *A*, *B*, and *C* are the inputs that enter the majority gate, and the output of the majority gate propagates through the NOT gate. In addition, the output of the NOT gate is the result of the proposed approximate XOR. The truth table in this regard is presented in Table

$$XOR\ (A, B,C) = NOT\ (M\ (A, B,C))$$

Results of the proposed approximate XOR in Table demonstrate two incorrect answers when all the inputs are low and high, which means that there are two false answers in eight different inputs, indicating an error rate of 25%.

An approximate five-input XOR gate has been introduced in the following section, which consists of a five-input majority gate, Schematic view of the proposed model is and the QCA design of the proposed gate is depicted in Fig. Other five-input majority gates can be used in the design of this approximate gate as well, while the current design was selected for the lower number of the cells to optimize the design. The truth table of the accurate and approximate five-input XOR gate is presented in Table 3. Approximate

$$XOR(A, B,C, D, E) = M\ (A, B,C, D, E)$$

Table 4 clearly demonstrates the difference between the accurate and approximate output for five-input XORgate.As shown, there are 10 incorrect answers, indicating the error rate of 31.25%.

Table3 truth table of proposed approximate three input xor Gate

A	B	C	XOR	Proposed approximate three-input XOR	
0	0	0	0	1	x
0	0	1	1	1	✓
0	1	0	1	1	✓
0	1	1	0	0	✓
1	0	0	1	1	✓
1	0	1	0	0	✓
1	1	0	0	0	✓
1	1	1	1	0	x

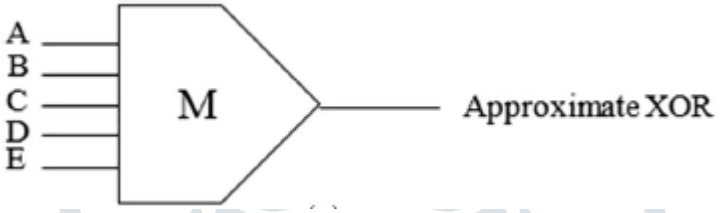

Fig. 13 schematic of 5 input xor gate

Table 4 truth table of approximate five input xor gate

A	B	C	D	E	XOR	Proposed approximate five-input XOR	
0	0	0	0	0	0	0	✓
0	0	0	0	1	1	0	×
0	0	0	1	0	1	0	×
0	0	0	1	1	0	0	✓
0	0	1	0	0	1	0	×
0	0	1	0	1	0	0	✓
0	0	1	1	0	0	0	✓
0	0	1	1	1	1	1	✓
0	1	0	0	0	1	0	×
0	1	0	0	1	0	0	✓
0	1	0	1	0	0	0	✓
0	1	0	1	1	1	1	✓
0	1	1	0	0	0	0	✓
0	1	1	0	1	1	1	✓
0	1	1	1	0	1	1	✓
0	1	1	1	1	0	1	×
1	0	0	0	0	1	0	×
1	0	0	0	1	0	0	✓
1	0	0	1	0	0	0	✓
1	0	0	1	1	1	1	✓
1	0	1	0	0	0	0	✓
1	0	1	0	1	1	1	✓
1	0	1	1	0	1	1	✓
1	0	1	1	1	0	1	×
1	1	0	0	0	0	0	✓
1	1	0	0	1	1	1	✓
1	1	0	1	0	1	1	✓
1	1	0	1	1	0	1	×
1	1	1	0	0	1	1	✓
1	1	1	0	1	0	1	×
1	1	1	1	0	0	1	×
1	1	1	1	1	1	1	✓

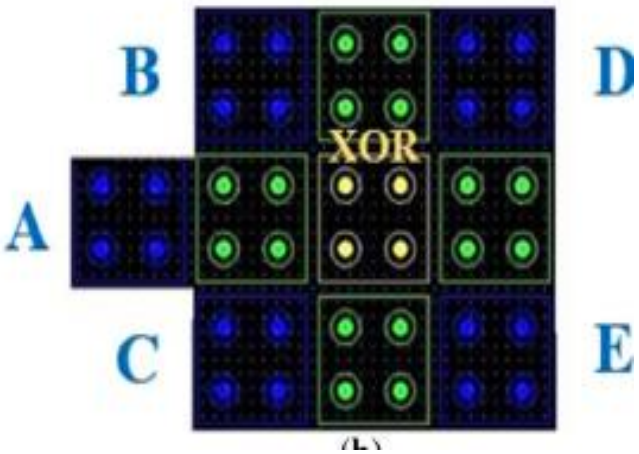

Fig. 14 QCA design of approximate five input majority gate

Evaluating the designs in which approximate computing has been used is possible by other parameters than circuit parameters, such as the pass rate and error rate. The pass rate shows the probability of correct outputs, and the error rate represents the probability of incorrect outputs In the present study, the pass rate of the proposed approximate three-input XOR gate was 75%, and the error rate was 25%, which is considered to be an acceptable rate of incorrect answers in the approximate computing. Moreover, the pass rate of the proposed approximate five-input XOR gate was 68.75%, and the actual error rate was 31.25%. Although this error rate is relatively high, it could be acceptable in some applications (e.g., multiplication filters in image processing). On the other hand, some circuit parameters are noticeable in designing QCA circuits. One of the advantages of the QCA compared to the earlier technologies is the small size of the circuits. The proposed quantum cost function has a direct correlation with the area of a circuit. Additionally, the complexity of a QCA-based circuit is determined based on the number of the cells used in a QCA circuit. As the number of the cells in a QCA circuit increases, the polarization of each cell will depend on a higher number of cells. Also, in most cases, increased number of the cells causes the design to use crossing wires and become layered. With this background in mind, the design of circuits will become more complex. Power is one of the important parameters in the evaluation of QCA circuits. Undoubtedly, power has a direct correlation.

V. SIMULATION RESULTS

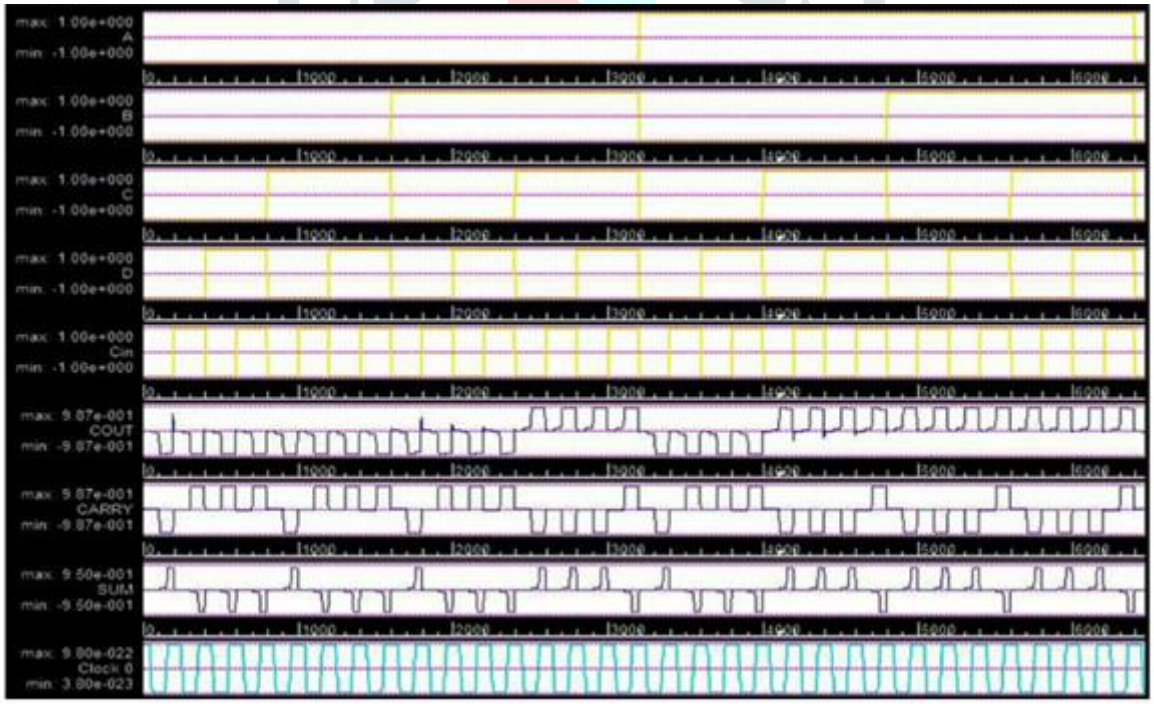

Fig 6.11 simulation of proposed 4-2 compressor

IV. CONCLUSION

XOR gates are one of the most important components used in designing several computing subsystems, such as compressors. On the other hand, inexact computing is considered to be an emerging paradigm for computation at the nanoscale. In the current research, a three-input XOR gate and a five-input XOR gate were presented based on the approximate computing using the QCA technology. To the best of our knowledge, this was the first study in this regard. The proposed models were used in designing approximate 3-2 and 4-2 compressors, respectively. Furthermore, the accurate XOR gates in the QCA technology were evaluated. The proposed approximate XOR will be used in designing approximate *n*-2 compressors and cascading them in order to achieve approximate compressors with more inputs in future studies in this regard. In this paper, A QCA cost function was also introduced based on the important parameters in a QCA circuit. The proposed approximate three-input XOR gate was observed to have a lower number of cells, delay, and area, as well as an accepted error rate. Although the approximate five-input XOR gate has a lower number of cells, delay, and occupied area, the acceptance of the error rate depends on its applications.

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