Review Paper on FPGA Implementation of Min-Sum Algorithm for LDPC Decoder

Pooja Zadey
P.G. Student
G.H. Raisoni College Of Engineering
Nagpur, Maharashtra
lndia

Prof. Wani Patil
Department Of Electronics Engineering
G.H. Raisoni College Of Engineering
Nagpur, Maharashtra
India

Abstract : **This paper presents Low-density parity-check codes as error correcting tool at present. By using LDPC (Low-density parity-check codes) decoder, aim to implement on the FPGA (Field Programmable Gate Array) with less complexity. The main propose of this decoding structure to reduce the complexity with the help of node unit which is check node unit (CNU) and the variable node unit (VNU) employing a min-sum algorithm for getting a good result. Here, we used a multiplexed storage structure for storing node message to get the result in minimum slice resources. This LDPC code is based on the Code scheme in 802.11n standards. Therefore it encodes 324 message bit and creates 648 bit encoded message using AWGN channel to pass the message. Hence this designing stages helps such as encoding, channel Additive White Gaussian Noise (AWGN), and LDPC decoder. Therefore we used here a min-sum algorithm for decoding and encoding bit stream. The low-complexity method becomes a research area to achieve the requirements put in future for wired and wireless communication field.**

Keywords— LDPC (Low-density parity-check codes) decoder; Low-complexity implementation; Min-Sum algorithm, Additive White Gaussian Noise (AWGN) channel.

INTRODUCTION

For sending information from transmitter to receiver in communication systems through intermediate communication channel the system must be robust with high reliability. In the real world, this is a difficult task because there exist many errors. Therefore the role of detecting the error and correcting it become very important task while transmitting information. If we are failed to correct received an error there will no use of the received message.

In 1948 Shannon present first noisy channel coding theorem[1], it states for every communication channel, nevertheless, it may be noisy, R represents positive rate, so at this rate errorless information can be transmitted. The important idea of forwarding error coding is to raise the bits of the message with conscious redundancy to introduce in the form of extra checks bits to produce code world for the message. Here forwarding error coding technique used to increase the throughput of the bit message with conscious redundancy to introduce the extra check bits to get the code word for the message stream. In the last decade, the number of practical code technique is used for high rate transmission nearer to the channel capacity. Therefore LDPC and Turbo codes become major representative of this class of codes.

In 1962 Low-Density Parity Check (LDPC) codes were first discovered by Gallagher, and after that in 1946 it rediscovered, therefore it becomes constantly in the centre attention by researchers for error correction codes. In the present era, LDPC codes are used as a block code with a check matrix that means the small number of entries with non-zero in the resent communication standards. In linear decoding system complexity and the minimum distance of Low-density parity-check codes is set to H matrix for the check matrix with parity to represent in a Tanner Graph [2].

In communication systems, throughput and power requirement increasing day by day. In a wireless communication system, wireless standards demand increases instead of wired therefore simultaneously the requirement of throughput above 1Gbps increases. Therefore this demand reached high innovative and adequate methods to design challenges for Low-density parity-check codes (LDPC) codes in future [3].

I.

In a literature survey, the first paper shows how to implement the matrix permutation technique for Low-density parity-check codes (LDPC) to achieve high throughput for decoding with less complexity of hardware for VLSI architecture. This approach of quasi-cyclic Low-density parity-check codes did not meet the requirement of the researchers (QC-LDPC). The second paper of literature survey shows how to implement sum-product or min-sum algorithm for Low-Density Parity Check (LDPC) codes but both required large space for memory and high complexity of interconnection. These algorithms did not fulfil the requirement of low complexity of the interconnection and memory even using Soft-bit-flipping algorithm (SBF). Here also used pipelined architecture technique to increase the throughput for the small area, therefore, these also not reach to desired output for high throughput and chip area for the VLSI design for future requirement even using projective-geometry Low-Density Parity Check (LDPC) codes. The third paper shows the how to achieve low-complexity of design using the high level of an algorithm such as a min-sum algorithm for Low-density parity-check codes (LDPC) for low power and less area, here also found that belief-

propagation (BP) based approach for Low-Density Parity Check (LDPC) codes with the a-min*-min algorithm.

In the methodology used additive white Gaussian noise (AWGN) channel for passing 324 messages bit and creates 648 bit encoded message. Here Low-density parity-check codes (LDPC) decoder, encode the message with the min-sum algorithm to get the exact message bit in row and column processing. Here employed stages such as an encoder. Channel white Gaussian noise (AWGN), and Low-density parity-check codes (LDPC) decoder. At the time of transmitting the message of a large bit stream of encoding low throughput and lower decoding bit rate occurs and hence here uses the min-sum algorithm for decoding encoded bit stream.

II. LITERATURE SURVEY

In this paper present here quasi-cyclic Low-density parity-check codes. the first paper shows how to implement the matrix permutation technique for Low-density parity-check codes (LDPC) to achieve high throughput for decoding with less complexity of hardware for VLSI architecture. This approach of quasi-cyclic Low-density parity-check codes did not meet the requirement of the researchers (QC-LDPC). [4].

The paper presented, an efficient fully-parallel Network of Programmable Logic Array (NPLA)-based for Low-density parity-check codes (LDPC) codes. Implementation of VLSI technique the LDPC codes are developed in tandem without affecting chip design constraints. Therefore two classes of codes are considered which are combinational objects derived from different sets, non-averaging sequences and based on progressive edge growth techniques. This proposed work reduced the routing complexity. Therefore operating power, delay and chip-size of the circuits were estimated for the better requirement. This LDPC designs modify in such a way to meet widely different requirements like arising in recording systems, as well as wireless and optical transmission devices. Therefore, the proposed multiplier gives high efficient parameter by saving 41% power, less delay by 24% with less area by reducing the slices up to 11.83% and a look-up table (LUTs) by 7.6% when compared to conventional component-based scalable logical architecture (CSLA) based Array Multiplier [5].

In this paper, an improved Low-density parity-check codes (LDPC) Decoding algorithm based on Min-Sum algorithm was proposed which uses a High-performance linear block code which is a type of Low-density parity check code. It is equivalent to Shannon limit. It has low decoding complexity, structure-free and receives extensive attention. For LDPC Low-density parity-check codes (LDPC), Low-density parity-check codes belief-propagation LLR BP algorithm is used for decoding, which is also called a “sum-product algorithm”. Nowadays, LLR BP is the best algorithm. On the other hand, it required complex computation, which causes great more complex hardware designs. To overcome this problem, we have to implement the LLR BP algorithm which is called a min-sum algorithm. The min-sum algorithm reduces complexity and makes design easier. This article analyzes the cause why min-sum is not feet and put into forward an improved algorithm called min-sum linear approximation algorithm based on a min-sum algorithm. Therefore this paper modifies the LDPC decoding algorithm based on a min-sum algorithm. Simulation results show that the new algorithm efficient than a min-sum algorithm [6].

In this paper, employed pulse-width-modulated min-sum (PWM-MS) that is new iterative decoder is proposed in which pulse width-encoded format used for message exchanged [7]. Therefore low switching activity, very low complexity check nodes, low routing complexity, and excellent energy efficiency these advantages achieved by this method. For a (660, 484) regular (4, 15) low-density parity-check code in 0.13 um complementary metal oxide semiconductor (CMOS) with 4-bit quantization, core space 5.76 (mm square) (4.24-mm square area or 556k equivalent AND gates) we implement a fully parallel pulse-width-modulation PWM offset MS decoder. At a signal-to-noise ratio of 5.5 dB, this decoder in post-layout simulation achieves an average information throughput of 5.71 Gb/s and energy consumption of 65.8 PJ/information bit. This paper shows results a 21% reduction in area, a 0.6-dB improvement in coding gain, and energy efficiency improvement of 19% over the bit-serial min-sum (MS) decoder. For improvement of throughput, area and energy the coding gain traded off by the implementation of 3-bit but this is meet the requirement.

This paper contributes a reduced complexity algorithm in the log-domain for LDPC codes (non binary) with long density ratio as a message. For binary codes the MS algorithm used by Extended Min-Sum (EMS) algorithm and has the advantage of performing addition only. The complexity of Extended Min-Sum (EMS) algorithm is O(dcnmq) per check node. The values of nm give near-BP error performance; this complexity is roughly the same as that of the belief propagation fast Fourier transform (BP-FET) decoder except for multiplication and division. By correcting the message along the decoding process, the performance of the BP-FET decoder the EMS algorithm can approach. The Extended Min-Sum (EMS) algorithm then becomes for hardware implementation of non-binary LDPC decoders, therefore the complexity of decoder greatly reduced compared with other decoding algorithms for non-binary LDPC codes and the performance degradation is negligible or small[8].

The message-passing algorithms based on belief-propagation (BP) are used in many applications with decoding error correction codes and solving constraint satisfaction and inference problems. The representation of Bp algorithm is to operate over graph representations called factor graphs that are used to model the input. In many cases, BP-based algorithms give impressive empirical results. Therefore this paper deals with packing and covering integer problems with a constraint matrix is zero-one. The constraint vector is integral, and variables are box constraints. This paper compares the solutions computed by the min-sum algorithm for covering and packing problems to the optimal solutions. After compare with each fractional component, the min-sum also computes multiple solutions or the solution oscillates below and above the fraction. This implies that the min-sum algorithm computes optimal solution if the LP has a unique optimal solution that is integral. The special case of packing and covering problems, this proves that if the LP has a unique optimal solution that is integral and on the boundary of the box constraints after that min-sum algorithm computes the optimal solution in pseudo-polynomial time. The result of this paper unifies and extends recent result for the maximum weight matching problem and for the maximum weight independent set problem [9].

This paper contributes a low-complexity LDPC decoding algorithm with easier check nodes updates. The proposed Min-Sum decoding algorithm gave the result of the second-minimum in check nodes based on the first minimum computation alternatively of enumerating directly. In order to obtain the nearest result, effectively corrected coefficients are exploited, thus the result can reduce the complexity by eject the complicated computations. Complex Analysis is getting and the result mentions that the analysis of the complexity of the calculation of algorithm is abundant lower than the general NMS algorithm and MS-based simplified algorithms. Therefore results show that the enforcement of the computed algorithm can closely match the NMS algorithm with the same number of iterations [10].

This paper present variously reduced complexity min-sum based decoding algorithms for LDPC codes. Here founded new belief-propagation BP-based approach for LDPC decoding and a-min*-min decoding algorithm was presented. For each algorithm complexity, effectiveness, and an average number of iteration are presented [11].

III. METHODOLOGY

It encodes 324 message bit and creates 648 bit encoded message. We are using additive white Gaussian noise (AWGN) channel to pass the message. LDPC decoder decodes the encoded the encoded message by using the min-sum algorithm where it produces the exact message bits by using row and column processing.

Therefore in designing, we are using three stages such as Encoder, channel additive white Gaussian noise (AWGN), and LDPC decoder. Here we are facing problem Convertible LDPC decoders because of the large bit stream of encoded bits result in low throughput and lower decoding bit rate. Our contributed architecture uses the min-sum algorithm for decoding the encoded bit stream.

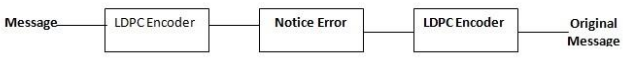

Fig. Original message from encoding

Code Encoder Of LDPC

Code word block length we have supported rate are ½, 2/3,3/4 and 4/5 encoding. The LDPC encoder is systematic, which means it encodes an information block, c=(a_0, a_1, ……, $a_{(l-l)}$), of size k, into a codeword, c, of size n, c=(a_0, a_1, ……, $a_{(l-l)}$, q_0, q_1,……, $q_{(n-k-1)}$), by adding n-k parity bits obtained so that $H*c^T=0$, where H is the parity-check matrix.

Encoding Process

The LDPC encoding process in this proposal is modified from that in 802.11n standard, the encoding process of LDPC Code can be divided into five steps as follows:
calculate the number of present bits, N_{avbits}, in the less number of modulation symbols in which the data field of the packet may set.

Npld = L*8

Where L-length

$$N_{avbits} = N_{CBPS} \times \left\lceil \frac{N_{pld}}{N_{CBPS} \times R} \right\rceil$$

Where
Length Represent the number of octets of user data.
N_{pld} Represent the number of bits of user data.
N_{CBPS} is the coded bit per symbol after modulation. For example, $N_{CBPS}=1$, if FSK or 2-GFSK is used, and $N_{CBPS}=2$, if 4-GFSK is used.
$\lceil x \rceil$ Denotes the smallest integer greater than or equal to x.

IV. CONCLUSION

It encodes 324 message bit and creates 648 bit encoded message. We are using additive white Gaussian noise (AWGN) channel to pass the message. This LDPC Code proposal is mainly based on the LDPC Code scheme in 802.11n standard. The Code Rate, Code Length and Parity Check Matrix in this proposal are same as those used in the 802.11n standard. The encoding process is modified based on LDPC Code encoding process in 802.11n standard. LDPC decoder decodes the encoded message by using the min-sum algorithm where it produces the exact message bits by using row and column processing. Therefore in designing, we are using three stages such as Encoder, channel additive white Gaussian noise (AWGN), and LDPC decoder. Here we are facing problem Convertible LDPC decoders because of the large bit stream of encoded bits result in low throughput and lower decoding bit rate. Our contributed architecture uses the min-sum algorithm for decoding the encoded bit stream.

V. REFERENCES

[1]C. Shannon, "“Certain Results in Coding Theory for Noisy Channels,", *Information and Control*, vol. 1, 1951. [Accessed 1 September 1951].

[2]W. Huffman, "“Fundamentals of Error Correcting Codes,”", *Cambridge University Press, Cambridge UK,*, 2003. [Accessed 1 October 2003].

[3]R. Tanner, "“A Recursive Approach to Low Complexity Codes,”", *IEEE Transactions on Information Theory*, vol. 27, 1981. [Accessed 5 September 1981].

[4]Zhongfeng Wang and K. Parhi, "High performance, high throughput turbo/SOVA decoder design", *IEEE Transactions on Communications*, vol. 51, no. 4, pp. 570-579, 2003. Available: 10.1109/tcomm.2003.810832.

[5]V. Nagarajan, S. Laendner, N. Jayakumar, O. Milenkovic and S. Khatri, "High-throughput VLSI Implementations of Iterative Decoders and Related Code Construction Problems", *The Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology*, vol. 49, no. 1, pp. 185-206, 2007. Available: 10.1007/s11265-007-0054-9.

[6]P. Sebastian, "FPGA Implementation of Min-Sum Algorithm for LDPC Decoder", *International Conference on Trends in Electronics and Informatics ICEI 2017*, vol. 17, no. 978-1-5090-4257-9, pp. 821-826, 2017. [Accessed 1 February 2017].

[7]K. Cushon, "A Min-Sum Iterative Decoder Based on Pulsewidth Message Encoding", *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS,*, vol. 57, pp. 893-897, 2010. [Accessed 11 November 2010].

[8]"Extended MinSum Algorithm for Decoding LDPC Codes over GF(q)", 2015. [Accessed 1 September 2015

[9]G. Even and N. Halabi, "Analysis of the Min-Sum Algorithm for Packing and Covering Problems via Linear Programming", *IEEE TRANSACTIONS ON INFORMATION THEORY*, vol. 61, 2015. [Accessed 10 October 2015].

[10]H. Li, J. Guo, C. Guo and D. Wang, "A Low-Complexity Min-Sum Decoding Algorithm for LDPC Codes", *17th IEEE International Conference on Communication Technology*, vol. 17, no. 978-1-5090-3944-9, pp. 102-105, 2017. [Accessed 17 November 2017].

[11]V. Vityazev, E. Likhobabin and E. Ustinova, "Min-Sum Algorithm-Structure Based Decoding Algorithms for LDPC Codes", *3rd Mediterranean Conference on Embedded Computing*, vol. 17, no. 978-1-5090-3944-9, pp. 102-105, 2014. [Accessed 17 November 2017].