A REVIEW ON MEDIAN FILTER IMPLEMENTATION/ DESIGNING TECHNIQUES

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Abstract: Digital image processing is the advancing technology which performs various operations on the photos, images, video footage etc. The study of different image processing techniques has been performed from 1960 and still continued. The various filters are used for the image processing, one of them is the median filter, the median filter is implemented on hardware by using the different algorithms or designing techniques such as PMU (Partial Median Unit) design, adaptive decision-based algorithm, digital image segmentation using morphological approach, real-time system implementation, etc. this paper provides the review of all the above techniques. The aim of this review paper is to give information of median filter implementation technique emphasizing better performance, low power consumption, less processing time, and high efficiency.

Index Terms - **median filter implementation techniques, PMU design, adaptive decision-based algorithm, types of filters.**

I. INTRODUCTION

Digital image processing treaties with manipulation of digital images through a digital computer, in a similar manner the digital signals are also manipulated using the digital computer. In the modern age, the importance of Digital Image Processing is more clear and accurate. Digital Image Processing has wide applications in almost all the fields which include the medical field, remote sensing, transmission and encoding machine/robot vision, color processing, pattern recognition, video processing, microscopic imaging, etc. Image processing includes image acquisition, filtering etc. there are the various image filtering filters one of them is the median filter. The Median filter is the nonlinear filter frequently used to remove the impulsive noise in image processing, Median filter is the generic filter used to reduce the various types of noises such as speckle noise, salt and pepper noise, additive noise etc. from images and signals also. It is also very essentially used to remove impulsive and Gaussian noise in color images [1]. It is a more robust method than the traditional linear filters, as it preserves the sharp edges of images. Recently median filter is also applied for image "UP-Sampling", and nowadays median filter is combined with the neural network to improve the quality of filtered results. [2]

TYPES OF FILTERS

An Average filter is commonly known as the mean filter as the center pixel value is replaced by the average value. It is also a type of low pass filter, it acts upon the spatial intensity derivatives present in an image and decimates the same. Average filter calculates the average value by performing the convolution. It is easy to use, simple to implement but its results are not accurate. Disk filter is the modified type of average filter.

The Gaussian filter is highly effective for removing the Gaussian noise, highly efficient, and effectively meetings image edge blurring. But it requires more time to filter images in comparison with the other filters. Laplacian filter is widely used in edge detection applications. It allows the easy restoration of fine details of an image, also it is omnidirectional and having fixed characteristics, only it is very much sensitive to noise. LoG filter is a Laplacian of Gaussian filter it gives better filtering at the edges and considers the broader area for filtering. It gives poor filtering response at corners and filtering varies with intensity, are the disadvantages of it.

The working of the Prewitt filter is based on the principle of edge detection; the edge detection is achieved by applying a 3x3 mask. It is a simple to implement and effective for performing the edge detection. As it is much sensitive towards the noise, hence produces inaccurate noise. The working of Sobel filter is based upon Sobel operator which is a discrete differentiation operator. It calculates the gradient of the intensity of the considered image its hardware implementation is simple and effective for performing edge detection, but it is a more complex than Laplacian filter, and post-processing techniques are required for the better response. Unsharp filter is easy to use and effective to perform edge enhancement.
But the use of this will distort the overall image. The working of the Weiner filter is based upon the technique of minimum mean square estimation. it performs pixel-wise adaptive filtering of the considered image. Only it leaves residual noise and slows to apply.

The Median filter is a nonlinear filter, it considers all the neighboring pixel for median value calculation and in this filter, the central pixel value is replaced by the median value. the median value is a more effective statistical parameter as compared to the

mean value, better results can be obtained by increasing the size of filter mask. Its disadvantages are it is highly complex to implement and low size filter mask gives poor results in comparison to mean filter [1]

II RELATED WORK

I have already mentioned that the aim of this project is to provide information on the various algorithm used for implementing various types of median filters, and these are as given below.

A   In this paper the authors Mohammad Ismaeil, Keisham Pritamdas, Kh. Jilen Kumari Devi and Samarth Goyal have proposed an adaptive decision-based algorithm to implement a median filter with efficient hardware for removing impulse noise mainly salt and paper noise, and also proposes hardware implementation of the proposed algorithm for real-time execution on FPGA. In this method, the noisy pixel is detected first by using the concept of the fixed threshold value and then filtered. They have considered the two stages to investigate the performance of filter, at the first stage the image quality, Peak Signal to Noise Ratio (PSNR), and Mean Squared Value (MSE) was computed for different noise signals using MATLAB application, at the 2nd stage the parameters like area, number of slice register, number of LUTs, flip-flops pair, number of bonded IOBs, number of buffers were calculated by using Xilinx vivado 2015 design tool. Also they have designed the proposed architecture in pipeline fashion to minimize the computation time, and parallel processing had been used to accelerate the process, delay blocks to generate the row of window and the median value was evaluated by sorting the odd window pixel values arranging the odd window pixel values, choosing the intermediate value as the median value. By considering the experimental results of filtering operation which was performed on 3 images using a simple median filter and proposed architecture, it was concluded that the proposed architecture gives better PSNR values. The proposed hardware design was implemented on Artix-7 FPGA board of XC7A100T-1csg324c device family using VHSIC Hardware Description language in vivado 2015 design tools. Future works will be implementing a modified threshold based median filter with a better signal to noise ratio with fewer hardware resources. The proposed filter is giving better PSNR quantities in higher noise ratios. The proposed design gobbles up more power due to larger operating speed and pipeline steps. [2]

B.   In this paper, the authors Shih-Hsiang Lin, Pei-Yin Chen Chih-Kun Hsu have proposed a hardware architecture of a median filter constitute of some numbers of submodules which were called as PMUs (Partial Median Filter) arranged in a proper sequence, the partial median value was generated by each unit by considering certain bits from Most Significant Bit (MSB) and Least Significant Bit (LSB). They have divided the 8-bit into two 3-bit and one 2-bit partition and accordingly the median value was evaluated. The proposed design could process huge collection of data providing throughput greater than the other current designs. The proposed filter was comprise of variable combinations and permutations of PMU submodules. Due to this feature, low area and computation time could be attained at the same time. The proposed hardware was bringing about forward by using soft intellectual property methodology, which increases the flexibility of the proposed hardware making it more comfortable to the users. The main drawback of the proposed design was greater power consumption in several intermediate modules. The large power was goggle up by the data buffer used in the design. The less signal transition could be achieved by designing a systematic algorithm at the RTL stage. All the architectures involved in this paper were synthesized using 90-nm process technology in Taiwan Semiconductor Manufacturing Company (TSMC), and the output values were estimated with the output values of other designs, containing bit-level and word-level method. [3]

C.   In this paper, the author Vidya P Korakoppa has described an optimized sorting algorithm for the median filtering process to combat salt and pepper noise in images. This technique calculates the median value by comparing the same column pixel values which are acquired from FPGA parallel, the results of an adjacent window are temporarily stored using D flip-flop. To have a synchronization within designed circuitry circle delay is provided by using two D flip-flop in each comparison process. It can be implemented with ease in real time applications. However, the reduction in comparing times from 21 to 13 is the main factor which enhances the processing efficiency by nearly 40%. The FPGA kit used for the implementation is Spartan 6 LX45. It is cost effective and also powers efficiently since it consumes half the power compared to earlier Spartan Families This technique can also be applied to high-resolution images, which is its main advantage. [4]

D.   In this paper, the authors Lovi Garg, Arushi Garg, Amit Kumar have presented a hardware implementation of the median filter using FPGA. Because of the good denoising power and computational efficiency of the nonlinear median filter, it is most popular and the hardware implementation of the median filter can give better speed by using pipelining and parallelism technique than the software implementation. According to this paper when the median filter is implemented in runtime application, the software implementation does not give good results due to the high computational cost of sorting algorithm as temporal complexity is $O(NlogN)$ for sorting N pixel. Whereas reconfigurable FPGA efficiently allows to reduce the complexity of the algorithm and also simplifies the debugging and verification. They have proposed a new architecture called as sort hardware which is used in the implementation of the median filter. This sort block is used to make computation easy, fast, efficient. The FPGA implementation of this block was carried out by using the Xilinx synthesis tool. [5]

E.   In this paper, the authors M. Ali Altuncu, Taner Guven, Yasar Becerikli, and Suhap Sahin have proposed the real-time image processing algorithm with Hardware/Software Co-design on FPGA. They had considered the real- time working system of the 256X256 image and approximately 40fps were obtained. They have used the convolution coprocessor design for calculation of median pixel value and hardware is implemented on ZedBoard Znyq-7020 FPGA development kit of vivado2014.2. As the Zynq-7000 contains both Artix-7 FPGA and ARM Cortex-A9 processor on the same chip hence it is different from standard FPGA. In such FPGA's the part of design having extreme computations are performed using FPGA and the control part which does not contain computations are simulated by using the software. The complete Zynq system is divided into two parts i.e., the processing system (PS) and Programmable logic (PL). as the PS consist of ARM Cortex A-9, Floating point unit, Memory controller, Gigabyte Ethernet controller, and USB controller hence its working is same as that of a traditional processor. Whereas the PL consist of all structures of a standard FPGA. The PS communicates with the PL through high-performance data-paths, but in this architecture, they have used Advanced Extensible Interface (AXI) which is a modified interface of Advanced Microcontroller Bus Architecture (AMBA) to achieve the communication between PS and PL. The proposed architecture consists of two parts i.e., hardware and software, the image was captured and transferred to the hardware by using software and in the hardware part, the image processing algorithms were applied on the captured image. The input images were taken from the video source and the processed images were viewed on the monitor connected to HDMI which is the output of development kit and the Verilog HDL was used in this study. The convolution coprocessor used in this technique is enough for working on large-scale images hence the future scope of this technique was to work on high-resolution images real-time by using DMA (Direct Memory Access) implementation [6]

F.   In this paper, the authors Mohsen Azizabadi, Alireza Behrad have explained the new pipeline architecture for implementing pre-processing filters which include Gaussian filter, Median filter, and weighted median filter, which is a combination of Gaussian and median filter, as a hardware implementation of filtering algorithms using pipelined and parallel architectures confirm the higher accuracy. As the main part in image processing is how to move the mask over the image, in this architecture they have used the sliding window algorithm in a pipeline fashion. To achieve this, they had used the set of registers and FIFO (First in First Out) blocks FIFO was the just SRAM blocks. As the direct implementation of sorting algorithm on pixel values requires more clock cycles thus in turn increase in latency of the algorithm. They have calculated the median value by first arranging each column values in ascending orders, by arranging each row values in ascending order, then the middle value of diagonal element was the median value of 9 pixel value and the complete operation was carried out in 3 clock cycles. The proposed architecture of weighted median filter computes the median value in 4 clock cycles whereas other's design requires 6 or 7 clock cycles. They have implemented the complete architecture in Verilog HDL and compared the results of software and hardware implementation to calculate the truncation error, and HDL codes were synthesized in an ASIC Digital Design Flow using 65nm CMOS technologies. [7]

G.   In this paper, the authors Anis Boudabous, Ahmed Ben Atitallah, Lazhar Khriji, Patrice Kadionik, and Nouri Masmoudi have described a new efficient HW/SW codesign which was implemented for the VMRHF filter based on SoPC system. they have developed a hardware acceleration portion to achieve better filtering speed, which was later implemented using fast parallel architecture. The hardware part was implemented on single stratix II EP2S60F672C3 FPGA using VHSIC HDL, and software part was implemented on NIOS-II softcore processor embedded in FPGA. They have implemented the software solution in the system on programmable chip context using NIOS-II softcore processor and microClinux as the operating system. HW/SW solution has improved considerably the filtering speed (82 times faster) compared to the software solution. [8]

H.   In this paper, the author Miguel A. Vega-Rodríguez, Juan M. Sánchez-Pérez, Juan A. Gómez-Pulido have presented a new optimized architecture and its implementation using FPGA. They have used the HOT2-XL board to perform implementation, which belongs to Virtual computing corporation. Also, they have used the 32-bit data bus because of that 4 pixel could be read/write in a single clock cycle, assuming each pixel value is of 8 bit, hence the operation of median filter gets accelerated by 4 times. The 9 pixel were read by using 6 words read cycle thus reducing the number of reading operations and performance also get increased. Their proposed optimized architecture consists of 19 basic nodes, each basic node is composed of an 8-bit comparator and two 2:1 multiplexer. They have implemented the proposed architecture using XC4062XLA-09HQ240C FPGA of HOT2-XL board, and performed the image processing operation on the image of 640x480 pixel of 256 grayscales, by using hardware (FPGA) and software (Visual C++). By comparing the results, they reached up to the conclusion that the hardware implementation of median filter gives faster results than software implementation, they got the computation time of hardware implementation is nearly 85 times smaller than the software implementation. To overcome the reconfiguration time of HOT2-XL the board they have used the configuration cache provided by board. By using parallelism techniques like replication and pipelining, reducing the sorting and selection network, reusing common resources, they have achieved the optimized architecture and high real-time performance.

II. ACKNOWLEDGMENT

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