THREE PHASE 7-LEVEL SEMI CROSS SWITCHED MULTILEVEL INVERTER

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Abstract: This paper demonstrates how the reduced harmonic distortion can be achieved for multilevel inverters. The semi cross switched topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels. The modes of operation are discussed for 7-level semi cross switched multi level inverter, as similar modes will be realized for higher levels. Three phase seven level of the proposed inverter topology is simulated in MATLAB/SIMULINK environment and results are presented.

.IndexTerms - Harmonic distortion, multilevel inverter, semi cross switched.

I. INTRODUCTION

Multilevel inverters continue to receive more and more attention because they are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating, low switching losses, high efficiency and low output of Electro Magnetic Interference (EMI). Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference.

Many topologies for multilevel inverters were proposed, the most popular being the diode-clamped [2], [3], flying capacitor [4], and cascaded H-bridge [5] structures, Diode clamped and Flying capacitor MLIs require complex circuitry as number of levels increase.

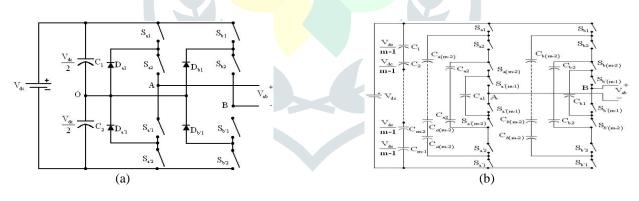


Figure 1. (a)2-Phase Diode-Clamped MLI (b) 2-Phase Capacitor-Clamped MLI

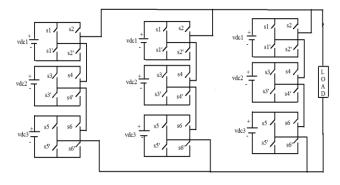


Figure 2. Three phase cascaded H-bridge multilevel inverter.

II. SEMI CROSS SWITCHED MULTI LEVEL INVERTER

In this technique, the number of phase voltage levels at the converter terminals is 2N+1, where N is the dc link voltages or number of cells. For 7-level inverter the number of switches required is only seven i.e S1, S2, S3,S1', S2', S3', S4' Therefore, the number of driver circuits in the proposed system is also only seven and thereby with less switch count compared to existing topologies, gives low switching losses and thereby increase in efficiency[1]. So size and cost of the inverter is reduced compared to cascaded H-bridge multilevel inverter. There are no diodes and capacitors are used in these topologies.

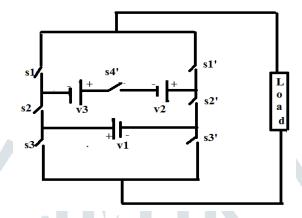


Figure 3. single phase semi-cross switched multi level inverter

Voltage sources V1(100v), V2(100v), V3(100v) are connected as shown figure 4. The switches are operated ON and OFF According to requirements. For example to get +vdc the switches s1,s2,and s3' are in ON state. Similarly same operation for +2vdc, +3vdc, 0, -vdc, -2vdc, -3vdc.

2.1 Modes of Operation

Mode-1:

Mode-2:

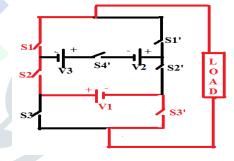
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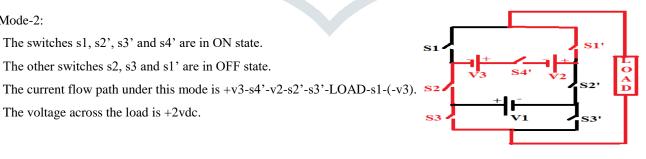
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- The switches s1, s2 and s3' are in ON state. \geq
- The other switches s3, s1', s2' and s4' are in OFF state. \triangleright
- The current flow path under this mode is +v1-s2-s1-load-s3'-(-v1). \triangleright
- The voltage across this load is +vdc. \geq







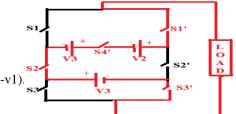
The switches s2, s1',s3' and s4' are in ON state. \geq

The switches s1, s2', s3' and s4' are in ON state.

The voltage across the load is +2vdc.

The other switches s2, s3 and s1' are in OFF state.

- The other switches s1, s2', s3 and s4 are in OFF state. \geq
- The current flow path under this mode is +v1-s2-v3-s4'-v2-s1'-LOAD-s3'-(-v1)
- The voltage across the load is +3vdc.



Mode-4:

- > The switches s1, s2, and s3 are in ON state.
- > The other switches s1', s2', s3', and s4' are in OFF state.
- > The current flow path under this mode is LOAD- s1-s2-s3-LOAD.
- The voltage across this load is 0.

Mode-5:

- > The switches s3,s1' and s2' are in ON state.
- > The other switches s1, s2, s3', and s4' are in OFF state.
- > The current flow path under this mode is(-v1)-s2-s1'-LOAD-s3-(+v1).
- The voltage across this load is –vdc.

Mode-6:

- The switches s2, s3, s1'and s4'are in ON state.
- The other switches s1,s2'and s3'are in OFF state.
- ➤ The current flow path under this mode is (-v3)-s2-s3-LOAD-S1'-V2-S4',-(+V3).
- The voltage across this load is -2vdc.

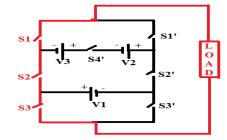
Mode-7:

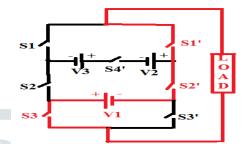
- > The switches s1, s3, s2'and s4' are in ON state.
- > The after switches s2, s1'and s3'are in OFF state.
- The current flow path under this mode is (-v1)-s2'-v2-s4'-v3-s1-LOAD-S3-(+v1).
- The voltage across this load is -3Vdc.

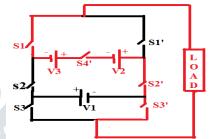
III. SIMULATION RESULTS

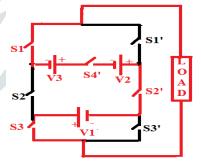
Simulation of three phase 7-level cascaded H bridge multilevel inverter and semi cross switched multilevel inverter with resistive load 1500hms is done in MATLAB/SIMULINK environment.

3.1 Three phase 7-level cascaded H-bridge multilevel inverter









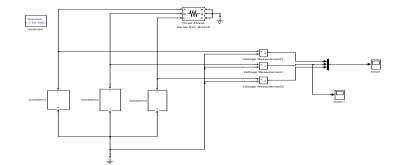


Figure 4. simulink diagram of three phase 7-level cascaded H-bridge multilevel inverter

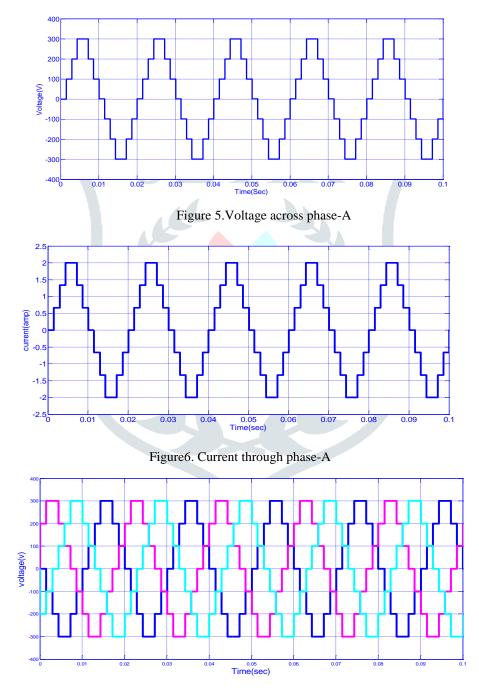


Figure 7. Three phase Voltage.

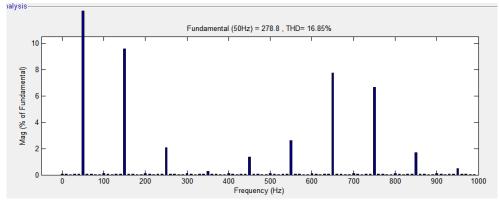


Figure 8. THD analysis of voltage

3.2 Three phase 7-Level semi cross switched multilevel inverter

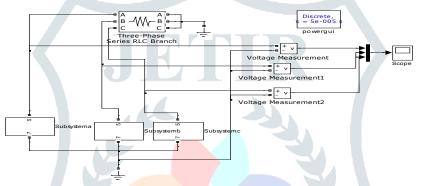
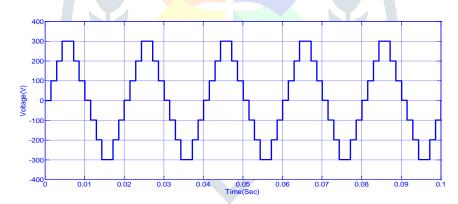
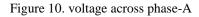


Figure 9. simulink diagram of three phase 7-level semi-cross switched multilevel inverter





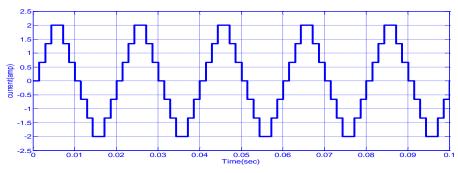


Figure11. Current through phase-A

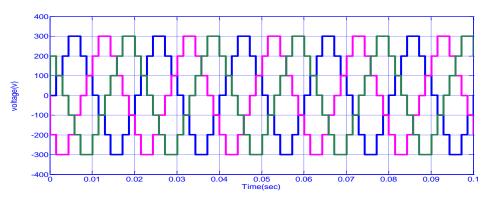


Figure 12. Three phase voltage

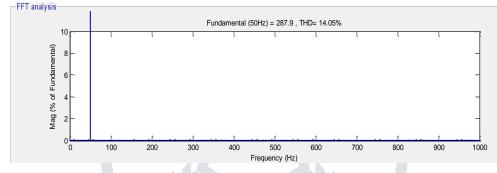


Figure 13. THD analysis of voltage

Conclusion

Simulation of three phase 7- level cascaded H-bridge multilevel inverter and three phase 7-level semi cross switched multilevel inverter is done, plotted voltage and current wave forms. The number of switches and THD of semi-cross switched multilevel inverter is less compare to the cascaded H-bridge multilevel inverter.

REFERANCES:

[1] E.Avinash, L.Jebaraj "A NewVariable Frequency Inverted Sine Carrier PWM Modulated Semi-Cross Switched Multilevel Inverter Topologies" 2016 International Conference on Circuit, Power and Computing Technologies [ICCPCT]

[2] M. Fracchia, T. Ghiara, M. Marchesoni, and M. Mazzucchelli, "Optimized modulation techniques or the gemeralized N-level converter," in proc. IEEE power electronics specialist conf, 1205-1213, Madrid, Spain, 1992.

[3] K. A. Corzine and J. R. Baker, "Reduced parts-count multilevel retifiers," "IEEE Trans. Ind. Electron." vol.49, no.3, pp. 766-774, Aug 2002.

[4]] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," "IEEE Trans. Ind. Applica," vol. 37, pp. 611-618, Mar./April 2004.

[5] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for highpower applications," "IEEE Trans. Ind. Applica," vol. 36, pp. 834-841, May/June 2000.

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