Design of a Multiplexer in Different Logics at Nanometer Regime- A Review

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Abstract : The Low power and low energy has become an important issue in today's consumer electronics. The increasing demand for low-powered devices can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. Combinational circuit can be represented as a several input lines with single output line. Multiplexers are used to design any digital combinational logic circuit. Hence it is required to design a multiplexer with low power consumption and high speed. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style like CMOS, PTL,TG for implementing combinational circuits. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects such as transistor count, power dissipation, and delay become important, disallowing the formulation of universal rules for optimal logic styles. This paper presents study about 2:1 and 4:1 multiplexer with Different Techniques and topologies at Nanometer regime.

Index Terms - CMOS, DPTL , FinFET, Power Dissipation, Speed, Transistor Count.

I. INTRODUCTION

The need for low power ,area efficient and high speed devices has been increasing rapidly. The demand for battery-operated portable gadgets have increased day by day, they need more battery backup which can be achieved only with the low power consumption circuits that are internally designed in them. So energy efficiency has become major concern in the portable electronics devices to get effective performance with small power dissipation. In 1965, Gordon E. Moore predicted that the number of transistors in an Integrated Circuit will double every two years (Fig.1) (widely known as Moore's law). By making transistors in smaller dimensions, more circuits can be fabricated on the silicon wafer and therefore, the circuit becomes economical. The reduction in channel length allows faster switching operations as time required for the current to flow from drain to source is reduced. There are different types of technology advancement in the VLSI design such as 90nm, 65mn, 45 nm etc. These technologies are used to enhance the performance of the circuit in terms of the power, area, delay etc. These technologies depend on the length between source and drain.

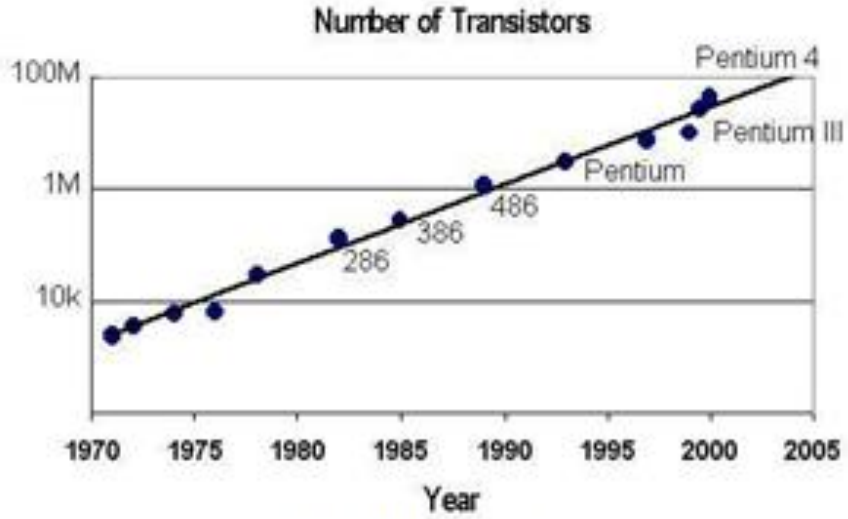


Fig. 1 Moore's Law

II. INTRODUCTION TO MULTIPLEXER

A **multiplexer** or mux is a combinational circuits that selects several analog or digital input signals and forwards the selected input into a single output line. A multiplexer of 2^n inputs has n select lines and are used to select which input line to send to the output.

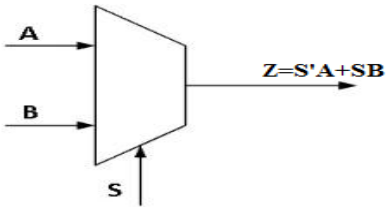
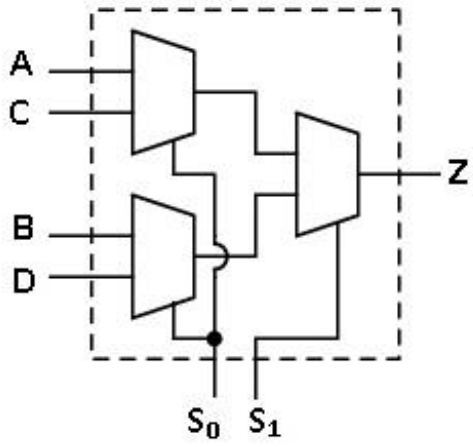


Fig.2: The schematic diagram, Boolean equation and the truth table of a 2:1 multiplexer with inputs *A* and *B*, select input *S* and the output *Z*

S	A	B	Z
0	0	0	0
	0	1	0
	1	0	1
	1	1	1
1	0	0	0
	0	1	1
	1	0	0
	1	1	1

Figure 3 shows how a 4:1 MUX can be constructed out of two 2:1 MUXs.



$$Z = \left(A.\overline{S}_0.\overline{S}_1\right) + \left(B.\overline{S}_0.S_1\right) + \left(C.S_0.\overline{S}_1\right) + \left(D.S_0.S_1\right)$$

Fig3: Implementation of 4:1 MUX using 2:1 MUXs

B. Design using Pass-Transistor Logic (PTL)

A multiplexer can be designed using various logics. Fig.4 shows how a 2:1 MUX is implemented using a pass-transistor logic

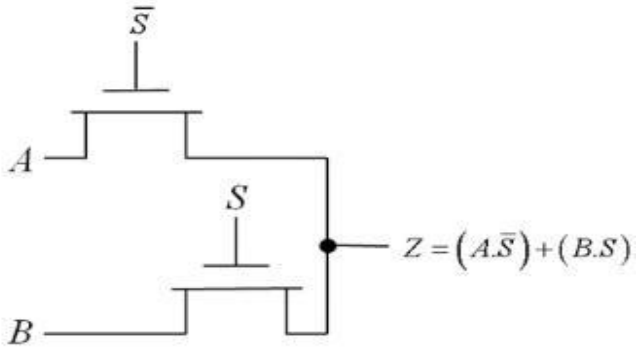


Fig.4. Design of a 2:1 MUX using pass-transistor logic

The pass-transistor logic attempts to reduce the number of transistors to implement a logic by allowing the primary inputs to drive gate terminals as well as source-drain terminals. The implementation of a 2:1 MUX requires 4 transistors (including the inverter required to invert S), while a complementary CMOS implementation would require 6 transistors. The reduced number of devices has the additional advantage of lower capacitance.

C. Design using Transmission Gate logic

A transmission gate (TG) is an electronic element and good non mechanical relay built with CMOS technology. It is made by parallel combination of nMOS and pMOS transistors with the input at the gate of one transistor (*C*) being complementary to the input at the gate ($\bar{C}$) of the other. The symbol of a transmission gate is shown below in fig.5.

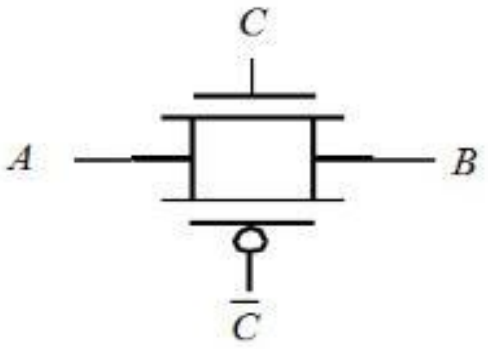


Fig.5: Symbol for transmission gate

The transmission gate acts as a bidirectional switch controlled by the gate signal *C*. When *C=1*, both MOSFETs are on, allowing the signal to pass through the gate. In short, *A=B, if C=1*. On the other hand, *C=0*, places both transistors in cut-off, creating an open circuit between nodes *A* and *B*. Fig.6 shows the implementation of a 2:1 MUX using transmission gate logic.

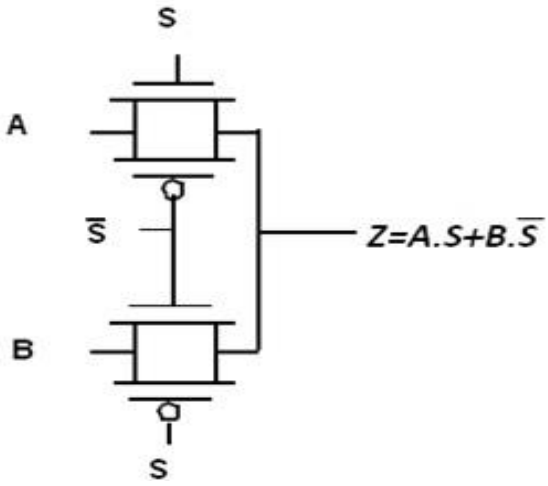


Fig.6: Circuit diagram of a 2:1 MUX using transmission gate logic

Here, the transmission gates select input *A* or *B* on the basis of the value of the control signal *S*. When *S=0, Z=B* and when *S=1, Z=A*.

III. PERFORMANCE METRICES

Multiplexer is a basic circuit for any digital circuit. so a high speed, reduced delay, reduced area and low power consumption will results in effective digital system designs. Thus it is proposed to design a multiplexer with high speed, reduced delays, less area and low power consumption using different logic style in different geometrical devices at nanometer.

1. Propagation delay:

Propagation delay is the time required to complete the operation. The overall propagation delay of a Multiplexer comprises of the delay caused by the transistors and the delay contributed by the interconnect resistance and capacitances. If the Multiplexer is designed using smallest area transistors & less number of transistor then the circuit layout of which requires smaller chip area. The smaller layout area leads to smaller interconnections and reduced propagation delay.

2. Power consumption :

Power consumption is the amount of power used by a circuit. Proposed multiplexer consumes low power because of reduced hardware and reduced delays.

3. Transistor count

Transistor count is the total number of transistors required to design multiplexer. As the number of transistor reduces, power consumption reduces and propagation delay reduces.

IV. RELATED WORK

The author Anugraha Rose V et al.[1] reviewed proposed Design of 2:1 MUX using (a) Static CMOS (b) Pseudo logic (c)Dual Rail Domino logic (d) Domino logic using CADENCE VIRTUOSO SCHEMATIC EDITOR 6.1 at 180nm. The results obtained show that, the Domino logic based 2:1 MUX is the most efficient design because the average power consumption is 20.06% and PDP(Power Delay Product) is 20.1% lesser than that of other logic families.(Table 1)

Name of the logic	No of transistors	Average Power(W)	Delay(s)	Power Delay Product (J)	Area(m)
Static CMOS	12	55.33µ	4.573n	0.253	4.32p
Pseudo NMOS	7	411.5µ	4.561n	1.87	2.52p
Domino logic	**7**	**126.2µ**	**4.5505n**	**0.574**	**2.52p**
Dual Rail domin	14	248.8µ	4.5515n	1.13	5.04p

Table 1

The author Ch.S.Daya Adarsh et al.[2] studied different types of dynamic logic like Complementary CMOS (C2MOS), DCVS Logic, Pseudo NMOS, Domino Logic, Low Power Feed through Logic. And implement 2:1 Multiplexer using both conventional & Double Gate Technology by incorporating different dynamic logic styles. The performance parameters are compared between Conventional Multiplexer and Double Gate Multiplexer which are implemented using dynamic logic styles. The Implementation and Simulation of Low Power Multiplexer using DSCH 2.6F Microwind Tool using 120nm technology. The comparative analysis of both technologies by using dynamic logic styles indicates the reduction of power consumption about 50% and delay is about 25% by using Double Gate for 2:1 Multiplexer. His findings are as per Table 2.

Sr. No.	Logic Styles	Power Consumption	Delay
1	CMOS	125µW	6.5ps
2	DG CMOS	31µW	13.5ps
3	Pseudo NMOS	114µW	5ps
4	C^2MOS	104µW	13.5ps
5	DCVSL	575µW	14.5ps
6	DOMINO	89µW	13ps

Table 2

The author Pragati Gupta et al.[3] worked on design of 4:1 MUX using Nand gate and MOS transistor. Her finding shows that the area of the die is approximately becomes 41% in MOS transistor as compared to the area of fabrication of 4:1 MUX using logic gates.

The author Vikash Kumar Sharma et al.[4] In this paper author has designed and simulated 4:1 multiplexer using conventional and NMOS, TGL, DPTL techniques observe that CMOS has more power dissipation and transistor count than other techniques. His findings are shown in Table 3.

Technique used	Transistor count	Power consumption	Delay
Conventional	36	75.596uW	0.588ns
DPTL	6	2.544nW	0.053ns
TGL	18	12.887nW	0.075ns
NMOS	6	34.544nW	0.0483ns

Table 3

The author Mohit Vyas et al.[5] has worked on 2:1 MUX using CMOS and Proposed Design of FinFET based 2: 1 MUX by using 45nm technology at cadence virtuoso version 6.1 platform which shows the reduction in noise in the circuit is about 60% while the reduction in power consumption and leakage current is about 40% and 50% respectively by using FinFET in place of CMOS.

In this paper the 2: 1 MUX is designed by using FinFET in place of CMOS. The FinFET is used for the reduction in leakage power for performance improvement of the circuit. The working of both design is same but performance parameters are improved. Author's proposed design is shown in Fig, 2.

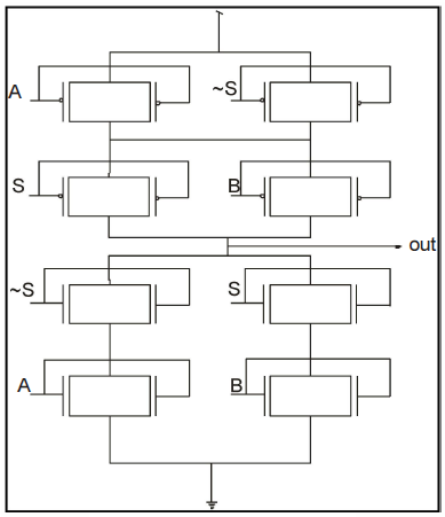


Fig 7. FinFET based 2:1 MUX

The author Anshul Jain et al. [6] worked on 2:1 multiplexer using CMOS, transmission gate, pseudo logic, NMOS pass transistor logic, Pass transistor logic and designed multiplexer using sleep transistor with Tanner tool on 45nm technology and observe that proposed multiplexer has given improvement in power technique for designing of low power, low area Multiplexer but it has high delay as compare to other Multiplexer design. Author's experimental results are as follows.

Logic Style	No. of transistor	Power	Delay
CMOS	12	$2.388x10^{-7}$	$2.79x10^{-11}$
Transmission gate	6	$3.64x10^{-8}$	$5.26x10^{-12}$
Pseudo Logic	9	$2.26x10^{-8}$	4.41×10^{-12}
NMOS logic	4	1.41×10^{-8}	7.17×10^{-12}
Pass transistor logic	6	1.57×10^{-8}	6.94×10^{-12}
Proposed Design	13	1.01×10^{-8}	5.51×10^{-12}

Table 4

The author Ira Parashar et al. [7] designed and simulated 4:1 multiplexer using different low power techniques namely Gate Diffusion Input (GDI), Dual Pass Transistor Logic(DPTL),Adiabatic Logic, Energy Charge Recovery Logic(ECRL), Transmission Gate and also done a comparative study with conventional CMOS design on the basis of Transistor count, Speed, Power dissipation and Area using Cadence tools for simulation. Author observed that CMOS has more power dissipation and transistor count as compared to other proposed techniques. Authors results are as per table 5.

Technique used	Transistor count	Speed	Power Dissipation	Area
CMOS	26	LOW	932uW	MORE
GDI	6	LOW	1.8570pW	LESS
DPTL	6	HIGH	98.655pW	LESS

Table 5

The author B.Dilli Kumar et al. [8] studied performance of 4:1 multiplexer in different low power techniques such as Dual Pass Transistor Logic (DPTL), Gate Diffusion Input (GDI), and Adiabatic logic and their performance is compared with CMOS design. Author found that the adiabatic logic has less power dissipation compared to other design styles and DPTL and GDI has less transistor count compared to other design styles. Comparison shows in table 6

Logic Style	Power Dissipation (p Watts)	Transistor Count
CMOS	408.0268	26
GDI	133.7856	6
DPTL	133.7856	6
Adiabatic logic	26.1855	28

Table 6

V. CONCLUSION

We have reviewed Design of Multiplexers using different Logics with PMOS and NMOS devices in Nanometer to reduce Power Consumption, Delay and Transistor Count i.e. size. . Different technologies are used for implementing the different designs in the global Foundries. The Review has given us a result of various topologies showing decrement in Power Consumption, Delay and Transistor Count i.e. size.

In the future Work we will work on good multiplexer design with optimize parameter at nanotechnology, also work must carried out at different logic style in different geometrical devices like FDSOI (Fully Depleted Silicon Over Insulator), FinFET (A Fin Field-effect transistor) etc. along with PMOS and NMOS at nanometer.

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