RF LOW NOISE AMPLIFIER DESIGN FOR 2.4GHz ISM BAND APPLICATIONS

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Abstract: This paper presents the design and analysis of low power RF low noise amplifier for ISM band wireless applications. Source degeneration technique is using for impedance matching; cascode common source amplifier is for gain improvement. Inductive load is placed at the output of LNA to achieve impedance matching. The LNA achieves the input reflection coefficient(S_{11}) -20.89dB, gain (S_{21}) of 20.42dB, Noise Figure of 0.68dB. The practical input resistance of the proposed circuit is 44.96Ω while consuming 1.53mW static power dissipation at 2.4GHz ISM band frequency.

***Index Terms*:** Cascode Amplifier, Noise Figure, Impedance Matching, Dual Band, Source Degeneration.

I. INTRODUCTION:

A CMOS reconfigurable LNA is implemented using switched inductors and varactors, performs continuous frequency tuning from 2.4 to 5.4 GHz. Switching transistor is used to provide variable gain control over a 12dB-range. The LNA supports standards including Bluetooth, WiMAX [1]. An inductor less LNA was operating in the frequency range between 200MHz and 3.8 GHz to cover the first two WiMAX bands namely 2.5GHz to 2.9GHz and 3.4GHz to 3.6GHz. Its low power consumption as well as its compact size, inductor less, permit portability and make it right for the rapidly developing IEEE 802.16e standard. Another design uses inductive shunt peaking along with the load capacitance to achieve a bandwidth of up to 6.2 GHz to cover the three bands including 5.2GHz to the 5.9GHz band[2]. A low-noise, low-distortion CMOS wide-band amplifier that matches a capacitive source is represented using CMOS technology, optimal noise matching with a capacitive antenna in the entire AM frequency band is possible so that better noise performance is achieved compared with the bipolar realization [3].

The quality factor of passive tuned circuits influences the circuit power dissipation. The use of high-quality inductors in the design of LNA lowers the power dissipated in tuned RF circuits[4]. The strong demand for wireless products, a greedy desire for spectrum that pushes carrier frequencies ever upward, and the constant quest for higher performance at lower power and cost, have recently driven the development of radio frequency integrated circuit (RF IC) technology in unprecedented ways. These pressures are stimulating novel solutions that allow RF ICs to enjoy more of the benefits of Moore's law that has been the case in the past. In addition to regular raw transistor speed increases, the growing number of interconnect layers allows the realization of improved inductors, capacitors, and transmission lines. A deeper understanding of noise at both the device and circuit level has improved the performance of low noise amplifiers[5].

A CMOS low noise amplifier has designed for application in a 3.1GHz to10.6GHz ultra wideband radio-frequency (RF) receiver system [6]. A wideband pass multistage RF amplifier using a cascade of a three-segment bandpass LC section filter with a common gate stage is using for RF front end[6]. Wideband input impedance matching can be obtained using resistive shunt feedback in combination with a parallel LC load to make the input network equivalent to two branches[7]. The complementary topology is merged with unbalanced inductive source degeneration to attain broadband input matching while preserving low noise figure [8].

A 90 nm CMOS low noise amplifier for 3 to 10GHz ultra-wideband (UWB) applications is designed based on a current-reuse technique and performs UWB (3–10 GHz) input matching and cascode amplifier with resonant load is used to improve the gain and reverse isolation [9]. A new technique is used to enhance the ("piggyback boosting") transconductance of the CG LNA by implementing a current-reuse method to reduce the power dissipation by sharing the bias current between the boosting and the UWB signal amplifying stages[10]. An enhanced π match input network is used to achieve wideband input impedance matching as well as high and flat gain [11].

A 1-to-6 on-chip transformer acts as a low noise amplifier with zero power dissipation and high linearity while providing ESD protection and differential outputs [12]. Low power input matching has achieved by implementing an active shunt feedback architecture while the current of the feedback stage is also reused by the input transistor to improve the current efficiency of the LNA. A forward body biasing method is utilized to tune the feedback coefficient [13]. Low noise figure and wideband matching in the subthreshold region has attained by using a gate inductor aided impedance matching and a current-reuse feed forward noise cancellation technique, respectively [14]. An inductor between the gate of the cascode transistor and the power supply combined with a digitally programmable capacitor between the gate and the drain of the cascode transistor facilitate to improve the Third-order Intermodulation Intercept Point (IIP3) of a subthreshold LNA [15].

II. Common Source Cascode LNA:

N_1 acts like an amplification transistor in Cascode LNA with LC load shown in Fig 1. N_2 acts like Cascode transistor. Cascoding increases the output resistance of the circuit and hence the gain. Cascoding provides isolation between input and output. Thus N_1 and N_2 are the same types of amplifiers; therefore the given cascode amplifier can be named as Telescope

Cascode Amplifier. By inserting a simple resistor at the input of the LNA can achieve impedance matching at the input. If Rs =R_1 then $V_{in} = \frac{V_s}{2}$ (i.e.) while placing a signal amplitude becomes half this is undesirable effect at the input and the noise produced at the input due to R1, is amplified by the transistor N1 and it appears at the output. Therefore, resistors are not convenient to place at the input to achieve impedance matching. In common gate topology, the input is applying at the source instead of the gate. By adjusting the bias current in CG topology; hence g_m, the 50Ω input impedance can be achieved. But common gate topology produces higher noise than common source topology. By connecting a resistor (R_F) between drain and gate, the impedance matching can be achieved. But the R_F introduces negative feedback between output and input hence the gain decreases. Source degeneration technique is another alternative to achieve impedance matching.

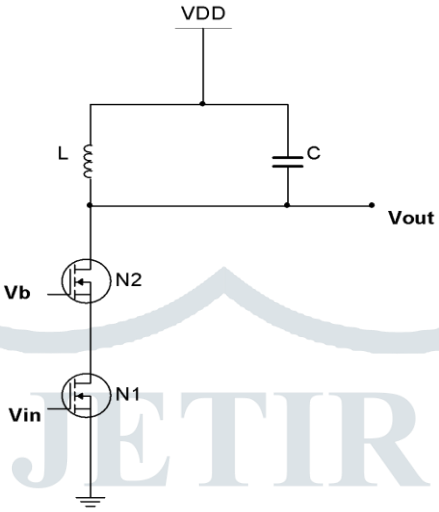

Fig 1: Cascode LNA with LC load

The cascode amplifier with source degeneration technique is shown in figure 2. Hence 'Z' is an unknown passive component. Z may be replaced by a capacitor (or) resistor (or) inductor to achieve impedance matching. The input impedance of the circuit shown in figure 2 has represented in Eqn 1 where g_m is transconductance; C_{gs} is the gate to source parasitic capacitance.

$$Z_{in} = Z + Z\left(\frac{g_m}{j\omega C_{gs}}\right) + \frac{1}{j\omega C_{gs}} \qquad (1)$$

Where 'Z' is source degenerated impedance g_m is transconductance of N_1. When a capacitor replaces z, then the input impedance of the circuit shown in Fig 2 is represented in Eqn 2.

$$Z_{in} = \frac{1}{j\omega C} + \left(\frac{-g_m}{\omega^2 C_{gs}\, C}\right) + \frac{1}{j\omega C_{gs}} \qquad (2)$$

Here $\frac{-g_m}{\omega^2 C_{gs}\, C}$ term gives negative resistance and $\frac{1}{j\omega}\left(\frac{1}{C} + \frac{1}{C_{gs}}\right)$ is the capacitive term. Hence replacing Z with a capacitor is not suitable for impedance matching.

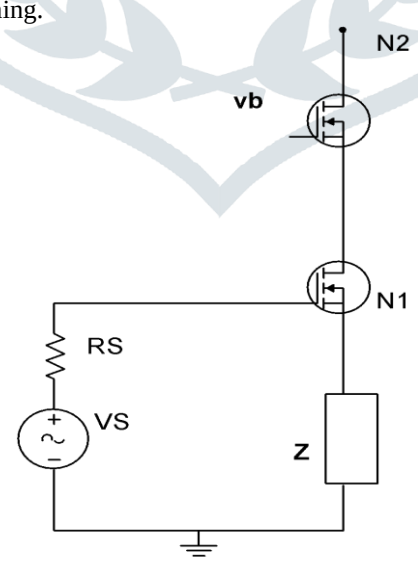

Fig 2: CS Amplifier with Degeneration

When 'Z' is replaced with a resistor, then the input impedance of the LNA shown in Fig 2 can be written as shown in Eqn 3.

$$Z_{in} = R + \frac{g_m R}{j\omega c_{gs}} + \frac{1}{j\omega C_{gs}} \qquad (3)$$

$$Z_{in} = R + \frac{g_m R + 1}{j\omega C_{gs}} \qquad (4)$$

From Eqn 4, Z_{in} is the combination of resistive and capacitive, therefore replacing Z with a resistor is not suitable for impedance matching. Then 'Z' is replaced with an inductor (say Z=Ls) then the input impedance, frequency of operation and input resistance of the LNA shown in Fig 2 can be written as shown in Eqn 5,6 and 7 respectively,

$$Z_{in} = \frac{g_m L_S}{c_{gs}} + j\omega L_S + \frac{1}{j\omega c_{gs}} \quad (5)$$

$$\omega_o = \frac{1}{\sqrt{L_S c_{gs}}} \quad (6)$$

$$R_{in} = \frac{g_m L_S}{c_{gs}} \quad (7)$$

Here Z_{in} is resistive with the input resistance $R_{in} = \frac{g_m L_S}{c_{gs}}$ by choosing proper values of g_m, L_S and C_{gs} the impedance be achieved is R_{in} = 50Ω. Hence the inductance at the source gives possible input matching at resonating frequency; the resultant circuit looks like as shown in Fig 3. The input resistance is set to be 50Ω by choosing the values of g_m from Eqn 8, Ls and C_{gs}.

$$g_m = \sqrt{(\mu_n C_{ox} \frac{W}{L}(2I_{DS})} \quad (8)$$

C_{gs} depends upon the MOSFET device dimensions and frequency of operation. Choose the value of L_s according to g_m and C_{gs}. It is difficult to achieve the desired frequency of operation while maintaining impedance matching. Hence an inductor is placed at the gate of the MOSFET to achieve impedance matching as well as desired frequency of operation as shown in Fig 4.9. Here L_s is an on-chip inductor, and L_g is an off-chip inductor. Now the input impedance doesn't change, but the frequency of operation is changed as shown in below Equation 9.

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \quad (9)$$

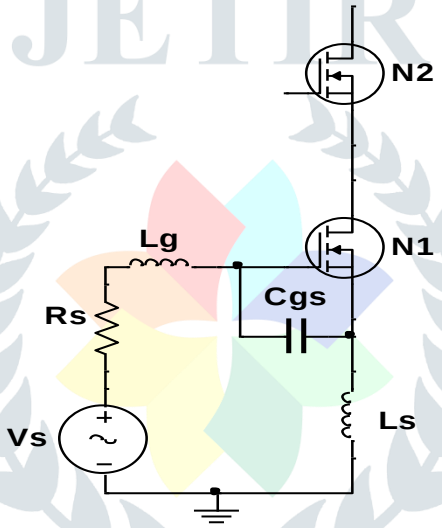

Fig 3: Cascode Amplifier with Gate Inductor & source degeneration

III. Proposed LNA Circuit:

In the proposed LNA is shown in Figure 4, Port 0 is input port where it is the source port. The input signal received from the antenna with resistance 50Ω, C_0 is DC blocking Capacitor that allows only AC signals and blocks the DC signal, Lg is Gate Inductor that acts as an inductor in a series resonant circuit formed at the input side that helps to achieve the desired frequency of operation.

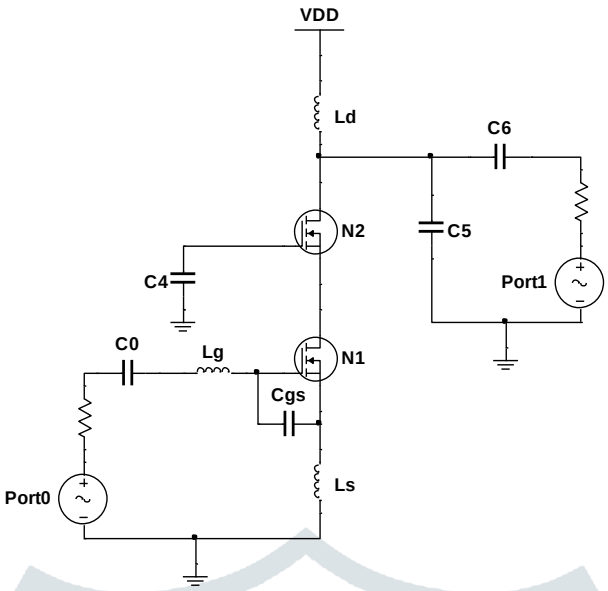

Fig 4: Proposed LNA Circuit

Here R_b is biasing resistor; V_b is DC biasing voltage that is used to bias the transistor N1 since the received source voltage is not sufficient to ON the transistor N1. The N1 acts like common source amplifier that converts the input voltage into current, Ls is source degenerated inductor, it helps in deteriorating the input resistance, to achieve the desired frequency of operation and it is used to produce the impedance matching at the input.

The transistor N2 acts like common gate amplifier that directs the current to pass through the load; it provides isolation between the input and output. Here C4 acts like AC grounding capacitor, where the unwanted AC signal is grounded through this capacitor. Here Ld acts as an inductor in a parallel resonance circuit at the output. It helps to achieve impedance matching at output along with the desired frequency of operation 2.4GHz operating frequency. Here C5 is Noise blocking Capacitor that helps to ground the noise. Here C6 is a coupling capacitor that helps in coupling the output with next stages. The Port 1 indicates the output Port where the output of LNA connected to the next stages

The design values of Proposed LNA circuit are Co = 1nF, L_g = 30nH, R_{in} = 50kΩ, V_{gs} = 600mV, V_{DD} = 1.8V, Ls = 420pH, C_4 = 10pF, L_d = 4nH, Rd = 5Ω, C_5 = 680fF and C_6 = 345fF.The simulation is done by using the above practical values to achieve the frequency of operation at 2.4GHz.

IV. Simulation Results:

The graph shown in Fig 5.4 represents how Input Reflection coefficient is varied with the frequency. In this figure -20.888 dB input signal is reflected from the input, i.e., 1.5% of the input signal is reflected and the remaining 98.5% of the input signal is incident on the circuit.

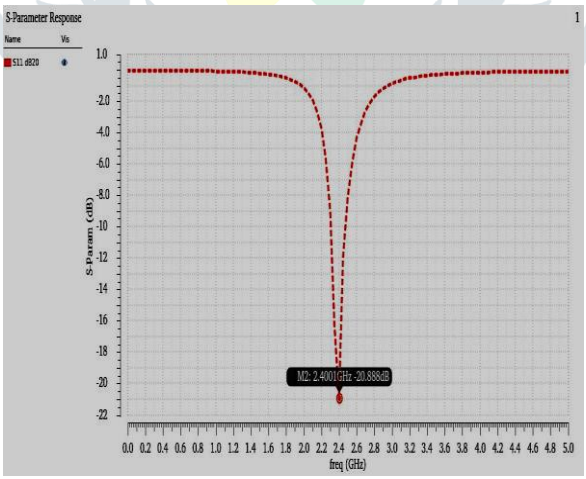

Fig 5: Input Reflection Coefficient (S_{11})

The graph shown in Fig 6 represents how the gain of LNA behaves with the frequency. Here 20.423dB can be achieved at ISM band (2.4 GHz).

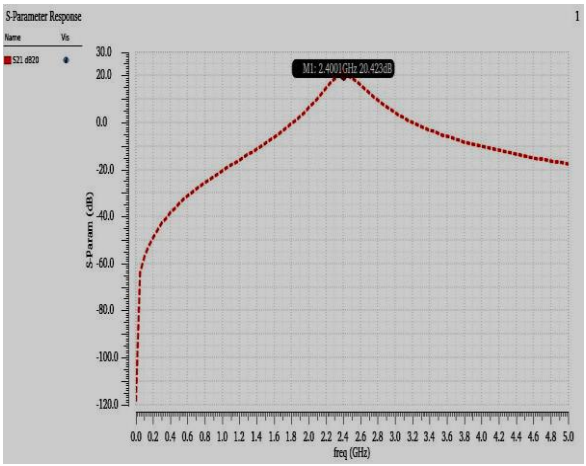

Fig 6: Gain (S_{21}) vs. Frequency

Fig 7 represents the relation among Power Gain (G_P), Transducer Gain (G_T) and Available Gain (G_A). G_P represents the power gain of the circuit.

$$G_P = \frac{P_L}{P_{in}}$$

P_L indicates maximum power delivered to the Load. The P_{in} indicates the maximum available input power. G_A represents the available gain of the circuit.

$$G_A = \frac{P_{av,L}}{P_{av,S}}$$

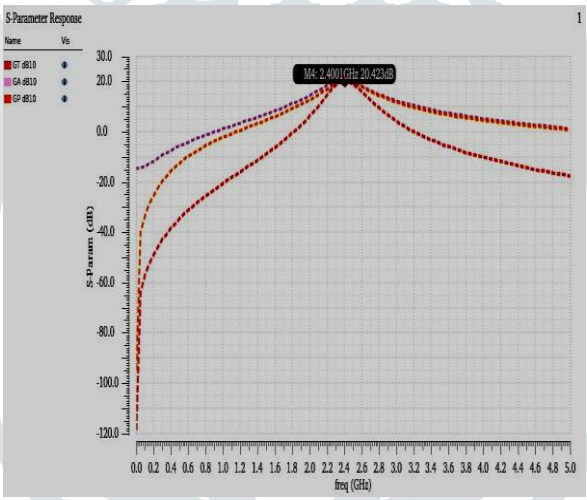

Fig 7: Comparison of Gains vs. Frequency

G_T represents the transducer gain of the circuit. $P_{av,\,L}$ indicates available power at the load. $P_{av,\,S}$ indicates available power from the source.

$$G_T = \frac{P_L}{P_{av,S}}$$

The graph shown in Fig 8, represents how the Noise Figure degrades at different frequencies, particularly at 2.4 GHz frequency. Here 0.68 dB Noise Figure is obtained at 2.4 GHz frequency. At lower frequencies, Noise Figure is high due to flicker noise.

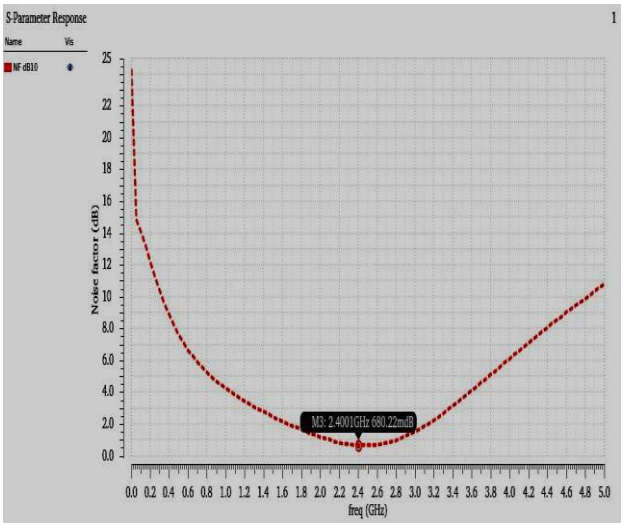

Fig 8: Noise Figure vs. Frequency

The graph shown in Fig 9 represents the relation between input resistance and frequency. Here 44.957Ω input resistance is achieved through this proposed circuit. From the cadence schematic circuit setup, it can write the values of the parameters as shown below. The transistor N1 parameters are $I_{DS1}$is 851.583µA, V_{DS1} is 970.023mV, V_{GS1} is 0.6V and g_{m1} is 12.1412mʊ. The transistor N2 parameters are I_{DS2} is 851.675µA, V_{DS2} is 829.977mV, V_{GS1} is 0.6V and g_{m2} is 12.24mʊ. The static power consumption consumed by transistor N1 is 0.8245mW. The static power consumption consumed by transistor N1 is 0.7055mW, and the total static Power consumption in the circuit is 1.53mW.

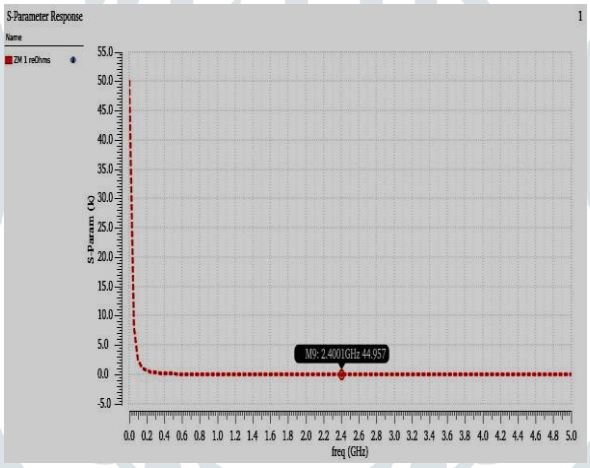

Fig 9: Input Resistance vs. Frequency

V. Conclusion:

The proposed LNA is designed for 2.4GHz Industrial, Scientific and Medical applications. The circuit is simulated in Cadence Virtuoso Schematic Editor using 0.18um technology. The LNA circuit produces very less noise figure of 0.68dB with input reflection coefficient(S_{11}) of -20.89dB, gain (S_{21}) of 20.42dB while consuming 1.53mW static power. In the future, the LNA can also be designed for 5th Generation wireless applications by shrinking the MOSFET technology node.

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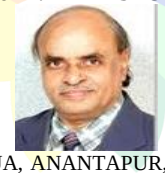

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