A REVIEW ON DESIGN OF 8- BIT RISC PROCESSOR

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Abstract: Based on research survey it is concluded that CISC processor complex instruction are replace by group of simple instruction. In that sense RISC processor is design to execute very simple instruction. It used to reduce the number of space needed, its reliability in preferred design. So nowadays, most of the embedded processor is designed by RISC processor. In this paper we will discuss various study conducted by different researchers to design a RISC processor in more modified ways.

Index Terms - Complex Instruction set Computing (CISC), Reduced Instruction Set Computing (RISC), and Field programmable gate array (FPGA), Universal Verification Methodology (UVM), Parallel Processing RAM (PPRAM), Application specific instruction-set processor (ASIP).

I. INTRODUCTION

From last few decades, electronics industry has achieved a phenomenal growth, due to rapid advances in system design applications and integration technology, number of applications has been increased. The latest current cutting-edge technology resolve any issues like power processing, low bit-rate video, cellular communication. This trend is growing rapidly, in VLSI technology. With the growth and advancement in the field of electronics, those days are not far when every object around us will have a small processor/sensor embedded within itself, invisible us but still communicate with all other devices around us.

Since its "birth" in 1971, embedded processor is commonly used with microcontrollers, whereas, they perform similar functions they integrate with given system in many ways. It ends up in technological advancement of the processor by decreasing the dimension of controller. Reduced instruction set Processor is also a mainframe style strategy to be used. It uses general instructions instead of specialized instructions. They are most cost effective to design. This is advantage of reduced instruction set computer in technological field. So it may be used in variety of application.

Embedded chip is being used in latest technological due to its speed and programmability. Therefore, for innovative style, its processor should match the subsequent characteristics: relatively low cost, flexible, adaptable, fast, and reconfigurable/reusable. Use of FPGA as a design tool is the best solution for this problem. ASICs made-to-order for a selected uses are relatively expensive albeit they provide the most effective performance. DSP based mostly design, on the opposite hand, are less costly and low in power reduction and heat-emission. However, they supply restricted speed for processing. FPGAs are typically slower than ASICs but however has the advantage of shorter time to market, ability to be re-programmed and cheap. It has both the benefit of ASICs and DSPs. FPGA makes system permits for use in various different languages.

II. LITERATURE SURVEY

Jikku Jeemon has exhibited consider an issue dependent on low power for installed framework. They have been reasoned that Clock control is essential factor in the plan that lessens control utilization. To lessen the power Register Transfer Level (RTL) is utilized which decreases the check motion in the entire framework. The objective of this paper is to style processor which fits the above criteria and contains 8-bit ALU, banner register, program memory chipping away at 2.5 voltage supplies and the recurrence of 25MHz. The module contains 2 hinder and both are cover capable. The general processor accompanies the preferred standpoint that increasingly number of guidelines can be executed. The idea of pipelining makes the framework configurable. There are two location transport isolated. After the examination of the outcome it is presumed that checking method helps in use of less power [1]

E. Ayeh, K. Agbedanu, Y. Morita, O. Adamo, and P. Guturu have presented on FPGA usage of installed processor. The reasonable distinction have been referenced that why FPGA is favorable. They have referenced a portion of the upside of ASICs, DSP based structure and infer that FPGAs are ordinarily slower than ASICs however have overwhelming interest in market. The principle of this paper is to structure processor dependent on FPGA having 8-bit guidance recognizes the location. The three

primary parts control unit, ALU, and furthermore the memory is utilized in the framework. FSM is utilized to structure the administration unit. They have utilized SRAM memory of 8-bit long. All the unit of the proposed processor is planned and tried independently utilizing VHDL with recurrence of 95.364 MHz at deferral of 10.486 ns [2]

Reuben James L. Austria, Annaliza L. Sambile, Kahr-Lile M. Villegas, Jay Nickson T. Tabing have exhibited consider and issue of broadly useful processor in correlation with application explicit processor to process the information of the gadget stage. There are many existing processor that can be utilized in sensor stage for our need. The processor is planned with the goal that it very well may be utilized in much application. Be that as it may, this plan can be minimal costly in view of the utilization of sensor yet have many preferred standpoint in it. By thinking about all the issue the processor planned with 5 phases pipelined with discrete information and guidance memory in this manner it improves the speed and turnout of the chip. They have utilized UVM as a testing apparatus and got high precision results. The 90 nm innovation is utilized for incorporating the plan and got a door level net-list utilized for check. The style was conjointly executed and tried in FPGA [3]

Dr. S. L. Lahudkar1, Amit M. Mankar, Sudesh D. Bhong have presented based on latest technology in VLSI domain. Customer wants system that suits their objectives this is creating pressure on designer. The paper pointed towards designing processor which can be used as single chip or array of chip access for SoC design. The processor is designed using Von Neumann architecture with various different modules like control unit, ALU, shifter, and an address and data bus. The concept of pipelining increase the performance of the processor it's speed with less power consumption and less area. The design core is compatible with binary Microchip. The use of Microchip PIC-core makes system reliable to be used in wide verities of application. The processor is design and implement on Xilinx tools [4]

Krishna Kumar mishra, Vaibhav Purwar, Pankaj Singh have presented a design of RISC processor using a Finite State Machine designing approach using structural programming. The paper is pointed towards reducing the execution time and increasing the performance of the processor by using reduced instruction set architecture. The complete system works on 146.370 MHz frequency with 6.832 ns delay. Each of the instruction is executed in more than one clock cycle with non-pipelined concept. The design has been made with four separate ports and clock and reseat pin for communication purpose. They have shown the comparison table for analysis of instruction in Sim2 and AD8051 Microcontroller and concluded that speed is much faster in AD8051 than Sim2 [5]

Antonio Hernández Zavala, Oscar Camacho Nieto, Jorge A. Huerta Ruelas, Arodi R. Carvallo Dominguez have presented on complete understanding of computer architecture. By keeping in consideration the use of computer in technological world the proposed style has been designed which gives the details from its internal structure up to testing. They have listed 5 different approach used to explain computer architecture- paper, simple hardware, simulator, Hardware Description Languages HDL, Logic blocks and whole designing of processor with instruction set, ALU, and control unit. The design was tested in using the Xilinx ISE tools [6]

Ramandeep Kaur, Anuj have displayed on planning the processor by most recent Verilog coding taking in thought the drifting utilization of RISC Processor. It is most reasonable plan for the processor building in light of the fact that by structuring processor by this style is anything but difficult to test and fabricate. This whole element causes the style to be utilized in mechanical field. The processor is intended for higher proficiency and throughput. This proposed processor contain different little modules to be incorporated trailed by 3 organize pipelining (get, interpret and execute). The structure bolsters with the sixteen headings for different guidelines. The total paper is partitioned in discrete parts and all the engineering is clarified appropriately with configuration is tried in Xilinx Straightforward 3E innovation with correlation of the outcomes is done.[7]

Hyejung Kim, Kyomin Sohn, Jerald Yoo and Hoi-Jun Yoo have presented an issue to resolve the enhancement in memory yield. The architecture designed to improve the yield of the system. The suggestion has been made to use the BISO algorithm to resolve this issue. The processor style is adopted to reduce the area occupation of the system along with general purpose functioning. The architecture works on 3 stage pipelining but few instructions may require multi cycle. They have used the PRAM testing to verify the effectiveness of system but also require more control to optimize this. By using RISC style improves the issue regarding PRAM and provides the throughput of 100 Mbps/s [8]

Lopamudra Samal, Chiranjibi Samal have presented on designing an application specific processor because it's flexible and provides low power dissipation. The design of 8-bit microprocessor contains same functions as that in 8051 with the operating frequency of 84 MHz. The processor contains separate address and data bus. Coding is done in VHDL and simulated using Xilinx

tool and can handle as many task which is present in particular area with low power dissipation. And concluded that we can increase the area of the system [9]

R. Uma has have presented a solution to analyze issue like area occupied by system its power dissipation and clock delay by using RISC processor. The features of RISC processor is mentioned clearly along with the concept of pipelining. The design of an 8-bit processor is presented. With separate instruction format, register set as well as ALU for basic operation. The designs contain 3 stages pipelining along with fetch, decode and execute. The RISC processor is evaluated in XILINX SPARTAN 3E XCS500E technology with delay of 77.4 ns and power dissipation of 6.258 W. And concluded that by using adiabatic logic we can reduce the power dissipation of the system [10]

III. CONCLUSION

As the aspect and growth of VLSI design is increasing day by day, customer wants design to suit their need. So enhancement in processor leads to better functioning of electronics device. Demand of application- specific Processor is increased and implementation of it on FPGA tool is required in order to meet the customer requirement. In this paper, we discussed various researched conducted to resolve this issue. However, these work mainly focused on the designing the best RISC processor by taking some of the characteristics into consideration. For making the design to be competitive it should be compatible with subsequent characteristics comparatively cheap, amendable, tolerable, and quick. The best solution for all this characteristics is to use an processor along with FPGA as a design tool. Selection of proper method could be a key factor for the improved and efficient system.

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