# "USB 3.0 Based Digital Data Pattern Generator and Data Formatter"

**Harsidhdhi S. Kotila[1*], Vishal S.Vora[2]**

[1]*Department of Electronics & Communication Engineering, Atmiya Institute of Technology & science, Rajkot, Gujarat, INDIA*

**Abstract** – The project is concentrating on development of digital pattern generator and formatter for the high speed systems. As the technology advances the requirement of fast data transfer and processing arises. To meet the requirement the data should be read, write or processed in faster rates typically in Gbps. The proposed system is an effort to the same field and develops the high speed USB data pattern generator and formatter working in the Gbps speeds. USB is an interface that connects a device to a computer. With this connection, the computer sends or retrieves data from the device. USB gives developers a standard interface to use in many different types of applications. A USB device is easy to connect and use because of a systematic design process. Presently there are many systems available with USB 2.0 interface at 480 Mbps. The USB 3.0 specification, released in 2008, allows a maximum signaling rate of up to 5 Gbps (SuperSpeed), which is 10 times the signaling rate of High Speed. USB 3.0 based Digital Data Formatter card which acquires data from multiple data chains and feeds it to USB 3.0 module and it sends data to host PC over USB 3.0 cable, for storing the acquired data in the system memory of host PC for further evaluation.

**Keywords:** - USB 2.0, USB 3.0 CONTROLLER, SIMULATOR, FORMATTER, PATTERN GENRATOR, FPGA, PCIe, etc..

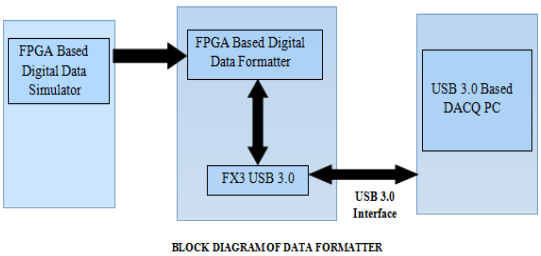
## I. INTRODUCTION

Aim of this project is development of digital data pattern generator and data formattar Using USB protocol to communicate between the nodes for SAC ground checkout systems. Pattern generator is a device, which can be programmed to generate any particular digital signal for testing purposes. It usually consists of several channels. These channels serve as the output of the generator. Each channel can individually be programmed for a desired signal. The programmed signal or the pattern is stored in a buffer memory and clocked out at a user defined sampling rate. The application for a pattern generator varies from generating a single channel square wave to digital protocols such as SPI, USB, and multi channel complex patterns. Digital Signal formatting is the process of transforming information from one format into another. This is often used in many digital devices and for communication processes. A digital system is a data technology that uses discrete (discontinuous) values. By contrast, non- digital (or analog) systems use a continuous range of values to represent information. Although digital representations are discrete, the information represented can be either discrete, such as numbers, letters or icons, or continuous, such as sounds, images, and other measurements of continuous systems.

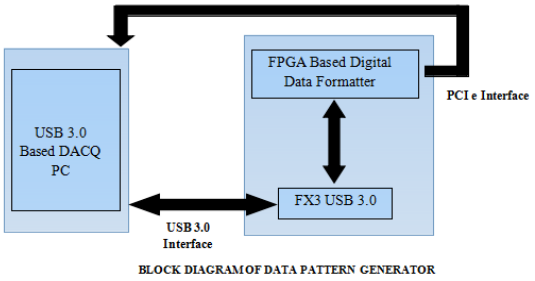
In our proposed system, USB interface is used. Motivation for USB 2.0[2] was stem from the fact that PCs have increasingly higher performance and are capable of processing vast amounts of data. At the same time, PC peripherals have added more performance and functionality. User applications such as digital imaging demand a high performance connection between the PC and these increasingly sophisticated peripherals. The same demand has increased and motivated the development of FX3 to meet higher data rate demand up to 5 Gbps. For the testing of high speed devices the digital data pattern generator and formatter is used. The proposed solution meets the high speed data rate requirement for digital communication. demand up to 5 Gbps. For the testing of high speed devices the digital data pattern generator and formatter is used. The proposed solution meets the high speed data rate requirement for digital communication.

## 2. USB INTERFACE DESCRIPTION

USB 3.0 and USB 2.0 devices connect to and communication with the USB 3.0 host. The USB 3.0 interconnect inherits core architectural elements from USB 2.0, although several are augmented to accommodate the dual bus architecture. The baseline structural topology is the same as USB 2.0. It consists of a tiered star topology with a single host at tier 1 and hubs at lower tiers to provide bus connectivity to device.




BLOCK DIAGRAM OF DATA FORMATTER




BLOCK DIAGRAMOF DATA PATTERN GENERATOR

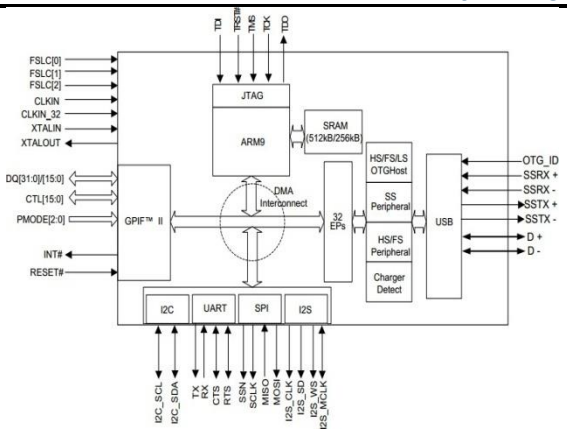



Fig.3 Block diagram of FX3

FX3 is a USB 3.0 peripheral controller with an integrated ARM9 processor. Parallel and serial interfaces provide high-speed connectivity with other devices in the user system. The main function of the FX3 device in a system is to transfer high- bandwidth data between a USB host and a peripheral device, such as a camera or scanner. The presence of a powerful ARM9 processor on-chip also allows FX3 to access the data stream and efficiently process data. In systems where FX3 is not required to perform data processing, the ARM9 firmware only initializes and manages data transfers between two interfaces—USB and a data consuming/providing device.

FX3 has a highly flexible, programmable interface known as the General Programmable Interface Generation 2 (GPIF II) in addition to I2C, SPI, UART, and I2S serial interfaces. GPIF II programmability allows FX3 to be connected to various types of devices including FPGAs, image sensors, ADCs, and application processors. This makes FX3 a good controller choice in a wide range of high-performance USB 3.0 applications.

## 3. LOGICAL STRUCTURE OF THE INTERFACE

### A. FPGA/ASIC Interfaced to FX3

Several applications connect an FPGA or ASIC to FX3 over a high-speed parallel GPIF II interface. Another device, which is the source or sink of data is connected to the FPGA or ASIC. Examples of such applications are data acquisition devices, printers, scanners, and imaging devices. In such applications, FX3 serves as a fast data pipe to and from a USB host. For these applications, the FX3-to FPGA/ASIC interface is typically the synchronous Slave FIFO interface.

In applications where FX3 connects to an FPGA, it may be preferred to load the FPGA bit file through FX3. In this case, the FPGA configuration file can be transferred from a USB host through FX3 to the FPGA. This saves the cost of an FPGA boot memory and enables FPGA reconfiguration (including updates) from the PC.

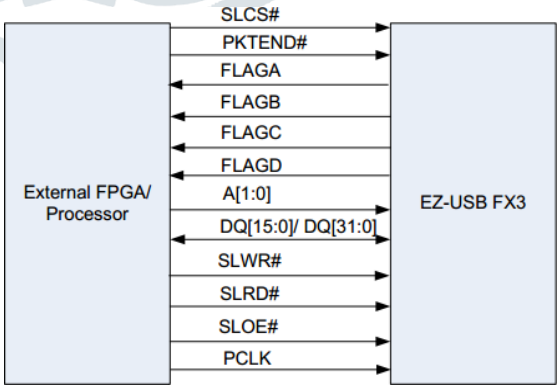
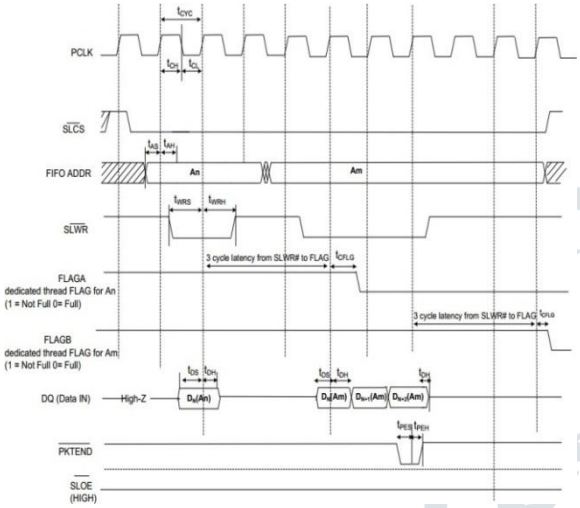



Fig 4. FPGA/ASIC Interfaced to FX3

### B. Synchronous Slave FIFO Write Sequence

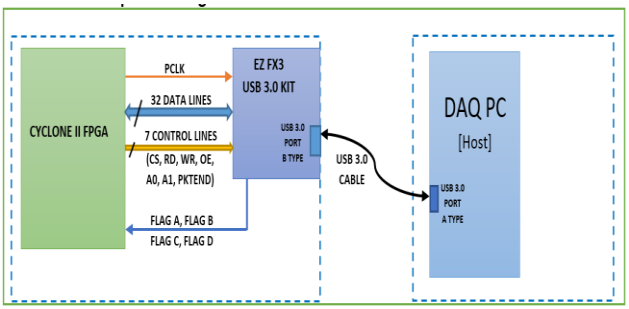
The sequence for performing writes to the synchronous Slave FIFO interface is - 1.FIFO address is stable and the signal SLCS is asserted. 2. External master/peripheral outputs the data onto the data bus. 3.SLWR is asserted. 4.While the SLWR is asserted, data is written to the FIFO; on the rising edge of the PCLK, the FIFO pointer is incremented. 5.The FIFO flag is updated after a delay of Tc flag from the rising edge of the clock.




### C. Synchronous Slave FIFO Read Sequence

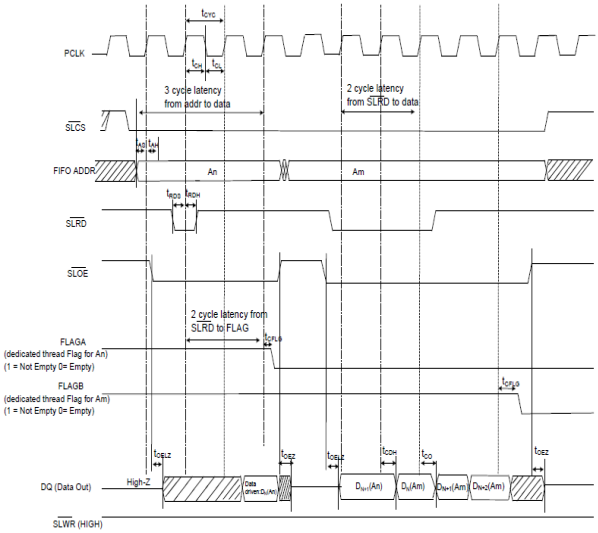
The sequence for performing reads from the synchronous Slave FIFO interface is:1. FIFO address is stable and SLCS is asserted.2.SLOE is asserted. SLOE is an output enable only whose sole function is to drive the data bus. 3.SLRD is asserted.

The FIFO pointer is updated on the rising edge of the PCLK while SLRD is asserted. This action starts the propagation of data from the newly addressed FIFO to the data bus. After a propagation delay of Tco (measured from the rising edge of PCLK), the new data value is present. N is the first data value read from the FIFO. To drive the data bus, SLOE must also be asserted.




### D. Test Setup

Block diagram of test setup implementation is shown**.** Here 32 bit data bus and all control signals of EZ USB FX3 module are connected to FPGA. This FPGA is used to generate digital data pattern and control signal to provide FX3 module. Quartus II software and VHSIC Hardware




Description Language (VHDL) is used for programming the FPGA.FX3 USB module is a FIFO based device, FIFO write operation is done to communicate with this module. FX3 module is connected to host PC through USB 3.0 interface. Stored data in FIFO is transfer through USB 3.0 interface when host is ready to receive data. This system can be utilized as high speed communication system working on Gbps speed.

## 4. RESULT AND DISCUSSION

### Output Testing in two different types of application.

### A. Vendor Application – USB Control Center and C++ Streamer

Using USB control centre, different data pattern can be given to the FX3 card [refer figure 7]. The USB control centre can be divided into two modules, i.e. USB control centre and C++ streamer. To test the input sequence to FX3 card, USB control centre is used and for testing the output bit rate of read and write sequence the USB streamer is used which can simulate output speed of FX3 interface for given test sequence.

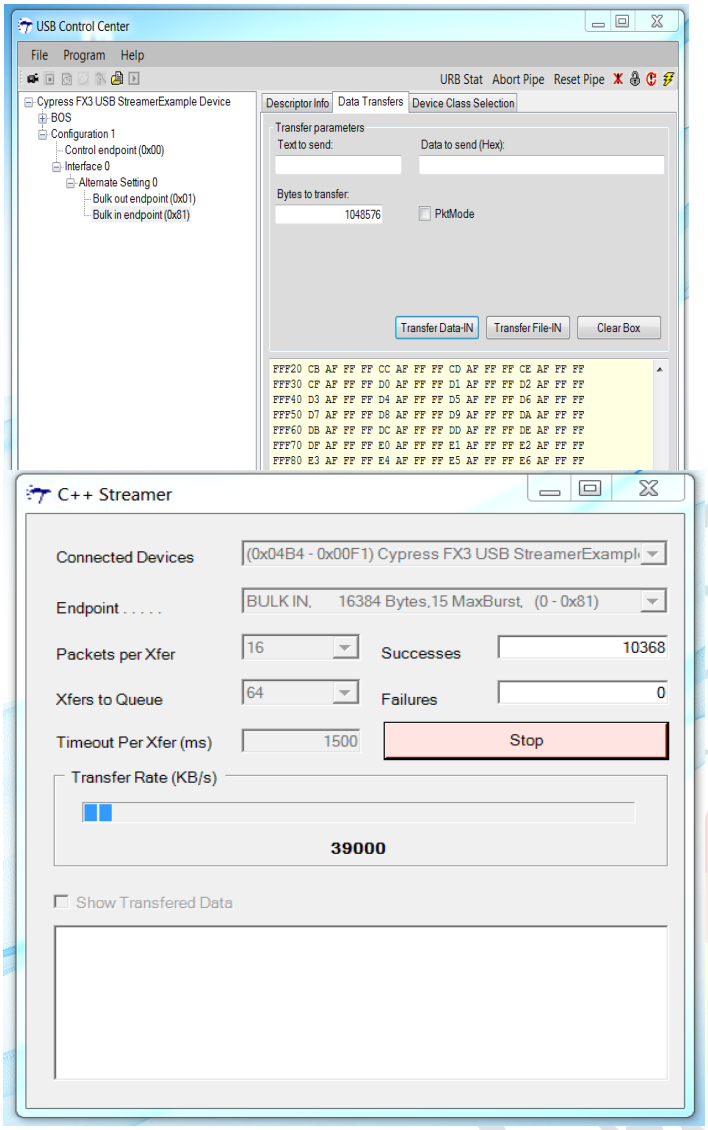
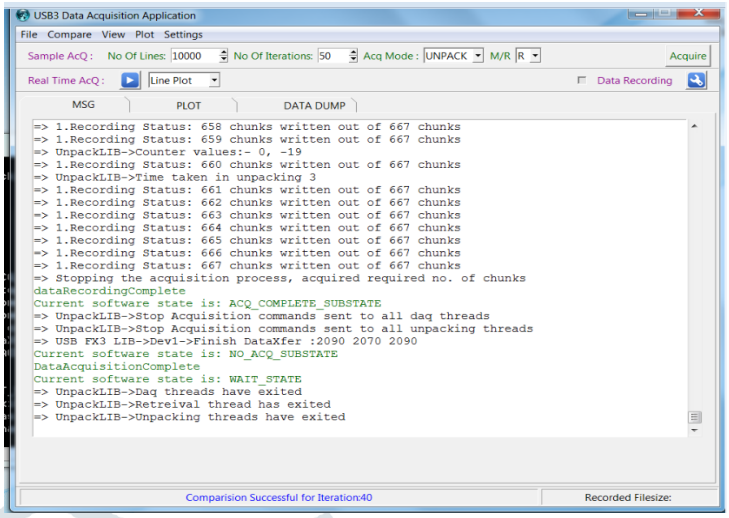



Fig.7 USB Control Center




## B ISRO DEVELOP APPLICATION- USB3 DATA ACQUISITION APPLICATION

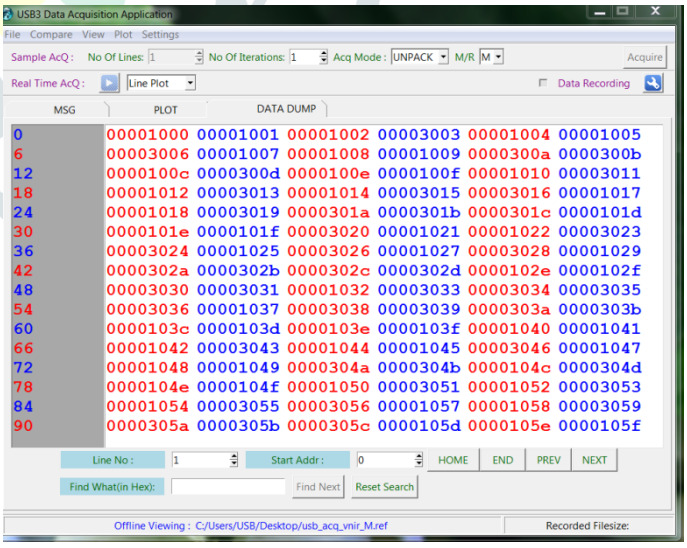



Fig.9 USB 3 Data Acquisition Application

## 5. APPLICATION

There are well-establish solutions for connection with desktop processors, like multi-gigabit optical fibre or external PCI-Express, the same is not true for portable detection application that are often used connected to laptops through the USB 2.0 bus or the Ethernet bus. However, the bandwidth of the USB 2.0 bus is too small for very high data rates, both in case of fast sampling and in presence of a high number of channel. So, USB 3.0 Protocol is used.

## 6. CONCLUSION

In the proposed system, Digital data Formatter is generated for testing the bit rate of USB 3.0. The system of FX3 card is done on FPGA simulation card USB FX3 card is acting as data formatter card and FPGA is acting as simulation card for the proposed system. With this concern, higher bit rate has been achieved. The USB 3.0 is having maximum bandwidth of 5 Gbps. So, future scope is to achieve the highest bit rate near to 5 Gbps with the same system. This System can be used in high speed data interfacing in modern system, imaging applications in satellites, data storage and transfer etc.

## 7. REFERENCES

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