Reversible Carry Look Ahead Adder using SOA based Optical Mach-Zehnder Interferometer Switch

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Abstract: Optical computing is emerging in designing of low power high speed architectures. Reversible logic is trending in designing for nano-circuits due to its ability to reduce power consumption. Adder is the basic building elements in designing any architecture of the digital circuits. As the carry look ahead adder is fastest among all the digital adders where carry is independent of the previous stages. This paper presents the carry look ahead adder based on reversible SOA based (Mach Zehnder Interferometer) MZI switch. These MZI switch are used in realizing the digital circuits with respect to optical computing. This paper aims in reducing the delay of the proposed carry look ahead adder circuits when optical logic gates are used. Also the comparison when reversible logic gates are used. The proposed designs are synthesized using XILINX ISE Design suite 14.7 and simulated using ISim simulator using Verilog.

Keywords-**Reversible logic, Optical computing, Carry look ahead adder, MZI switch.**

I. INTRODUCTION

Reversible computation is gaining familiarity in the era of low power VLSI technology. Research is going on reversible computation in various fields specially quantum computation. Quantum computers are the hot topic to do the research and also various works are going towards machine learning with the help of quantum computing.

Reversal of time on quantum computers is also emerging so fast. For quantum computation, reversible logic is the backbone. Reversible logic used reversible gates for lossless information. In conventional computation the logic circuits are irreversible in nature. The inputs are not regenerated from outputs. So they dissipate a large amount of heat. According to Landeurs principle erasing a bit of information causes kTln2 joules of heat energy to be dissipated. In conventional logic bit of information may be erased which leads to loss of information and no chance to recover the inputs from outputs. So to avoid such kind of erasure reversible computation is used.

It is also proved by many of the researchers with respect to conventional computation that any logic circuit performed leads to loss of information. According to thermodynamics Bennett proved that kTln2 Joules of energy is not dissipated when any logic computation is carried out using reversible logic. Bennett in 1973 showed that for power not to be dissipated in an arbitrary circuit, it is necessary that this circuit be built from reversible gates. The importance of Bennett's theorem lies in the technological necessity that every future technology will have to use reversible gates in order to reduce power loss.

The original motivation towards the reversible computation is they dissipate less heat under ideal conditions, considerably less heat. According to the launder principle it is no heat. Considering the logic gate that performs a certain operation; information present at input will be lost at output. This lost information is dissipated into the environment. This is according to the principle of thermodynamics entropy. It is clearly understood that the charge present at input of the circuit gets grounded and flown away when it changes it state to obtain the output. Here a small amount of energy is taken away leaving to information loss. Whereas the reversible gates moves around the states and does not gets grounded. So as a result the loss of information is not possible leaving to energy conservation.

II. OPTICAL MZI SWITCH

An optical MZI switch is a device which consists of two semi conductor optical amplifiers namely SOA 1 and SOA 2 along with three couplers namely C1, C2, C3 as shown in fig 1.as which most of the designs uses two couplers, one coupler for output and one for the input is used.
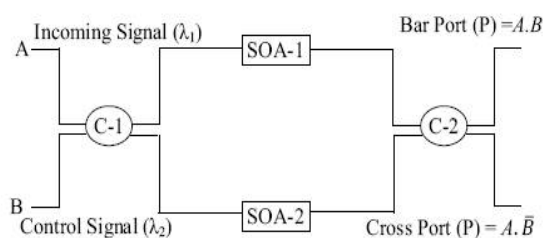

Fig 1: SOA based optical MZI switch

The inputs to first coupler are the incoming signals which is sent to both SOA1 and SOA 2.when control signal is sent to any one SOA either SOA1 or SOA2, it results in refractive index change which is given as $\Delta n = nI$. Here I is intensity of incident light and n is the refractive coefficient.MZI is balanced when control signal is absent. Change in refractive index causes the shift in phase of signal passing through SOA1. This results the incoming signal gets switched to bar port.

The optical MZI switch is shown in fig 1. It acts like a switch with the incoming signal being controlled by control signal. This incoming signal has the wavelength which is divided by the C1 coupler and propagates through SOA1 and SOA2 separately. When no signal is applied, the port is open. Due to this SOA1 and SOA2 were providing unsaturated gains. When a pulsed signal is applied to MZI through C2 providing most of signals to SOA1, this causes SOA1 to get into saturation mode resulting differential phase shift. In this mode SOA2 will be in unsaturation. "Switched state" takes place because of this phenomenon causing the output signal port 4 to switch to port 3 which is bar port. When no pulsed signal is given to MZI, "unswitched state" occurs resulting the output signal port4 which is cross port.

A. Beam Combiner (BC) and Beam Splitter (BS):

Beam combiner (BC) simply combines the optical beams while the beam splitter (BS) splits the beams into two optical beams. The optical cost and the delay of beam combiner and beam splitter are negligible [4, 6] and while calculating optical cost of a circuit, it may be assumed as zero.

B. Optical cost and delay:

As the optical cost of BS and BC are relatively small, the optical cost of a given circuit is the number of MZI switches required to design the realization. The optical delay is estimated as the number of stages of MZI switches multiplied by a unitΔ

III. IMPLEMENTATION OF REVERSIBLE LOGIC GATES WITH MZI SWITCH

The optical MZI switch is the fastest switch and is very much suitable in designing of low power high speed architectures .the optical implementation of various reversible logic gates are shown in this section.

A. Optical Peres gate (OPG):

The unique inputs 'A', 'B', 'C' of Peres gate (PG) are uniquely mapped to outputs 'P', 'Q', 'R' in such a way that the functionality is $P = A; Q = A \oplus B; R=AB \oplus C$
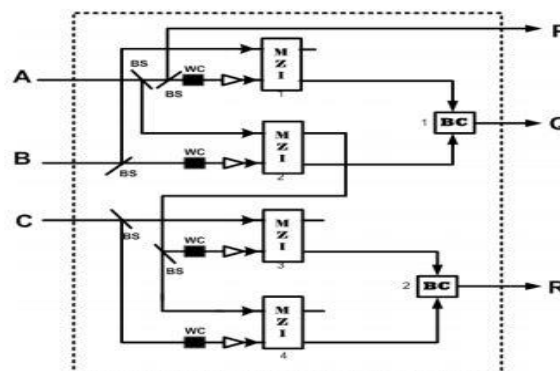

Fig 2: Peres gate using MZI switch

B. Optical Toffoli gate (OTG):

The Toffoli gate is also known as controlled – controlled NOT gate. If two inputs are set to logic '1', it inverts the third bit else all the bits remain same. The unique inputs 'A', 'B', 'C' of Toffoli gate (TG) are uniquely mapped to outputs 'P', 'Q', 'R' in such a way that the functionality is $P = A; Q = B; R=AB \oplus C$.
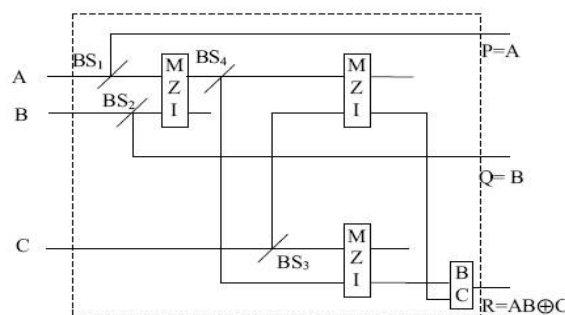

Fig 3: Toffoli gate using MZI switch

This gate is constructed using two controlled – V gate and one controlled – v+ gate and two Feynman gate.

C. Optical Feynman gate (OFG):

The Feynman gate is also called as controlled NOT gate. The unique inputs 'A', 'B' of Feynman gate (FG) are uniquely mapped to outputs 'P', 'Q' in such a way that the functionality is $P = A$; $Q = A \oplus B$. It is used to double the inputs in order to avoid the fan out.
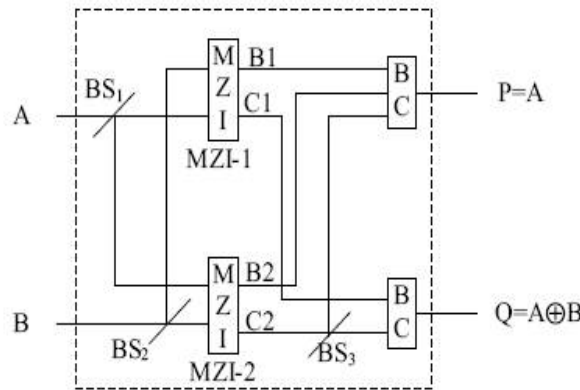

Fig 4: Feynman gate (FG) using MZI switch

IV. CARRY LOOK AHEAD ADDER USING OPTICAL MZI SWITCH:

Carry look ahead adder is the fastest adder when compared to ripple carry adder. The ripple carry adder depends on previous stages where as carry look ahead adder doesn't depend on previous stage. The propagation delay decreases by propagating and generating carry. In this type of adder we don't need to wait for carry and also the sum of the before stage. It computes carry in parallel form. It is similar to full adder but has carry stages. Carry generate and carry propagate are the stages of carry.

Generate and propagate of carry look ahead adder are given by

$$G_i = A_i \text{ AND } B_i \qquad (1)$$
$$P_i = A_i \oplus B_i \qquad (2)$$
$$\text{SUM } S_i = A_i \oplus B_i \oplus C_{in} \qquad (3)$$
$$\text{Carry out } C_{i+1} = P_i . C_{in} + G_i \qquad (4)$$

Carry generates logic '0' only when both the inputs A and B are logic '0'. Carry generates logic '1' only when both the A and B inputs are in '1' logic. Carry gets generated to next stage only when the input bit A and B doesn't have same logic bits.

A. Carry calculation:

$C_1 = G_0 \oplus P_0C_0$
$C_2 = G_1 \oplus P_1C_1$
    $= G_1 \oplus P_1 (G_0 \oplus P_0C_0)$
$C_3 = G_2 \oplus P_2C_2$
    $= G_2 \oplus P_2 (G_1 \oplus P_1C_1)$
    $= G_2 \oplus P_2 (G_1 \oplus P_1 G_0 \oplus P_1P_0C_0)$
$C_4 = G_3 \oplus P_3C_3$
    $= G_3 \oplus P_3 (G_2 \oplus P_2C_2)$
    $= G_3 \oplus P_3 (G_2 \oplus P_2 G_1 \oplus P_2P_1C_1)$
    $= G_3 \oplus P_3 (G_2 \oplus P_2 G_1 \oplus P_2P_1G_0 \oplus P_2P_1P_0C_0)$ and so on.

So the generalized carry expression for carry look ahead adder (CLA) having 'n' stages is

$$Cn = Gn\text{-}1 \oplus Pn\text{-}1(Gn\text{-}2 \oplus \text{-------} \oplus Pn\text{-}2Pn\text{-}3 \text{-------}P0C0) \qquad (5)$$

B. Sum calculation:

$S_0 = P_0 \oplus C_0$
$S_1 = P_1 \oplus C_1$
    $= P_1 \oplus G_0 \oplus P_0C_0$
$S_2 = P_2 \oplus C_2$
    $= P_2 \oplus G_1 \oplus P_1C_1$
    $= P_2 \oplus G_1 \oplus P_1 (G_0 \oplus P_0C_0)$
$S_3 = P_3 \oplus C_3$
    $= P_3 \oplus G_2 \oplus P_2C_2$
    $= P_3 \oplus G_2 \oplus P_2 (G_1 \oplus P_1C_1)$
    $= P_3 \oplus G_2 \oplus P_2 (G_1 \oplus P_1G_0 \oplus P_1P_0C_0)$
$S_4 = P_4 \oplus C_4$
    $= P_4 \oplus G_3 \oplus P_3C_3$
    $= P_4 \oplus G_3 \oplus P_3 (G_2 \oplus P_2C_2)$
    $= P_4 \oplus G_3 \oplus P_3 (G_2 \oplus P_2G_1 \oplus P_2P_1C_1)$
    $= P_4 \oplus G_3 \oplus P_3 (G_2 \oplus P_2G_1 \oplus P_2P_1G_0 \oplus P_2P_1P_0C_0)$ and so on.

So the generalized sum expression for carry look ahead adder (CLA) having 'n' stages is

$Sn= Pn \oplus Gn\text{-}1 \oplus Pn\text{-}1(Gn\text{-}2 \oplus \text{------} \oplus Pn\text{-}2Pn\text{-}3 \text{-----} P0C0)$ (6)

C.   Carry look ahead adder using MZI switch design 1.

In this design we designed carry/borrow look ahead adder/subtractor using reversible logic gates particularly Optical Peres gate and Optical Feynman gate.

The reason for using these gates is Optical Peres gate has the total quantum cost of 4 and the Feynman gate has total quantum cost of 1.so this design gives us the less quantum cost of the circuit.

As Ai and Bi are on either side of the OR operator in Eq.(4), it is rewritten as

$$Cout=C_{i+1}= G_i \oplus Pi.C_i.$$ (7)

When applied logic levels 0 and 1 to the Eq. (4) and Eq. (7) we get the same results of Cout. This is more advantageous in case of carry look ahead adder where + symbol also can be replaced by EXOR operator. This reduces the number of gates which certainly leads to less quantum cot of circuit. Also it leads to less delay and hardware complexity.
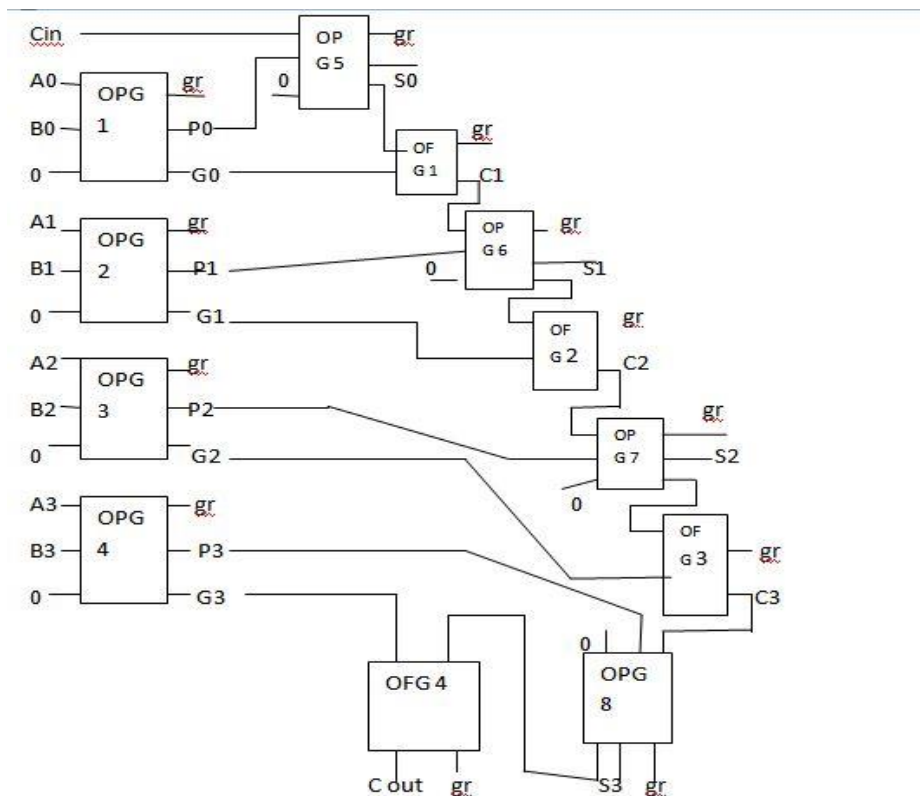

Fig 5: reversible carry look ahead adder using MZI switch design 1

The first step to design carry look ahead adder that also performs subtraction is computation of propagate and generate of the CARRY. To compute this we used Optical Peres gate (OPG). When logic 0 is applied to third input of Optical Peres gate it acts as EXOR operation as well as AND operation. From Eq.(1) and Eq.(2) it is clear that propagate has an EXOR operation of inputs and generate has an AND operation of inputs. So for propagate and generate Optical Peres gate (OPG) is suitable.

The second step is to realize the EXOR operator present in Eq. (3) and the AND operator in Eq. (7). For this Peres gate is used to realize this. Optical Peres gate with third input as logic 0 is used to produces second output Pi ⊕ Ci. This is the SUM output. And the third output of Optical Peres gate gives Pi.Ci. In this step we realized the SUM of carry look ahead adder.

The last step is to calculate the CARRY. As from Eq.(7) it is clear that EXOR operator is present. so Feynman gate is suitable to realize this. Using the Optical Feynman gate (OFG) Cout is achieved.

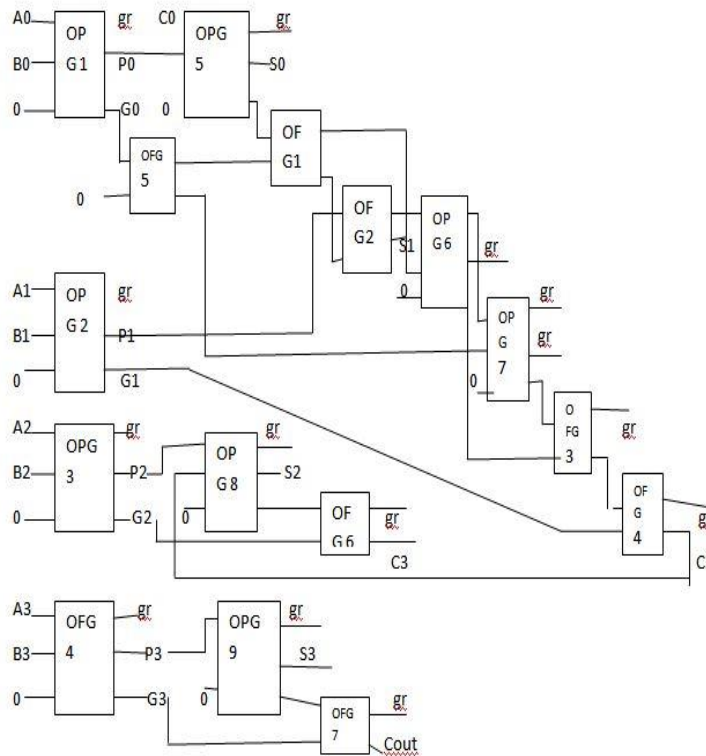## C. Carry look ahead adder using MZI switch design 2.

Fig 6: Reversible carry look ahead adder using MZI switch design 2

This design is designed making modifications with respect to the previous design without the change of functionality of carry look ahead adder. Here in this design we used Optical Feynman gate as copying gate to generate G0.the main advantage of copying gate is it can be used to copy the inputs at the outputs ,so that we can use it where ever needed.

V. RESULTS AND DISCUSSIONS

The functionality of the designs are designed using XILINX ISE design suite 14.7 and are simulated using ISim.

A. Wave forms of the proposed Reversible carry look ahead adder using MZI switch
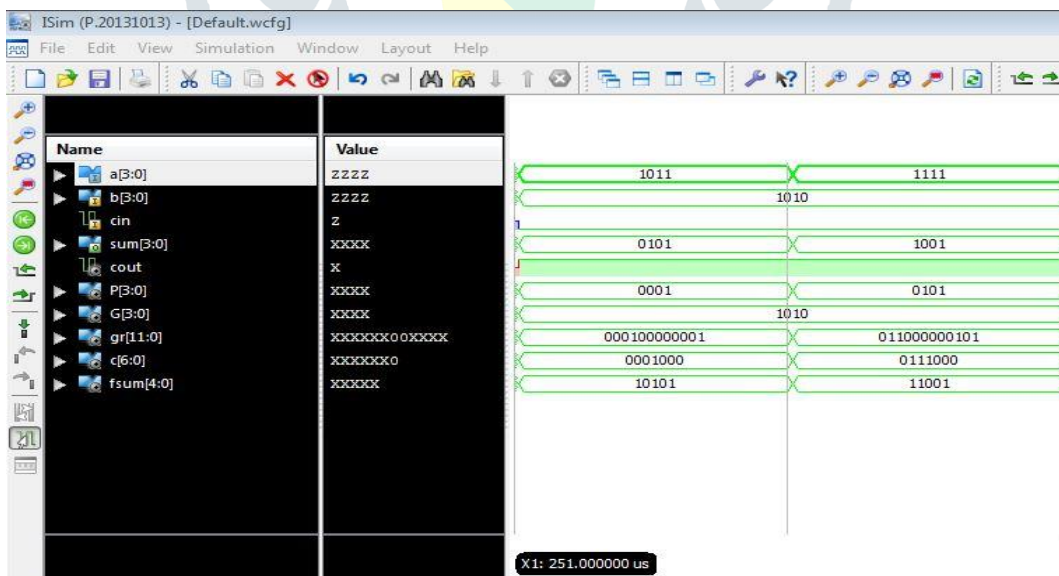

Fig 7: wave form of carry look ahead adder using MZI switch design 1

The above wave form shows the results when both inputs A and B are given with "1011" and "1010" respectively with Cin as '0'. As a result the output SUM is "0101" with Cout '1'. Also the carry generate G and carry propagate P are also shown.
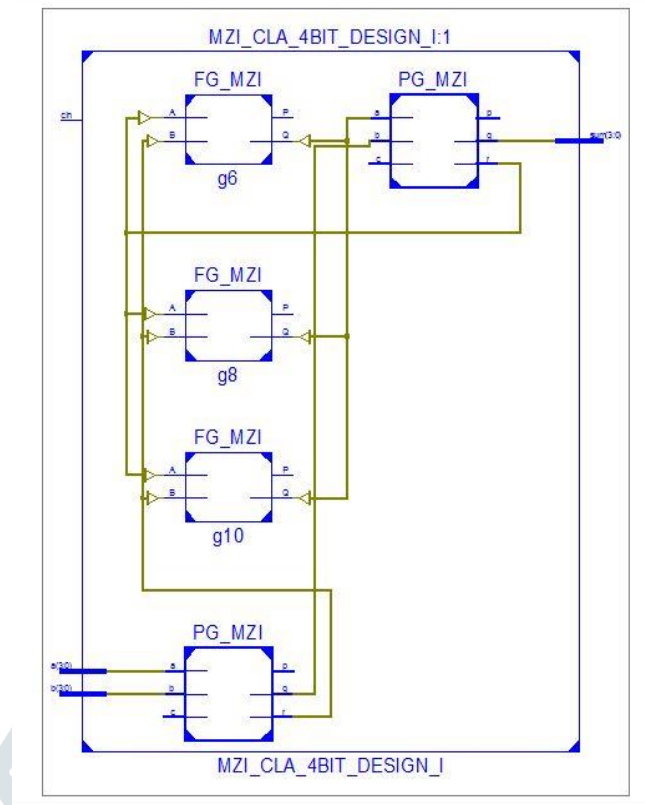
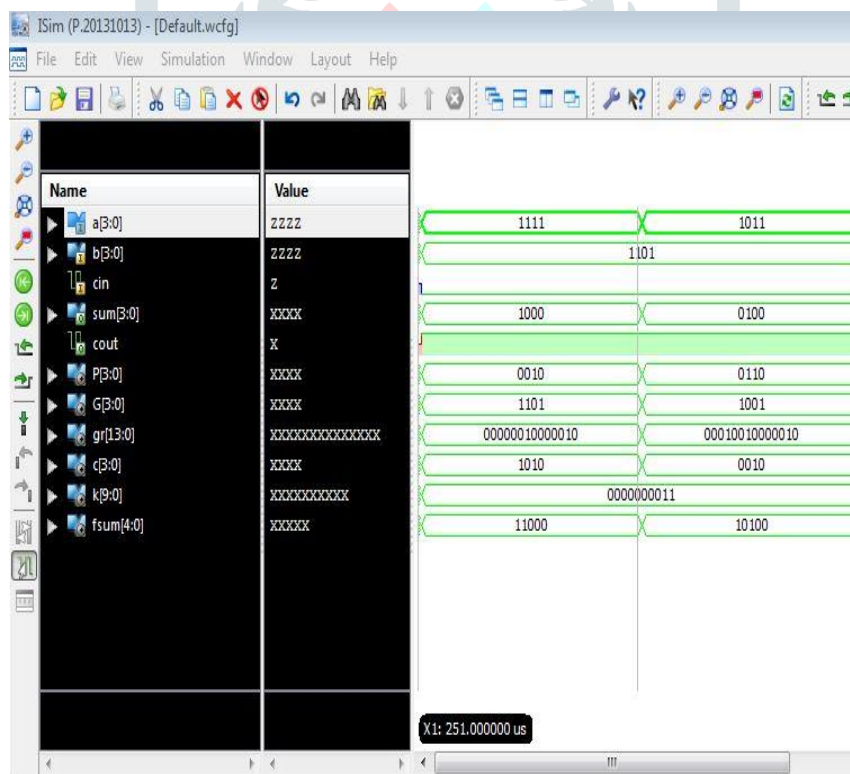Fig 8: RTL of carry look ahead adder using MZI switch design 1

Fig 9: Wave form of carry look ahead adder using MZI switch design 2

The above wave form shows the results when both inputs A and B are given with "1111" and "1101" respectively with Cin as '0'. As a result the output SUM is "1000" with Cout '1'. Also the carry generate G and carry propagate P are also shown.
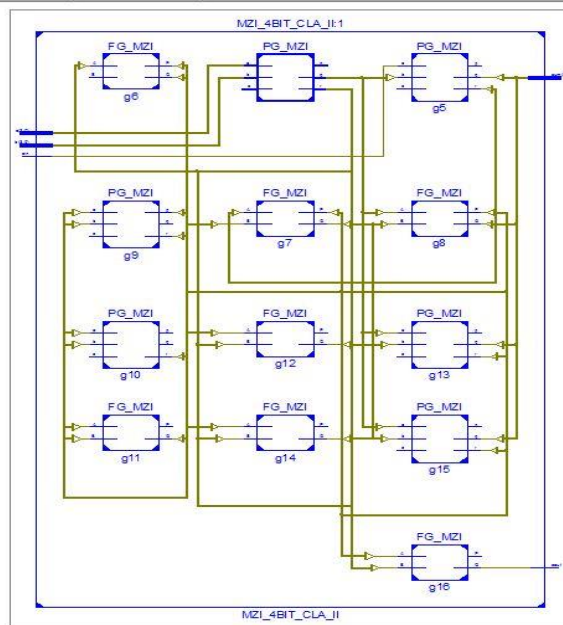
Fig 10: RTL of carry look ahead adder using MZI switch design 2

B. Results of carry look ahead adder using MZI switch

Table 1: Comparision table of the designs showing device utilization summary

Design	Number of slices (out of 960)	Number of 4 input LUT (out of 1920)	Number of IO's	Number of bonded IO's (out of 83)
CLA design 1	3	6	13	12
CLA design 2	4	7	14	14

        The above table shows the device utilization summary of the proposed designs in terms of number of slices used, number of 4 input LUT's used, number of IO's used and number of bonded IO's used. It is seen that the utilization is very less for the proposed designs.

Table 2: Comparison table showing delay

Design	Delay(ns)
CLA design 1	6.798
CLA design 2	6.834

    The delay for both the proposed designs of carry look ahead adder are shown in table 2 and are seen to have less delay. When these designs are designed using reversible logic gates these designs are shown to have more delay than this when compared to the proposed designs

Table 3: Comparison table showing various parameters when used reversible logic gates

Design	Number of slices (out of 960)	Number of 4 input LUT (out of 1920)	Number of IO's	Number of bonded IO's (out of 83)
CLA design 1	4	7	13	13
CLA design 2	4	8	14	14

Table 4: Comparison table showing delay when used reversible logic gate

Design	Delay(ns)
CLA design 1	7.859
CLA design 2	8.881

    From the comparison tables it is clear that design implemented using optical MZI switch has improvements in delay and device utilization than when implemented using reversible logic gates.

VI. CONCLUSION AND FUTURE SCOPE

In this paper, two types of reversible carry look ahead adder designs are implemented. These designs are simulated and verified using XILINX ISE Design suite 14.7 tool. The design 1 is designed using optical reversible logic gates mainly optical Peres gate (OPG) and optical Feynman gate (OFG). The design 2 is designed with more optical reversible logic gates. We use optical Feynman gate (OFG) as copying gate so that we get more no of reversible logic gates. The main aim of using copying gate is when we need the same variable to be used number of times we use copying gate to generate same variable so that it can be used where ever needed. On comparing the design 1 and design 2 it is clear that design 1 is better in terms of delay than design 2. In future we can extend it to more no of bits and can be used in high speed processors and low power architectures design. Also these architectures can be implemented in various fields such as quantum computing and nano computing for effective results. These designs can be further designed by introducing testing of the circuits.

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