Design and Implementation of High-Speed Low Power Compressors as standard cells for ASIC's

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Abstract: The 3-2, 4-2, 5-2 find many applications in the evolution of integrated circuits. One of the major applications of them is to add partial products that are generated at one stage in Multipliers. In this paper a newly proposed 3-2, 4-2, 5-2 architectures having less delay and reduced power consumption than the conventional architectures are presented. The key idea of designing these multipliers with better performance characteristics leads to the implementation of pass transistors, transmission gates and domino logic circuits. All the CMOS circuits used in proposed architectures are having better performances than their existing CMOS counterparts. The proposed 3-2 model offer 66.6-82.69% less power and 52.48-64.62% reduction in propagation delay than the conventional 3-2 model. The proposed 4-2 model offer 52.37-55.367% less delay and 7.8-16.86% reduction in propagation delay than the conventional 4-2 model. The proposed 5-2 model offer 54.93-57.4% less power and 9.2-74.82% reduction in propagation delay. With all these significance improvements in their performance, they are chosen as a best option in designing Multipliers.

Index Terms **- Multipliers, CMOS, Pass transistors, Voltage swing, Transmission gates, and Domino logic.**

I. INTRODUCTION

Evolution of integrated circuits requires large number of components to be incorporated in them. The design of these circuits should contain the logic styles having better performance characteristics to influence the speed of the processor. It is noted that arithmetic circuits are required to construct the sub system components of the proposed architectures. This paper gives an emphasis on how the design of these arithmetic circuits should affect the architecture performance in terms of power consumption and propagation delay. Design of adder circuits in code converters and ALU in microprocessors, convolution and filtering circuits in Digital Signal Processing (DSP) require multiplier circuits for better performance digital application. All these applications use Multiplication as its common arithmetic operation. [1-4].

Partial products generated in the adder circuits plays a key role in designing low power and high speed circuits. Power consumption, propagation delay and Lay out area in multipliers are reduced to some extent by generating partial products using Carry Save Structure(CSA).Carry propagation adder is used for computation of final result. Multiplications and divisions operations use adder circuits as one of the essential components. The design of these arithmetic circuits is grown up as a huge concern these days as they require very large complex circuits. DADDY's compression technique is one of the most widely used techniques in CS adders to reduce the propagation delay [1].

The objective of 3-2, 4-2, 5-2 compressors is to reduce the number of bits from higher order to 2 and is used in realisation of higher order compressors such as 7-2, 11-2 etc. This paper presents the use of logic styles of pass transistors, transmission gates, domino logic circuits in proposed 3-2, 4-2, 5-2 architectures which result in better performance than conventional 4-2 compressor architectures.

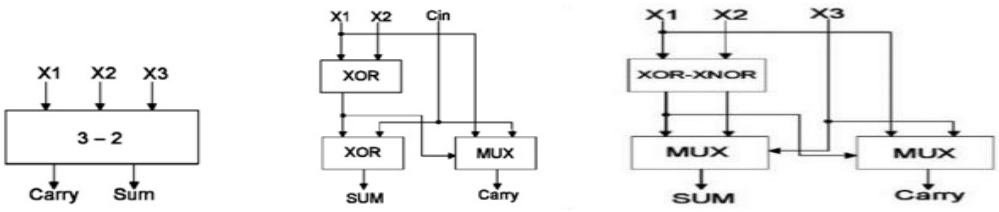
The rest of the paper is organised is as follows: In section 2, the previous work for designing compressors are presented in brief. In section 3, 4, 5 the proposed models of 3-2, 4-2, 5-2 compressors are discussed briefly. In section 6, comparison of these proposed models with the existing models are presented. Simulation of the models is done by using H-Spice tools in 180 nm technology and at 1.8V supply.

II. PREVIOUS WORK

In order to make the compressors make faster and to make less power consumption, XOR gates are replaced by Multiplexers. Multiplexers are used to construct 3-2, 4-2 and 5-2 compressors. This is achieved by taking the complements of XOR and multiplexer and implementing them as input for next stage of compressor architectures. This shows the effective use calculated values and reduces the garbage values in the circuit. Inverters are not included in the new architectures to increase the speed and to reduce the number of transistors. Simulations of conventional architectures and new architectures are done from 0.9V to 3.3V at a frequency of 100 MHZ in 180 nm technology. The new architectures are compared with conventional architectures and are found to have better performance of propagation delay and power [5] consumption at 0.9V for the cases of 3-2, 4-2 and 5-2 compressors. CMOS design use large number of transistors. By implementing XOR and multiplexers with Complementary Pass transistors Logic (CPL), number of transistors is minimized. Arithmetic circuits performing 8-bit addition, 16-bit addition, 32-bit addition are realized using CPL and are observed to have better power and area parameters.

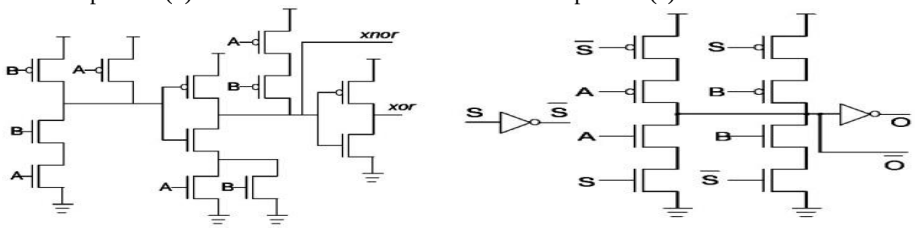
III. 3-2 COMPRESSOR

A 3-2 compressor takes 3 inputs X1, X2, X3 and generates 2 outputs, the sum bit S, and the carry bit C. When X3 = Cin, the 3-2 compressor is called a full adder cell [3].



(a) (b) (c)

Fig 1. (a) Block Diagram of 3-2 compressor (b) Conventional Architecture I of 3-2 compressor (c) Conventional Architecture II of 3-2 compressor



(a) (b)

Fig 2. (a) Implementation of XOR-XNOR Circuit (b) Implementation of Multiplexer Circuit

The Fig.1 shows block diagram and conventional architectures of conventional 3-2 compressor architectures. The figure 2 shows the implementation of XOR-XNOR and multiplexer circuits used in the conventional 3-2 compressor architectures [1], [3], [9]. The conventional architecture I of the 3-2 compressor employs two XOR gates which are implemented using CMOS logic in the critical path. This reduces the speed of the circuit because of high latency of XOR gates. The conventional 3-2 compressor architecture II replaces the second level XOR gate in the conventional architecture II with a multiplexer circuit to get better performance [3].

The proposed architectures of 3-2 compressors are realized using the following equations:

$$Sum = x1 \oplus x2 \oplus x3 \quad (1)$$

$$Carry = (x1 \oplus x2) \bullet x3 + (\overline{x1 \oplus x2}) \bullet x1 \quad (2)$$

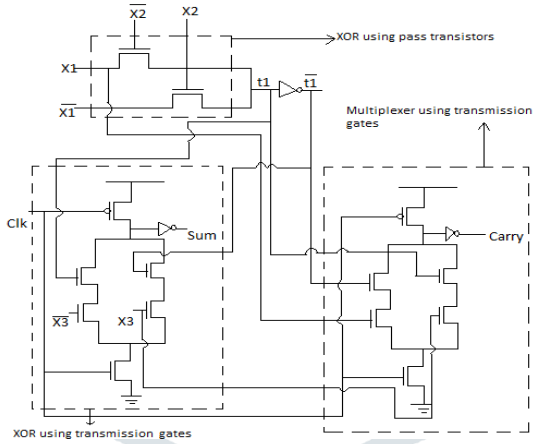


Fig 3. Proposed 3-2 Compressor Architecture I

The proposed architecture I of the 3-2 compressor (figure 3) uses a combination of pass transistors and domino logic. Domino logic is a CMOS logic style obtained by adding a static inverter to the output of the basic dynamic gate circuit. A clock value of clk = 0 is the precharge phase and clk=1 is the evaluation phase. The output of the circuit is always '0' in case of precharge phase as the input to the inverter is '1' (Vdd). The outputs depend on the inputs only when clk = 1. Once a node goes to '0' in a clock cycle, it cannot go back to '1'. It can go back to '1' only after the circuit goes to precharge phase i.e. in the next clock cycle [6]. The domino logic gates are very fast because they contain only one PMOS transistor for every stage. The power consumption for domino logic circuit depends on the clock speed. If the clock speed is more, switching of circuits happens more often and hence the power consumption is more. Domino logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used or refreshed before the charge in the output decrease enough to cause the digital state of the output to change, during the part of the clock cycle that the output is not being actively driven.

The proposed architecture II of 3-2 compressor (Fig. 4) uses NMOS pass transistors and transmission gates. A pass transistor acts as a switch and takes no static current from the supply rails. Thus, power dissipation is small since current only flows on switching. In addition, NMOS pass transistor logic results in lower number of transistors and high switching speed but it gives a threshold loss when sending a logic '1' output [5]. Connecting a transmission gate (or any other logic that gives full swing output) to the next stage of the circuit results in regaining the threshold loss. Transmission gates are used because of their better performance compared to CMOS logic.

Hence, in the proposed architecture II of the 3-2 compressor the first stage is realized by NMOS pass transistors and to regain the loss of swing, transmission gates are used in the second stage. The resultant model can be realized using less number of transistors and therefore, less power consumption and high switching speed.

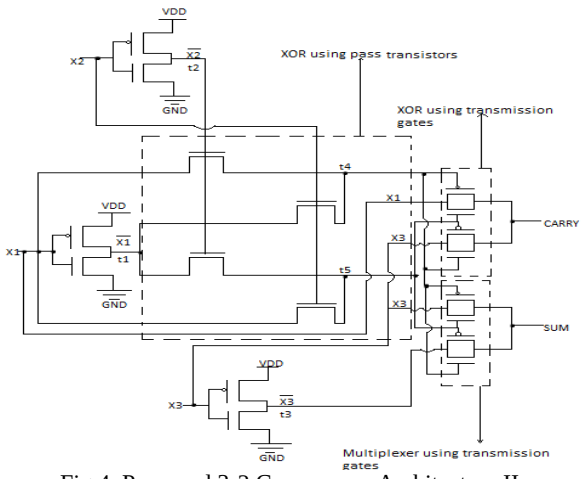


Fig 4. Proposed 3-2 Compressor Architecture II

IV. 4-2 COMPRESSOR

A 4-2 compressor takes 4 inputs X1, X2, X3, X4 and generated 2 outputs the sum bit S and carry bit C along with Carry-in(Cin) and Carry-out(Cout) as shown in below Fig5.

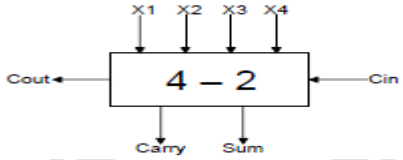


Fig5. 4-2 Compressor block diagram

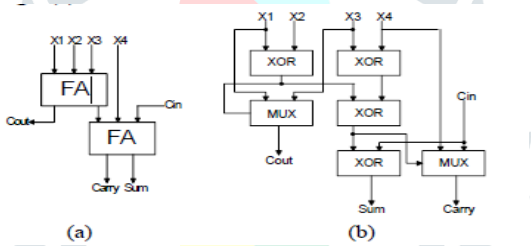


Fig6. Conventional architectures of 4-2 compressor.

The conventional architecture of 4-2 compressor employs 4 XOR gates and is implemented with CMOS logic style. Due to the high latency of XOR gates, the speed of the circuit is reduced. By replacing XOR gates with multiplexer circuits, better performance of conventional 4-2 compressor is obtained.

The proposed architectures of 4-2 compressors are realized using the following equations:

$$Sum=x1\oplus x2\oplus x3\oplus x4\oplus Cin \quad (3)$$

$$Cout=(x1\oplus x2).x3+(x1\oplus x2\ \bar{})\,.x \quad (4)$$

$$Carry=(x1\oplus x2\oplus x3\oplus x4).Cin+(x1\oplus x2\oplus x3\oplus x4\ \bar{})\,.x4 \quad (5)$$

A 4-2 compressor block consists of two 3-2 compressor blocks. Cin is the output from the previous compressor block. Cout is the output to the next stage compressor block. The 4-2 compressor is governed by the equation

$$x1+x2+x3+x4+Cin=Sum+2*(Carry+Cout) \quad (6)$$

In the proposed 4-2 compressor architectures, two 3-2 compressor blocks are joined together. They are two full adder blocks which are realised using logics of pass transistors and transmission gates. Realisation of each full adder block is similar to that of 3-2 compressor. Fig7 shows the implementation of 4-2 using 3-2 compressors.

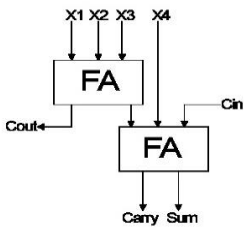


Fig7. Implementation of proposed 4-2 architectures using 3-2 proposed architectures

NMOS Pass transistors and transmission gates are the essential CMOS logic styles used in 3-2 compressors. NMOS Pass transistors are used in first stage whereas transmission gates are used in the next stage of the 3-2 compressor block as shown in Fig8.

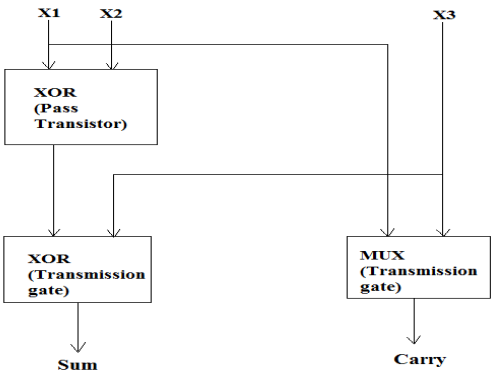


Fig8. 3-2 compressor block with implementation of pass transistors and transmission gates

The reason behind using the CMOS pass transistors in the primary stage is utilization of less number of transistors and high switching speed than that of multiplexers. In addition, NMOS pass transistor acts as a switch. As a result, current only flows by switching and power dissipation is reduced. It gives a threshold loss when it outputs logic 1 and results in some voltage drop. To get back the threshold loss, transmission gates are implemented in the next stage of the full adder circuits. Transmission gates simply work as a bi-directional voltage controlled switch using the complementary properties of NMOS and PMOS transistors. Pass transistors and transmission gates perform better than the other CMOS counter parts and can be widely used [6-9].

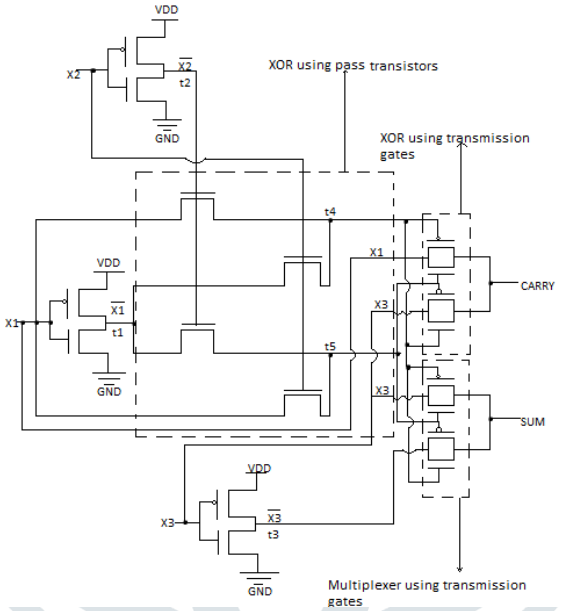


Fig9. 3-2 compressor architecture implemented with pass transistors and transmission gates

Two 3-2 compressor blocks are cascaded as shown in above figure. The resultant proposed model have less power consumption and high switching speed due to less number of transistors and perform better than that of conventional and modified 4-2 compressor architectures[1],[3].

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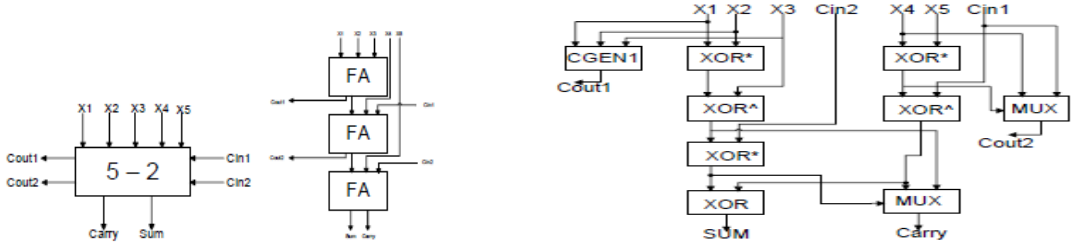
V. 5-2 COMPRESSOR

A 5-2 compressor takes 5 inputs, X1, X2, X3, X4, X5 and two outputs, sum and carry along with Cin1 and Cin2, Cout1, Cout2. The inputs Cin1 and Cin2 are outputs of previous compressor and Cout1 and Cout2 are taken as inputs to the next compressor blocks.



(a) (b) (c)

Fig10. (a) 5-2 compressor block (b) 5-2 compressors using two 3-2 compressor blocks (c) Implementation of XOR-XNOR and multiplexer circuits

The conventional architectures employ XOR gates. Due to their high latency and poor switching speed, the speed of the circuit is reduced. Use of multiplexers in place of XOR gates reduces the utilization of transistor count and increases the switching speed. So, due to this significance, multiplexers are used in the second stage of realisation while designing modified architectures.

The proposed architecture of 5-2 compressors are realised using the following equations.

$$x1+x2+x3+x4+x5+Cin1+Cin2=Sum+2*(Carry+Cout1+Cout2) \quad (7)$$

$$Sum=x1\oplus x2\oplus x3\oplus x4\oplus x4\oplus x5\oplus Cin1\oplus Cin2 \quad (8)$$

$$Cout1=(x1+x2).x3+x1.x2 \quad (9)$$

$$Cout2=(x4\oplus x5).Cin1+(x4\oplus x5\ \bar{}).x4 \quad (10)$$

$$Carry=((x1\oplus x2\oplus x3)\oplus(x4\oplus x5\oplus Cin1)).Cin2+ ((x1\oplus x2\oplus x3)\oplus(x4\oplus x5\oplus Cin1)\ \bar{}).(x1\oplus x2\oplus x3) \quad (11)$$

A 5-2 compressor block consists of three 3-2 compressor blocks cascaded to each other. Cout1 and Cout2 are the input carry bits to the next significant compressor block whereas Cin1 and Cin2 are the output carry bits the previous less significant compressor block. In the proposed 5-2 compressor architectures, three 3-2 compressor blocks are cascaded one another. Each 3-2 compressor is simply a full adder circuits implemented with the logics of NMOS pass transistors and transmission gates.Figure11shows the proposed 5-2 compressor architectures implemented using 3-2 compressor architectures.

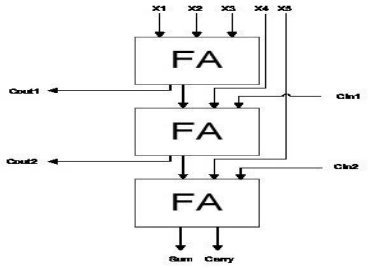


Fig11. Implementation of 5-2 compressors using 3-2 compressor architectures.

Each 3-2 compressor sub circuit has NMOS Pass transistors and transmission gates at subsequent stages. NMOS pass transistors are realised in the primary stage whereas transmission gates are implemented in the secondary stage of each 3-2 compressor sub circuit. Figure 12 shows 3-2 compressor implementation using NMOS pass transistors and transmission gates.

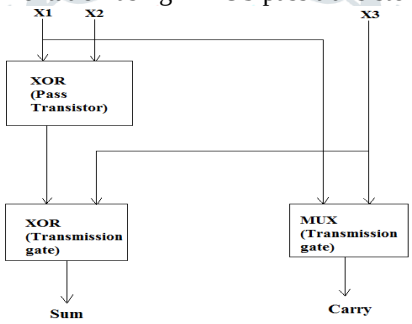


Fig12. 3-2 compressor architectures implementation using pass transistors and transmission gates.

Pass transistors are required to reduce the number of transistors using the complementary CMOS logic. NMOS pass transistor acts a switch. It has the advantage of utilising less number of transistors and high switching speed than the other CMOS counter parts. Another advantage is that it has lower capacitance due to reduced number of transistors. But NMOS devices are poor in pulling the node at VDD. So there exists a voltage drop VDD-Vth when logic 1 is given as output. As a result, threshold loss is obtained in each critical path. To regain the threshold loss, transmission gates are implemented at next stage of realisation. They act as bi-directional switches and perform better than other CMOS logic styles. Fig9 shows the 3-2 compressor architecture. The resultant model has less number of transistors, reduced propagation delay than the conventional and modified models of 4-2 compressor architectures and makes the utilisation of this model more efficient while designing multiplier circuits.

VI. SIMULATIONS

6.1 SIMULATION SETUP:

Simulations are performed using H-Spice Synopsis tools. Simulations are done at 1.8V supply and under 180nm technology. Power consumption and time delay are calculated using features provided in the H-Spice Software. PDP is calculated as the product of Power consumption and time delay.

6.2 SIMULATION RESULTS:

The TABLE I shows the results of the simulation of 3-2 compressors.

TABLE I. SIMULATION RESULTS

Name	Power Consumption (uW)	Time Delay(ps)	PDP(aW-s)
Conventional architecture-I	47.62	193.30	9204.946
Conventional architecture- II	34.17	194.37	6641.623
Proposed architecture-I	11.389	92.03	1048.129
Proposed architecture-II	8.245	69.607	573.944

From the TABLE-I it can be seen that the power consumption of the proposed I and proposed II architectures are 76.59% and 82.69% less than conventional I architecture and 66.6% and 75.88% less than conventional II architecture. This is shown graphically in Fig.13.

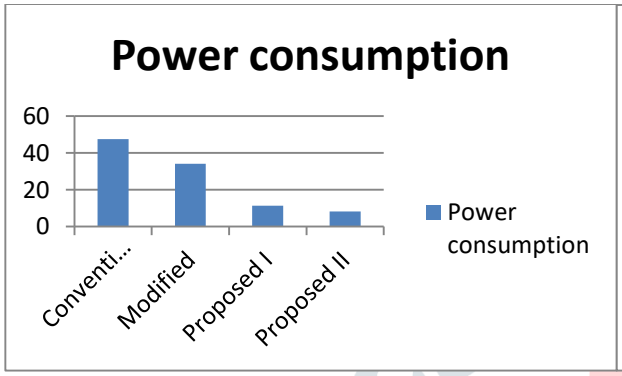


Fig 13. Comparison of Power Consumption

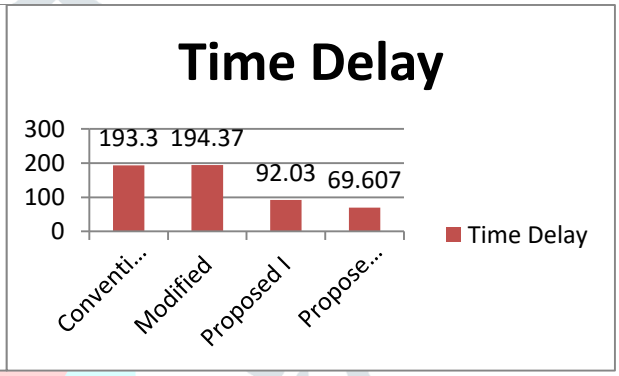


Fig 14. Comparison of Time Delay

From the TABLE-I it can be seen that the delay of the proposed I and proposed II architectures are 52.48% and 63.99% less than conventional I architecture and 52.57% and 64.62% less than conventional II architecture.This is shown graphically in Fig14.

From the TABLE-I it can be seen that the PDP of the proposed I and proposed II architectures are 88.61% and 93.76% less than conventional I architecture and 84.21% and 91.37% less than conventional II architecture. This is shown graphically in Fig 15.

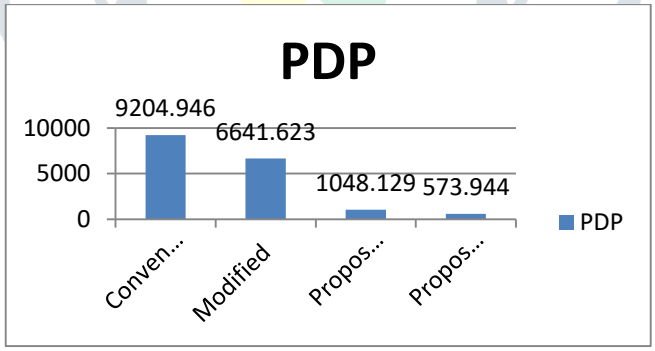


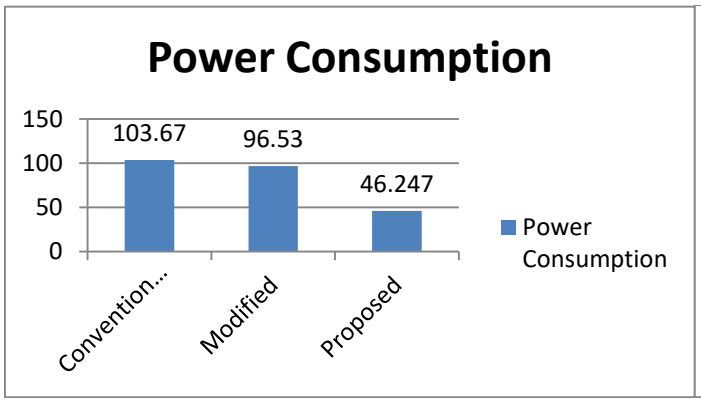
Fig 15. Comparison of Power-Delay Produc

The TABLE II shows the results of the simulation of 3-2 compressors

TABLE II SIMULATION RESULTS

Name	Average Power(uw)	Delay(ps)	PDP(aW-s)
Conventional model	103.67	332.48	34468.201
Modified model	96.5322	255.525	24666.3109
Proposed model	46.247	275.8363	12756.60

From the TABLE II it can be seen that the power consumption of the proposed 3-2 architecture is 55.367% less than the conventional model and 52.37% less than the modified model. This is shown graphically in Fig16.



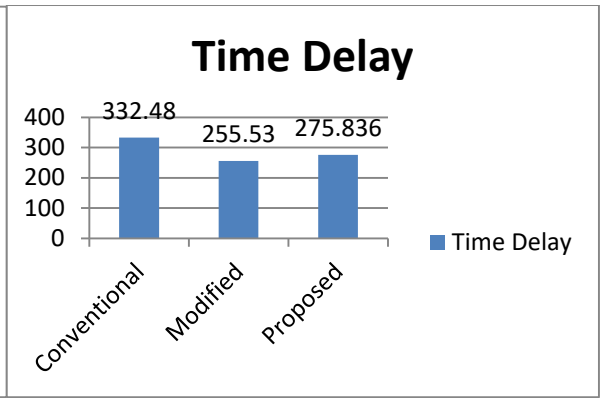


Fig16. Comparison of power Consumption

Fig17. Comparison of time delay

From the TABLE II it can be seen that the delay of the proposed model of 4-2 compressor model is 16.86% less than the conventional model and 7.8% more than the modified model. This is shown graphically in Fig17.
From the TABLE II it can be seen that the PDP of the proposed model of the 4-2 compressor is 62.99% less than the conventional model and 48.28% less than the modified model. This is shown graphically in Fig.18.

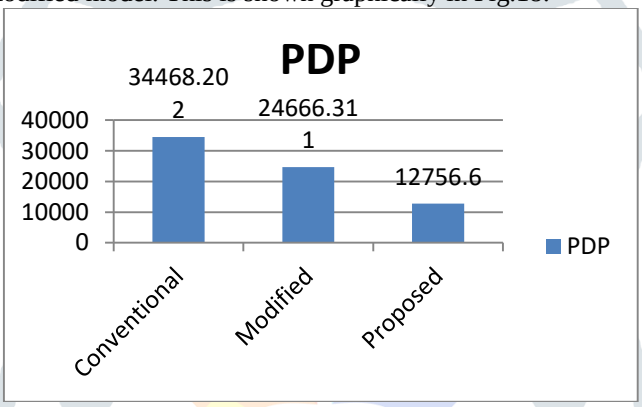


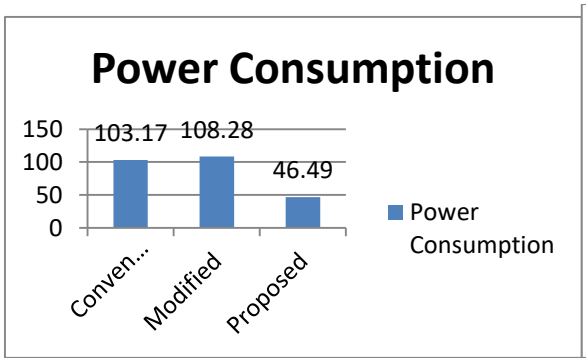
Fig18. Comparison of PDP

Table III shows the results of the simulation of 5-2 compressors.

TABLE3: SIMULATION RESULTS

Name	Average Power(uW)	Delay(ps)	PDP(aW-s)
Conventional model	103.169	546.590	56391.603
Modified model	108.293	286.13	30982.156
Proposed model	46.49	500.255	23256.589

From the Table III it can be seen that the power consumption of the proposed model is 54.93% less than the conventional model and 57.40% less than the modified model. This is shown graphically in Fig19.



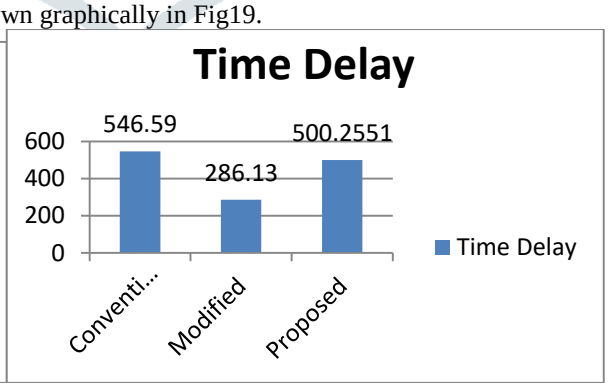


Fig19. Comparison of power consumption

Fig20. Comparison of time delay

From the Table III it can be seen that the time delay of the proposed model is 9.2% less than the conventional model and 74.82% more than the modified model. This is shown graphically in figure 20.
From the Table III it can be seen that the PDP of the proposed model is 58.75% less than the conventional model and 24.93% less than the modified model. This is shown graphically in Fig 21.

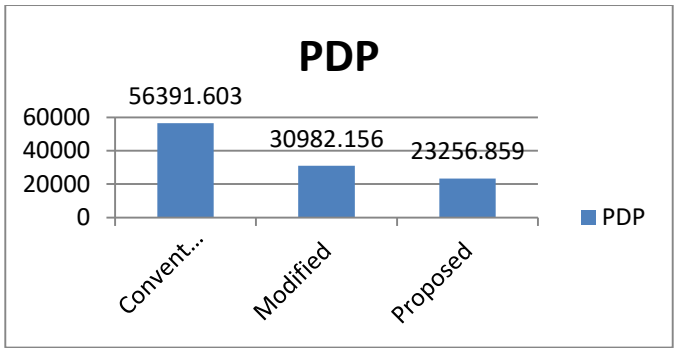


Fig21. Comparison of PDP

VII. CONCLUSIONS

These proposed architectures are implemented in designing higher order compressor architectures. The proposed architectures consisting of pass transistors and transmission gates as their essential elements reduces the power consumption, time delay and PDP than that of conventional and modified architectures. Simulations are performed at 1.8V supply under 180nm technology. Simulation results show that the proposed 3-2 model offer 66.6-82.69% less power and 52.48-64.62% reduction in propagation delay than the conventional 3-2 model. The proposed 4-2 model offer 52.37-55.367% less delay and 7.8-16.86% reduction in propagation delay than the conventional 4-2 model. The proposed 5-2 model offer 54.93-57.4% less power and 9.2-74.82% reduction in propagation delay. Due to all these significant improvements in performance characteristics, they are better choice to prefer in designing multiplier circuits.

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