A Review Paper on Vedic Multiplier

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Abstract : Multiplier is a core element of Digital signal processor(DSP). The speed of the multipliers affects the speed of the Digital signal processors. The execution of most DSPs is dependent on its multipliers, and hence need for high speed multipliers arises. In this digitization era, it becomes necessary to increase the speed of the digital circuits while reducing on-chip area and memory consumption. For increasing multiplication speed and reducing delay there is more and more emphasis on designing faster multipliers. There are many algorithms like standard modified booth algorithm, Wallace tree methods, vedic multiplier and several new techniques designed to enhance the speed of the multiplier. Among this, algorithms based on Vedic mathematics can be used to design faster and low power multipliers.[4] This paper presents study about different Vedic multipliers with different adders and different technologies used in different papers.

IndexTerms **- Vedic Multiplier, Urdhva Tiryakbhyam Sutra., Nikhilam Navatashcaramam Dashatah, Pass Transistor Logic (PTL), Ripple carry Adder, FPGA.**

I. INTRODUCTION

A multiplier is a major element in almost all the processors and contributes to the total power consumption of the system. Multiplication operation is intensively used in digital signal processing applications, so there is a need for high speed multiplier. This paper presents comparative analysis for fast and area efficient multiplier based on Vedic mathematics [1].The Multiplier Architecture is based on the Urdhva-Tiryagbhyam sutra of Vedic Mathematics.

Vedic multiplication algorithm:

From ancient Indian scriptures referred to as Vedas an ancient form of mathematics has been reconstructed which is known as Vedic Mathematics. It has different branches of mathematics like algebra, arithmetic, trigonometry based on 16 sutras of Vedic mathematics.[8] Most generalized sutra which is also used for the implementation of this Vedic algorithm is Urdhva Tiryagbhyam which reduces the number of bits results in reduced area and delays. Vedic Multiplier thus has become very popular for faster computations and analysis. This sutra is based on the principle of Vertical and Crosswise and only utilizes AND gate, Half Adder and Full Adders for multiplication process which saves large amount of processing time Traditionally this method is used to perform fast multiplication of two decimal numbers by using vertical and cross as can be seen in Fig. 1[8]

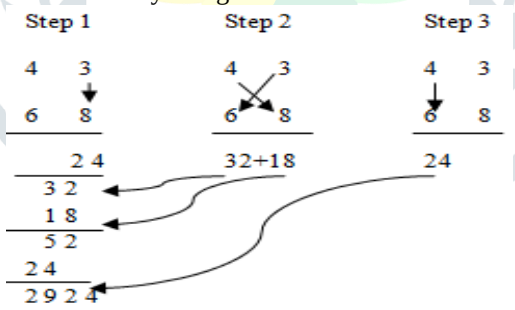


Fig.1-Vedic multiplication of decimal numbers

2 Bit Vedic Multiplier Algorithm Using similar process for 2 bit binary multiplication can be performed in few numbers of steps. Here two 2 bit binary numbers X = X_1 X_0 and Y =Y_1 Y_0 are multiplied using vertical and cross technique. Xo,Yo are multiplied and generate LSB bit of result [8]. Then cross multiplication of X_0 Y_1 and X_1 Y_0 is performed and product terms are added also carry of previous stage is added to this and thus generate next bit of result. At final stage XIYI are multiplied vertically and added with carry of previous stage and then addition is taken as MSB bits of the result. A simple architecture to perform this 2 bit multiplication can be given as shown in Fig. 2[8]

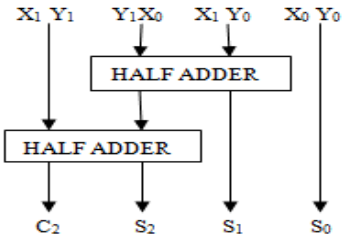


Fig.2-Vedic multiplication of binary numbers

A 4 bit Vedic multiplier algorithm is similar to 2 bit multiplier and implementation is also done with the help of 2 bit Vedic multipliers and adders. To implement this partial product terms are generated using 2 bit Vedic multiplier and then partial reduction and addition step is done with the help of simple adder circuit.Vedic mathematics has the best feature to simplify the complicated calculations in mathematics to a much faster and efficient manner. Vedic mathematics are based on the working of the human mind which reduces calculations by neglecting unnecessary steps, hence it presents effective algorithms which are applicable to many scientific studies.[4]

This Paper is structured as Follows - Various Vedic multipliers with different adders and technologies are described in section II. Finally, The Conclusion and Future Work is given in section III.

II. RELATED WORK

The author Shamim Akhter et al.[1] presented fast and area efficient Vedic multiplier design in this paper. The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics. The adder block used in Vedic multiplier is the main source of delay in overall multiplication operation. [1]

This paper presents logic for Vedic Algorithm based multiplication operation and it deals with different adder topologies. Also Comparative Analysis of Vedic Multipliers using different adder architectures is presented in the paper. The basic module is 2x2 Multiplier. For N x N multiplication, divide the multiplicand and multiplier into two parts, For example, if A& B are two binary numbers then the divided parts of A as AM and AL. Similarly for the input B, it is divided in two parts as BM and BL. Multiplication operation between A and B can be represented as:

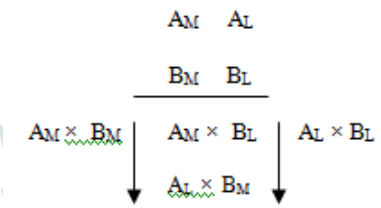


Fig.3- N×N multiplication [1]

These partial products can be generated and added as per structure proposed in paper [1]. The block diagram for 16x16 Multiplication based on Vedic technique as proposed in [1] is shown in Figure 4

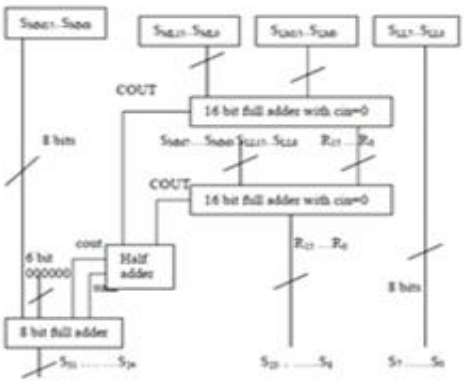


Fig.4- 16×16 multiplication [1]

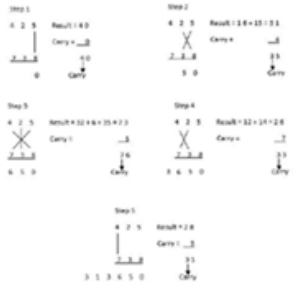
As can be seen that adder is used in the intermediate computation, hence fast and area efficient design will enhance the overall performance of multiplication. In this paper different architectures of adders namely Ripple Carry Adder (RCA) ,CSA , CBL and SQRT-CSA, Modified SQRT-CSA are used to compare the performance of vedic multiplier. A comparative analysis of Vedic multiplier using various digital adders has been presented in this paper. The parameters of comparison were delay, area and power.

The author VijayaLakshmi Bandi [2] presented in this paper the Performance analysis of Vedic multiplier using modified full adder. In this research, Vedic multiplier is designed using modified full adder which consumes less number of LUT's, slices and delay when compared to normal conventional Vedic multiplier. Simulation and synthesis are carried on XILINX ISE 12.2 software. Modified Vedic multiplier consists of three sections. In the first section eight bit multiplicand and eight bit multiplier are portioned into four sets. The proposed methodology is simulated and synthesized on XILINX ISE 12.2and the result analysis shows that the proposed architecture is better in terms of LUT's and slices when compared to conventional architecture.

The author Sanjay S. Chopade et al. [3] presented in this paper Comparative study of 4x4 multipliers with different adders at 32nm in different geometrical devices is done for low power requirement and high speed. In this paper Vedic Multiplier designed with Ripple carry adder(RCA) and carry look ahead (CLA) using SOI and FINFET devices.[3] Comparative analysis of multiplier is carried out on parameters like average power as a function of supply voltage, delay as a function of supply voltage, EDP as a function of supply voltage & process variations variation in power and delay with change in process parameter shows that Finfet based Vedic multiplier with CLA adder is having less process variation than FDSOI based conventional design and multiplier with CLA adder.

The author Nikhil R. Mistri et al. [4] Compared Multiplier using Vedic Mathematics . In this paper multiplier is implemented using "Urdhva Tiryakbhyam" and "Nikhilam Navatashcaramam Dashatah sutra. Multipliers in this paper are coded using Verilog language, it is synthesized and simulated using Xilinx ISE 14.5. Urdhva Tiryakbhyam basically means vertical & crosswise. This sutra of ancient mathematics is used for multiplication in algorithms. Sanskrit definition of Urdhva Tiryakbhyam is vertical and crosswise that means it performs multiplication vertically and crosswise. [4]

Nikhilam Sutra in Sanskrit means all from 9 and the last from 10. It can be applicable in all multiplication cases however it is more effective when higher order number are involved as it breaks the number with the nearest base and then this number is used for the multiplication. As the number is of higher order complexity is reduced.



a * b	105 * 102
A = a – (nearest base)	A = 105 – 100 = 5
B = b – (nearest base)	B = 102 – 100 = 2
C = A * B	C = 5 * 2 = 10
D = a + B = b + A	D = 105 + 2 = 102 + 5 = 107
Result = base * D + C	Result = 100 * 107 + 10 = 10710

Fig.5-Nikhilam Navatashcaramam Dashatah sutra [4]

In this paper, Urdhva Tiryakbhyam and Nikhilam sutra both algorithms are compared in terms of propagation delay and found that Urdhva Tiryakbhyam sutra performs faster for less bit input while Nikhilam sutra is faster for larger inputs.

The author R. raju et al. [5] realized 16-bit multiplier using a Vedic sutra named Urdhva Tiryagbhyam from Vedic Mathematics. The 16-bit multiplier is realized using an 8- bit multiplier which in turn realized by a 4-bit multiplier and so on. Modified Ripple Carry Adders are used to build the multiplier circuit. In this [5] design it is proposed to reduced the number of logic levels, thus reducing the logic delay. Also the area utilized is reduced by the design algorithm. Simulation of the architecture is performed using Xilinx ISIM and synthesized using Xilinx XST. The implementation is done in FPGA Spartan Kit. [5]
Vedic multiplier is faster compared to array as well as Booth multiplier. As the number of bits increases from 8x8 bits to 16x16 bits, the delay timing is reduced greatly for Vedic multiplier when compared to various multipliers. Vedic multiplier has the advantage as compared to other multipliers over delay of the gates and structures regularity. Thus this multiplier performs in the among multipliers which are conventional. It is preferred with high advantage than other multipliers.

The author Shashank S Meti et al. [6] proposed 8-bit Vedic multiplier using modified Gate Diffusion Input (mGDI). 8-bit Vedic multiplier is designed using Urdhva Tiryagbhyam sutra with 4 numbers of 4-bit Vedic multiplier and 3 adder circuits. [6]
In mGDI technique, a wide range of logic functions can be implemented by using a single pair of transistor (1nmos and 1 pmos). This result in reduction of power and area compared to existing CMOS technology.

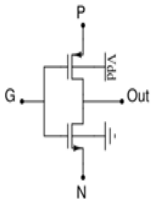


Fig. 5-Basic mGDI cell[6]

N	P	G	Out	Function
'0'	B	A	$\bar{A}B$	F1
B	'1'	A	$\bar{A}$+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	$\bar{A}B$+AC	MUX
'0'	'1'	A	$\bar{A}$	NOT

Fig. 6- Various functions that can be implemented using mGDI cell [6]

The Vedic Multiplier is simulated in cadence virtuos tool using 180nm technology at 1.8V power supply. The 8x8 Vedic multiplier designed is verified for the functionality.[6] AND gate, half adder, full adder, 4x4 Vedic multiplier, Adder-1, Adder-2, Adder-3 and 8x8 Vedic multiplier were implemented based on mGDI technique. The number of transistors, power consumed and delay of these gates is calculated and is compared with that of the conventional CMOS design. It shows that the multiplier built based on mGDI logic results in power, area and delay reduction, the comparison is done with the CMOS design. Power, delay and number of transistors are compared and it is observed that multiplier built with mGDI logic has less number of transistors, reduced delay and power.

The author Pournima Pankaj Patil' et al. [7] provides an optimization technique for the case of constant block size to improve the speed performance. Comparative Analysis of 8 Bit Carry Skip Adder using CMOS and PTL Techniques with Conventional MOSFET at 32 Nanometer Regime presented in this paper.
Following two design logic has been considered for the paper:
1. Static CMOS Logic
2. Pass Transistor Logic
Static CMOS Logic: The very common and popular design style in VLSI design is the Static CMOS logic style. In this, each logic stage is controlled by input signal which contains pull up network and pull down network. The pull up network contains p channel MOSFET devices, whereas the pull down network contains n MOSFET devices. The networks are designed in such a way that the pull down network as well as pull up networks are 'ON' one after other that means they never "ON" simultaneously. This ensures that there is no static power consumption.[7]

In electronics, many logic families are useful in the design of integrated circuits can be described by pass transistor logic (PTL). By eliminating redundant transistors, it reduces the number of transistors which are used to design all types of logic gates. Transistors are used as switches and it passes logic levels between nodes of a circuit, this reduces the number of active devices. Each transistor in series is very low saturated at its output rather than at its input. If these devices are used as a chain in series in a logic path, it is required to recover the signal voltage to the maximum value for conventionally constructed gate. PTL and gate is shown in figure 7.

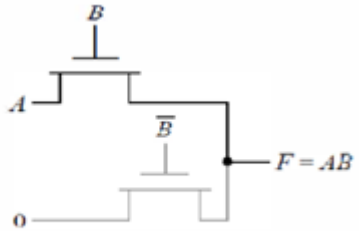


Fig. 7- PTL and gate[7]

In this paper, the performance parameters of delay, average power, PDP and EDP are compared at different techniques. In this paper 8 bit carry skip adder is used. [7] The carry skip adder splits the words which are added into blocks. In every block, Ripple Carry Adder is used to generate the carry and sum bit. Due to the carry computation the Carry Skip Adder minimizes the delay i.e. by skipping over group off a stage. Carry Skip adder is implemented using conventional MOSFET at 32 nm.
All the work has been carried out using Hspice It is observed that the CMOS techniques gives good delay over the PTL logic in supply variation, where as it is observed that the CMOS techniques consumes more power than the PTL, PTL techniques PDP is good and stable, PTL techniques EDP is good and stable over supply voltage variation than the CMOS Technique.

The author Raj Kumari et al. [8] presents an effective Vedic algorithm called as Urdhva-Tiryyagbhyam Sutra implementation and design for multipliers using 45nm technology in this paper. This is an effective design and implementation of a multiplier with high speed, reduced delays, less area and low power consumption using our ancient methodology of Vedic mathematics that is Urdhva-Tiryagbhyam Sutra.[8] For implementation of 2*2 Vedic Multiplier in this paper 45nm technology is used and work is done on transistor level. The whole implementation is done step by step starting from transistor level to module level.[8] Efficient Vedic Multiplier is implemented in VLSI Cadence Virtuoso tool, 45nm technology by using an ancient Vedic algorithm. This multiplier is much faster than that of other conventional multipliers and also consumes low power because of its carry skip addition methodology, reduced hardware and reduced delays.

The author Megha Dogra et al. [9] proposed a VEDIC multiplier “urdhva tiryagbhyam Multiplication” using MCLA (Modified Carry Look ahead Adder). Speed is one of the parameter of any digital circuit so to improve the speed of the multiplication the above mentioned multiplier is proposed and the results are compared with the existing multiplier. The multiplier using Modified carry look ahead circuit is more efficient and lesser delay compared with existing one.
In this paper they replaced last product generating section with CLA (Carry look ahead circuit)in Existing design. So proposed design consisting of existing circuit with MCLA (modified carry look ahead circuit circuit)[9] Each MCLA consist of MPFA(metamorphosis of partial full adder). In MPFA 2 XOR gates and one NAND gate is used and si, gi and pi is generated .That is called sum, generator and propagator section. In MCLA instead of taking Full adder carry output like c=(a^b)cin|ab. Here itself generating carry by taking partial products from MPFA (Metamorpholosis partial full adder). By applying this method number of LUTS reduced and no of slices used is also less.

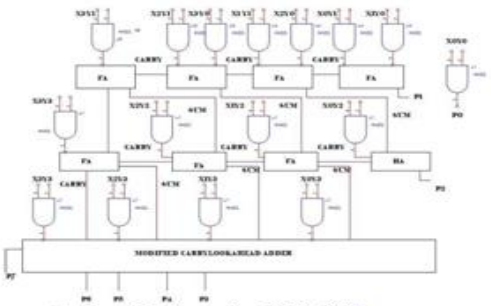


Fig.8-multiplier using MCLA[9]

The proposed multiplier is shown in Fig . Internal circuit of MCLA which consist of four MPFA (metamorphosis of partial full adder) consist of XOR gates and NAND gate .In this circuit partial products has been taken to generate and propagate signal .These generate and propagate has used in look ahead section to generate carry .So we are not consider with carry form first section .We are directly utilizing the propagate and generate to input of look ahead section. So sum will be ignored while using this section in Urdhav Multiplier look ahead section is made of full nand gates. In this paper the proposed multiplier is takes less time to compute the multiplication function when compare to the existing system.

The author Yogendri Anil Kumar Gupta [10] describes a design of fast and low power 8-bit multiplier architecture which implements Urdhva-tiryakbyham sutra of Vedic method of multiplication. The multiplier is designed in 180nm technology using cadence EDA tool and simulated using spectre simulator and found to be working correctly and results have been compared for pre-layout and post-layout analysis. It is shown that implementation of multiplier using the Vedic sutra leads to a very compact layout leading to significantly smaller Silicon area and very small contribution of interconnections to the overall propagation delay of the multiplier.[10]

The multiplication time and power dissipation of a multiplier almost entirely depends on propagation delay and the power dissipation of FA circuits used in the multiplier. For designing a low power and high speed multiplier it is necessary that FA's used in the multiplier must consume minimum power and provide highest speed. In addition to the above, FA should also have equal delay from input to both the outputs i.e. Sum and Carry. This feature will ensure that glitches are minimum. The layout of the proposed 8-bit multiplier has been designed using Cadence Virtuoso in 180nm CMOS technology. The performance of the multiplier was evaluated by simulation with the power supply voltage of 1.8 volt using Spectre simulator in Cadence Virtuoso. Performance analysis of the proposed multiplier is performed using Cadence EDA tool in UMC 180nm technology at 1.8V power supply and parasitic extraction is done using Calibre. The pre-layout and post-layout simulation has been done to analyse the operating speed (i.e. propagation delay) and power dissipation of the proposed multiplier. The transistor count, Layout area and its performance is also compared with existing architectures to show the effectiveness of the proposed architecture. It has been shown that implementation of Vedic multiplication method results in highly compact layout leading to small contribution of interconnections to the overall propagation delay. This is clearly indicated by relatively small difference between prelayout propagation delay and post- layout propagation delay as obtained by simulation. The speed of the proposed multiplier design has been shown to be significantly better than those reported earlier.

III. CONCLUSION

Review on different Vedic multipliers with a different adder and a technology is demonstrated in this paper. It is observed that different technologies like CMOS, PTL, and GDI are used to design a Vedic multiplier to reduce power consumption, to reduce the chip area and propagation delay. Different adders like ripple carry adder, carry look ahead adder and modified carry look ahead adder are used for implementing the Vedic multiplier. But still as Adder is one of the main components used in multiplier. Using fast adder will enhance the overall performance of the Vedic multiplier. Different adders can be implemented using different technologies to improve the performance of Vedic multiplier. Also Vedic multiplier can be designed with different technologies to improve the performance parameters like chip area, propagation delay & power consumption.

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