Design and Performance Analysis of Low Power Digital Circuits in Nanoscale Technology

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Abstract : Scaling down in technology facilitates high performance with less delay, but it also simultaneously increases the power dissipation. Reduction in power dissipation is very crucial because of increasing the demand of battery operated systems and portable devices. Due to scaling down feature of CMOS VLSI circuit, power dissipation is a most challenging issue [1]. The number of transistors is approximately double for every two years [2]. Power dissipation is directly proportional to the square of supply voltage. Scaling down the power supply voltage can significantly reduce the power consumption, but it degrades the performance of the circuit in terms of increased delay. The delay of the circuit is compensated by reducing the threshold voltage of the circuit. Lower threshold voltage in MOS transistors tremendously increases the leakage current. In this paper, first we reviewed a comprehensive survey and analysis of various low power circuit design techniques. The proposed digital circuits are designed by utilizing the merits of DTCMOS (Dual-threshold CMOS), stack and sleepy keeper techniques. The performance of proposed designed circuit is compared in term of power dissipation, delay and power delay product. All simulation are done at a temperature of 27 ^{0}C by using Mentor Graphics Pyxis EDA Tools in 130nm technology.

Index Terms **- power dissipation, DTCMOS, Stack, Sleepy Keeper**

I. INTRODUCTION

Power consumption is playing an important role in VLSI circuit design. In recent year, mainly concentrated on low power design due to increasing the demand of battery operated and portable devices so, it require low power dissipation with high performance such as laptop, mobile phones , hearing machine and communication portable devices. Many circuit designer and researcher solve the problem of power dissipation through many ideas. Digital system containing large number of logic gate around 1,00,000 or more it is fabricated on a single chip so, it require acceptable limited power dissipation[3] .

Power dissipation in CMOS circuit is mainly composed three different types: dynamic, static or leakage, short- circuit power dissipation. The total power dissipated in a CMOS circuit.

$$P_{total} = P_{dynamic} + P_{static} + P_{short-circuit} \quad (1.1)$$

Dynamic power is dissipated by charging and discharging output load of the capacitance. During charging phase, output node of the capacitance is charge from 0 to V_{DD} at the time of charging energy is dissipated from the power supply in the form of heat in conduction of pMOS transistor. During charge down phase, voltage level drop from V_{DD} to 0 so there is no energy is dissipated from the power supply but energy which is already stored in the output capacitance at the time of charging is dissipated in the form of heat in conduction of nMOS transistor.

$$P_{avg} = n.\alpha.f.\frac{1}{2}C_{avg}V_{DD}^2 \quad (1.2)$$

The short - circuit power is dissipated when both pMOS and nMOS transistor are conducting simultaneously at same time for a short duration during switching. There is a short circuit flow due to instantaneous short circuit connection between the ground and power supply. The nMOS transistor are turn on in the circuit when input voltage level is greater than threshold voltage .The pMOS transistor are still on condition until input voltage reaches to $V_{DD} - V_{th.}$

$$P_{short-circuit} = {}^{1}\!/_{12}.k.\tau.F_{clk}(V_{DD} - 2V_t)^3 \quad (1.3)$$

The static power dissipation due to small reverse leakage current and subthreshold current .A VLSI circuit fabricated a large number of transistors in a single chip. The reverse leakage current contributes large power dissipation when transistor is undergoing in standby mode.

Subthreshold leakage current flow in a weak inversion region. The weak inversion region is that region in which gate to source voltage less than the threshold voltage or nearly to threshold voltage of the device. The amount of subthreshold current depends on the carrier diffusion from source to drain region [4].

$$P_{static} = V_{DD}I_{leakage} \quad (1.4)$$

II. LEAKAGE REDUCTION TECHNIQUES

2.1 DTCMOS (Dual threshold CMOS)

DTCMOS technique shown in **Figure 1**it is very attractive technique for minimizing the leakage current in CMOS VLSI circuits. This circuit is consisting of pMOS and nMOS transistor with different (high and low) threshold voltages. Standard CMOS logic

gate consist with low threshold voltage for achieving high speed because switching speed is significant whereas high threshold voltage is used for effectively cut off the logic gates to obstruct the leakage. In active mode, high threshold voltage transistors are turn on and low threshold transistors are operated with small switching power dissipation with sufficient propagation delay. In standby mode high threshold transistor are turn off at that time subthreshold leakage current is generated with low threshold circuitry are strongly cut-off [5].

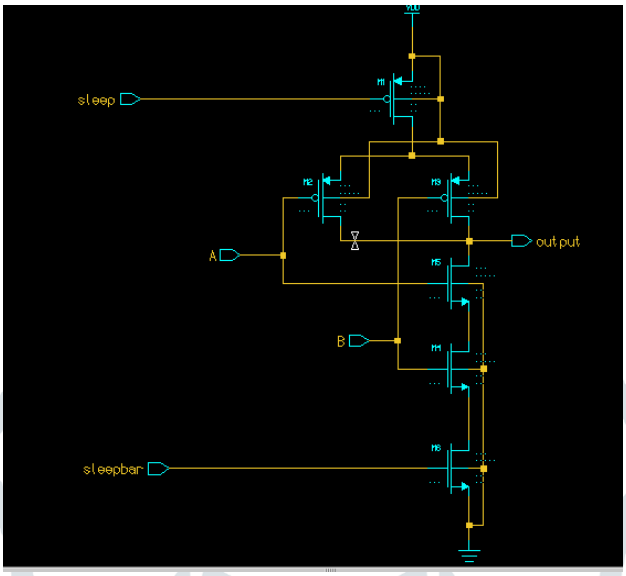

Fig.1 NAND circuit using DTCMOS technique

2.2 Stack approach

In stack approach, a MOS transistor is replaced by two half size transistors shown in **Figure 2**. When two or more transistor of nMOS and pMOS transistors are cascaded subthreshold leakage current is flowing through these transistors are reduces because of increasing threshold of transistor is known as stacking effect.

The leakage current determined by number of off transistor are cascaded is reduces by stacking technique. Thus, it is known as stacking effect or self bias effect. In self bias effect, two nMOS transistor are connected in series is turned off the source voltage of cascaded nMOS transistor is higher than zero as compared to single nMOS transistor which is virtually zero. The subthreshold leakage current in digital circuit such as NAND, AND, NOR and OR depend upon the input vectors which is applied to these gates [6].

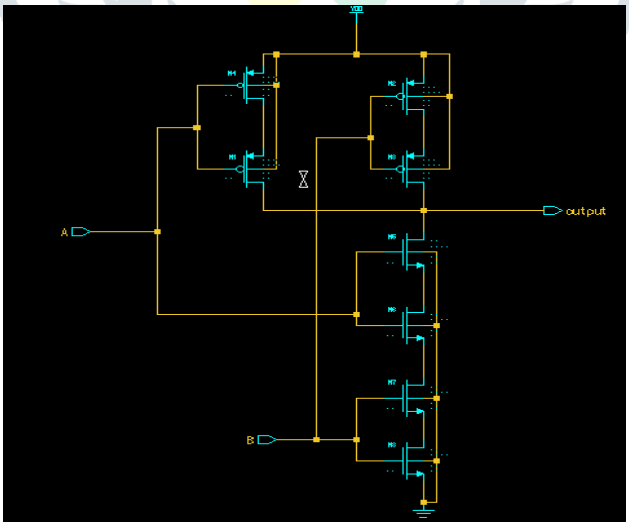

Fig.2 NAND circuit using Stack technique

2.3 Sleepy Keeper approach

Sleepy keeper technique is overcome the data retention problem of sleep technique. Sleepy keeper circuit consist with the nMOS transistor which is parallel to the sleep transistor and pMOS transistor which is parallel to the sleep bar transistor shown in **Figure 3.**These nMOS and pMOS transistor work as helper transistor during sleep mode which maintains sufficient power to retain data. One of them helper transistor are turned on according to the suitable output when high threshold transistor are turned off [7].

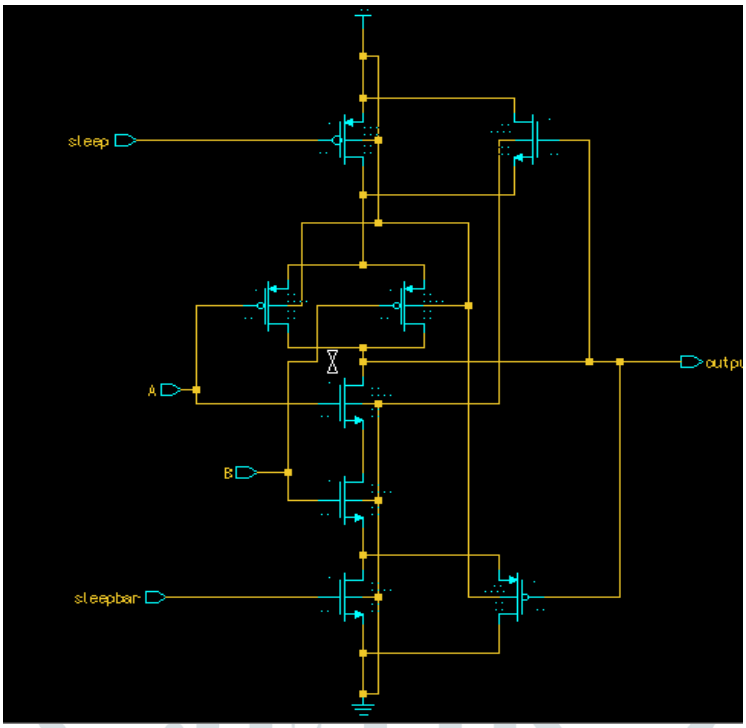

Fig.2 NAND circuit using sleepy keeper technique

III. MULTIPLEXER

Multiplexer is a combinational circuit which is sending more than one analogue or digital signals forwarded to the single output line by the application of control signal. Multiplexer circuit has 2^n input where n is selection line and single output. It converts parallel data into serial data communication [8]. The conventional multiplexer is replaced by pass transistor logic because it is more efficient in terms of low power dissipation, high speed and less area [9]. The multiplexer is implemented with the pass transistor logic it require 6 transistors which gives the advantage of lower capacitance. This circuit is parallel combination of nMOS and pMOS transistor with the gate input of one transistor and has complementary input to the other transistor. The pass transistor is a bidirectional switch is controlled by gate signal. If gate input is zero it select input A and gate input is one it select input B [10].

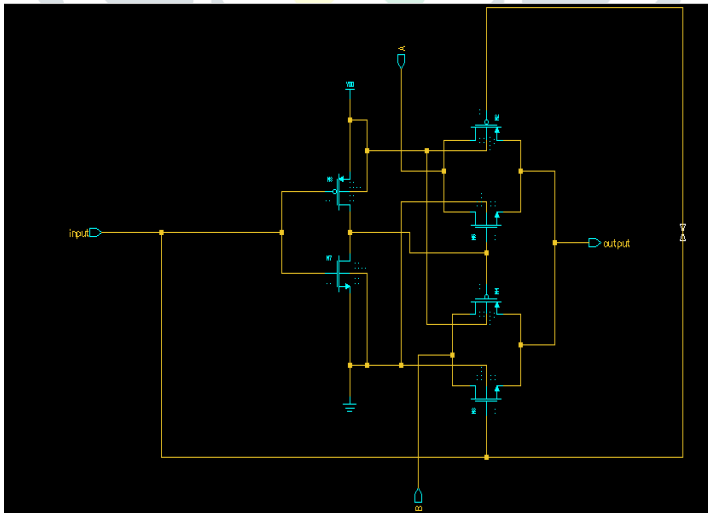

Fig. 4 2×1Multiplexer circuit

IV. PROPOSED CIRCUIT

In this section, we briefly describe about the proposed design and operation of low power structure DTCMOS, Stack with Sleepy keeper .This proposed NAND circuit and 2×1 multiplexer is compared with the already existing circuit such as DTCMOS, Stack, Sleepy keeper and multiplexer. This proposed approach is the combination of the DTCMOS, Stack and Sleepy keeper approaches. Sleep transistor is placed between power supply and pull up transistor while sleep bar transistor are placed between ground and pull down transistor, these transistors are designed with high threshold. Firstly, we discuss operation of proposed

NAND circuit in active mode sleep and sleep bar transistor are turn on which is driven by the complementary signal and low threshold transistor are turn on with small switching time with less delay. Another is stack approach to saving much power by increasing resistance with delay penalty but when we combined both approach it reducing more power with small delay. In standby mode, sleep transistor are turned off and low threshold transistor are forcefully cut-off to prevent leakage and stacking effect also help to block leakage. The nMOS transistor is connected in parallel to sleep transistor and pMOS transistor is connected in parallel to sleep bar transistor which provide appropriate power to retain logic during sleep mode. Consider nMOS and pMOS transistor work as a helper which is driven by suitable output. One of them helper transistor are turn on according to the suitable output.

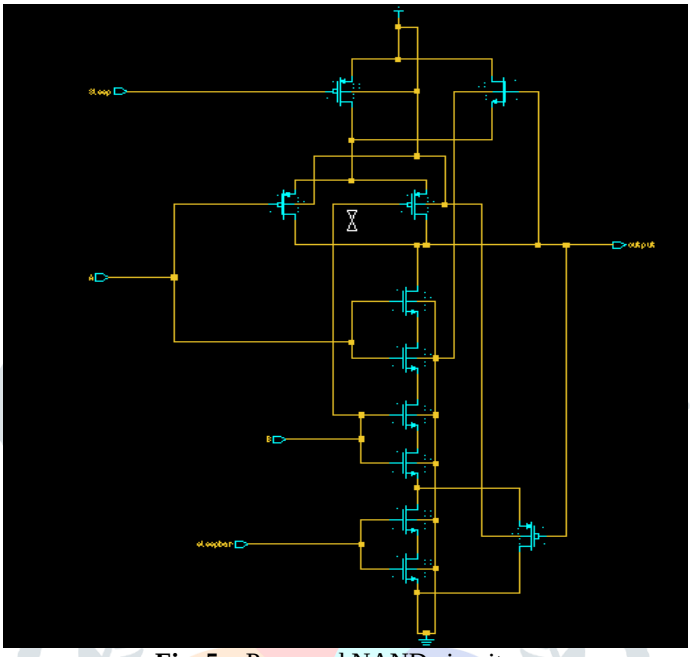

Fig. 5 Proposed NAND circuit

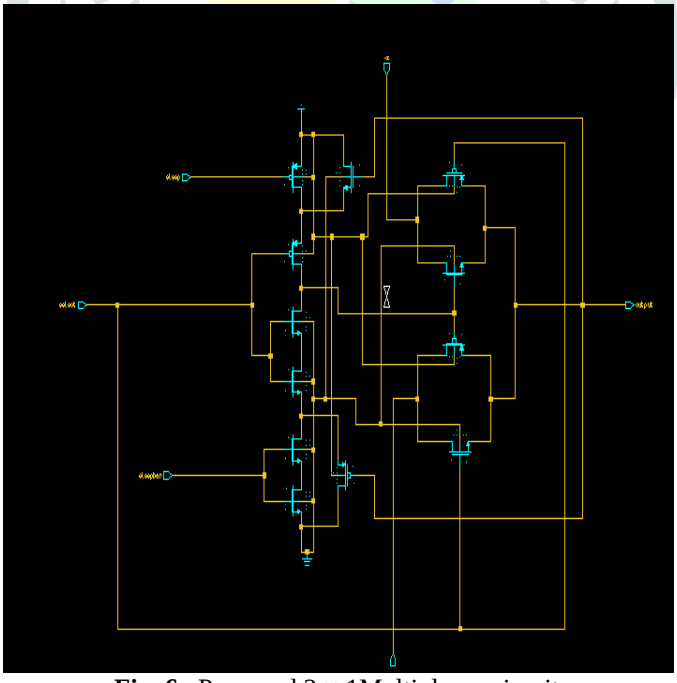

Fig. 6 Proposed 2 × 1Multiplexer circuit

V. SIMULATION RESULT

The simulation of two inputs NAND gate and 2×1 multiplexer with different leakage power reduction technique DTCMOS, Stack and Sleepy keeper. The simulation of all schematic design are performed on 130nm technology at supply voltage 1V,2V,3V to

estimate power dissipation ,delay and power delay product. After analysis of result we conclude that proposed circuit of DTCMOS, Stack and Sleepy keeper give better result as compared to other previous techniques.

Table 1 Performance Comparison at 1V V_{DD}

Technique	Average power(pW)	Static power(pW)	Delay(ns)	Power Delay Product(zs)
NAND gate using DTCMOS	137.8393	3.3325	21.094	459.349
NAND gate using Stack approach	95.5183	3.5009	21.145	2019.734
NAND gate using Sleepy keeper	141.4299	6.8768	21.122	2987.282
Proposed NAND circuit	75.2474	6.8765	21.100	1587.720
2×1 Multiplexer	778.1996	6.0025	0.097405	75.8005
Proposed 2×1 multiplexer	133.1277	9.3370	0.16514	21.9847

Table 2 Performance Comparison at 2V V_{DD}

Technique	Average power(pW)	Static power(pW)	Delay(ns)	Power Delay Product(zs)
NAND gate using DTCMOS	306.2963	13.3325	21.025	6439.879
NAND gate using Stack approach	206.3249	14.0015	21.038	4340.663
NAND gate using Sleepy keeper	320.5000	27.5002	21.039	6742.999
Proposed NAND circuit	167.3621	27.4993	20.916	3500.545
2×1 Multiplexer	3111.50	24.0053	0.088019	273.8711
Proposed 2×1 multiplexer	306.1464	37.3390	0.010607	3.24729

Table 3 Performance Comparison at 3V V_{DD}

Technique	Average power(pW)	Static power(pW)	Delay(ns)	Power Delay Product(zs)
NAND gate using DTCMOS	489.6228	29.9957	20.959	10262.004
NAND gate using Stack approach	325.6476	31.5052	21.003	6839.5765
NAND gate using Sleepy keeper	521.3504	61.8727	20.972	10933.760
Proposed NAND circuit	272.3923	61.8675	20.852	5679.924
2×1 Multiplexer	9694.0	54.0050	0.095283	923.6734

Proposed 2×1 multiplexer	508.1433	84.0059	0.0051293	2.606419

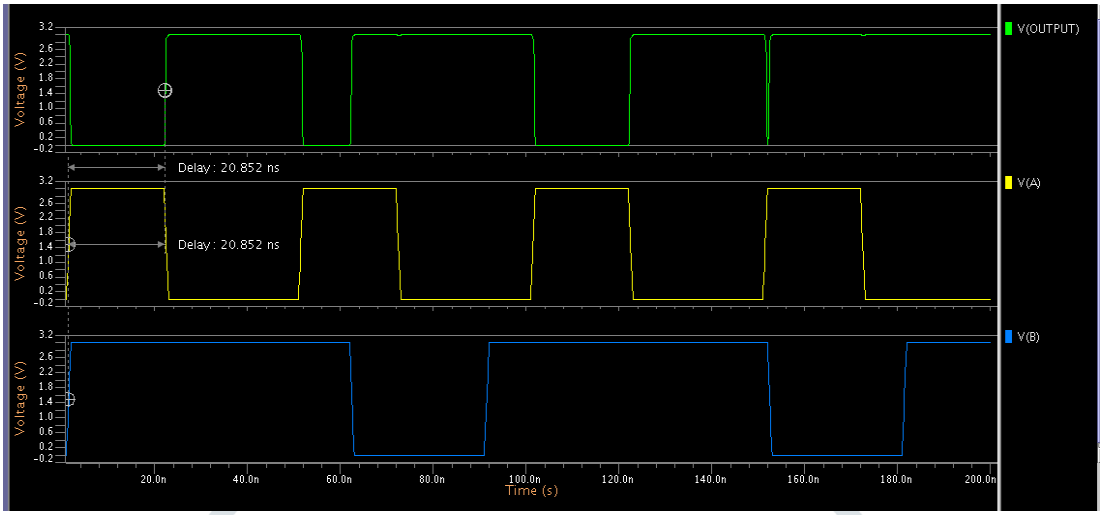

Fig. 7 Proposed NAND circuit

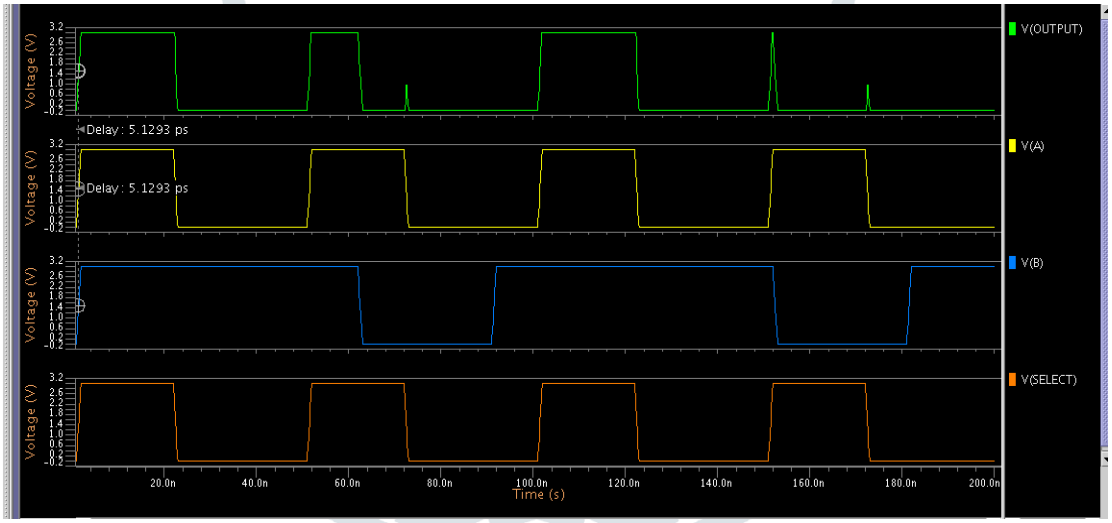

Fig. 8 Proposed 2 × 1Multiplexer circuit

VI. CONCLUSION

Leakage current is major contributor of the overall power dissipation due to scaling down feature of CMOS circuit. To limit the leakage current is a great challenge in nanoscale technology. The proposed technique is a best technique as compared to the already existing technique in terms of power dissipation, delay and power delay product. Th proposed NAND circuit and 2×1 multiplexer circuit also solve data retention problem when circuit undergoing in standby mode.

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