A NOVEL DESIGN OF CSD RECODING WITH FAULT TOLERANT FULL ADDER

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Abstract : Canonic signed digit (CSD) involves very few non-zero bits, designing it for high speed and area optimization in VLSI based DSP architectures. The CSD has been designed with number of adders. Because of faults like struck at faults present in the adders during its operation, there may be a deviation in the expected results. It is very difficult to detect these faults in offline. So that, We proposed CSD with Fault tolerant Full Adder. The ordinary full adder performs addition of bits, but it is not able to detect and correct whenever the faults occurred during the operation. The proposed Fault tolerant Full Adder in CSD play important role to detect the faults with their exact location and also tolerate the faults . In this paper, we present high speed, FPGA fabric aware pipelined architectures for CSD recoding circuits using fault tolerant Full Adder starting from a two's complement number to redundant signed digit input.

Keywords: Canonic signed digit; redundant signed digit; FPGA; carry chain, DFT (design for testability), double fault, Fault tolerance, Full adder, Verilog, Xillinx14.5.

I. INTRODUCTION

Canonic signed digit (CSD) representation is characterized by sparse and non-adjacent occurrence of non-zero bits,results in high speed, area efficient VLSI DSP architectures [1]. This property has significant research efforts in designing efficient VLSI architectures to facilitate conversion of two's complement or redundant signed digit (SD) numbers to their equivalent CSD form [2], [4]. Modern day FPGAs are susceptible to manufacturing defects and transistor aging owing to bias temperature instability and hot carrier injection, primarily due to substantial downsizing of logic nodes for increased logic integration within a single FPGA chip without appreciable augmentation in the chip size [6].

With technology advancement, the complexity of circuit increases results in increase the occurrence of the faults. The existence of these faults can deviate the functionality of overall system. Now a days, the integrated circuits with smaller sizes are more prone to transient faults due to electromagnetic noises, crosstalk and power supply noises. [1-3]. These faults can detect online by using the concept of design for design for testability and fault tolerance. Fault tolerant system performs two functions - detection and correction of the faults. The design can perform these functions with minimum hardware and area requirements [4-5].

Arithmetic operations are regularly used in VLSI circuits. Addition is a primary operation performed in many systems such as DSPs and microprocessor. There is a proposed design of adder improves the performance of system. So, the design of faster and reliable adder is necessary in such systems. There are many approaches to achieve the fault tolerance in circuits. The researchers have introduced the concept of redundancy to detect the faults in circuits. But in order to detect and tolerate the faults there is need of an efficient fault tolerant full adder.

A. Fault Tolerance

Fault tolerance is the capability of the system to continue performing its functions even one or more faults or failures occurred in components. Implementation of fault tolerance technique depends on faults, design, configuration and application of the system. The faults can be classified into different type- hardware or software. Hardware faults are permanent, transient, stuck-at faults occur in the system. It is essential to detect and fix these faults online. For detection and fixing the faults there is need of fault tolerant design which is reliable and have less area overhead and power requirements [7-10].

B. Redundancy

There most common approaches to design a fault tolerant system is redundancy. In hardware redundancy, there is need of extra hardware to detect and tolerate the faults. The redundancy technique is N- modular redundancy [11]. For N = 2 there is DMR (double modular redundancy) in which one extra full adder is used along with the original full adder to detect the faults as shown in Fig.1. Outputs of both are compared by using XNOR gates and if they are not equal then it shows there is fault in the circuit. It has 200% area overhead requirements.

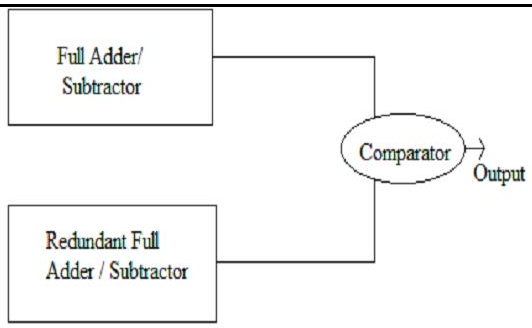

Fig.1 Double Modular Redundancy

likewise for N = 3, TMR (triple modular redundancy) in which two redundant full adder is used along with the original full adder or full subtractor as shown in Fig.2. The output of three can be compared by using XNOR gates and if two generate the same output then the output of third also considered as faulty. A fault condition is there if output of any two modules is different from the third module. It also requires 300% area overhead. This technique can detect the faults but can't able to repair the faults [12]. So there is need of fault tolerant design which can detect and repair these faults.

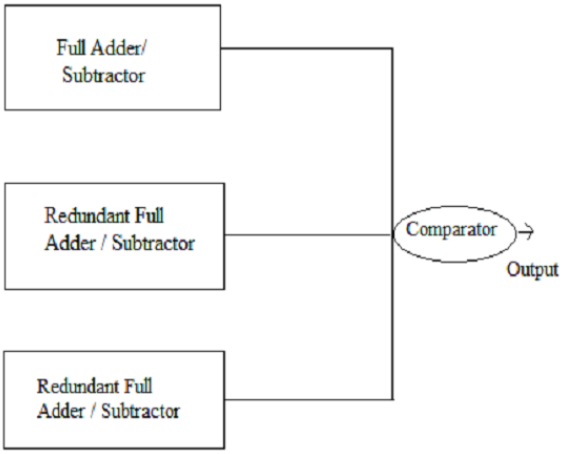

Fig.2 Tripple Modular Redundancy

Implementation of fault detection and fault correction techniques on FPGAs have gained momentum [7]–[9]. In this paper, we have targeted the configured to append fault tolerant full adder for the CSD recoding circuits. The following are the main
contributions of the paper:

- We have proposed fault tolerant full adder .
- Pipelined two's complement to CSD recoding circuit with fault tolerant full adder using RC scheme.
- Pipelined architecture for redundant binary to CSD recoding with fault tolerant full adder using RC scheme.

The rest of the paper is organized as follows. In Sec. II, we elaborate fault tolerant full adder and proposed CSD recoding architectures with fault tolerant full adder amenable to FPGA implementation. The results and discussions are presented in Sec. III. We conclude in Sec. IV.

II. EXISTING CSD RECODING ARCHITECTURES

2.1 Two's Complement to CSD Recoding Architecture

The CSD encoding $\{Y_{id}, Y_{is}\}$ = "00" for '0', "01" for '1' and "10" for '-1' is followed [3]. The conversion algorithm dictates replacement of a string of 1's ranging from index position i to $i + j - 1$ with a "1" at position $i + j$ and a 1 at position i. If X is a two's complement number, the Boolean logic governing the above functionality necessitates generation
of a carry equivalent signal $c_{i+1} = X_{i+1}X_i + (X_{i+1} + X_i)c_i = (\overline{X_{i+1} \oplus X_i})X_{i+1} + (X_{i+1} \oplus X_i)c_i$ Such logic forms are amenable to multiplexer based mapping of the carry chain, as shown in Fig. 1(a). The second logic level computes the CSD recoded bits as $Y_i^d = \overline{X_{i+1}}((X_i \oplus X_{i+1} \oplus c_i) \oplus X_{i+1}) = \overline{X_{i+1}}(X_i \oplus c_i)$ and $Y_i^s = X_{i+1}((X_i \oplus X_{i+1} \oplus c_i) \oplus X_{i+1}) = X_{i+1}(X_i \oplus c_i)$ using dual output LUTs whose outputs are registered using FFs available in the same slice as that of the
LUTs, also shown in Fig. 3.

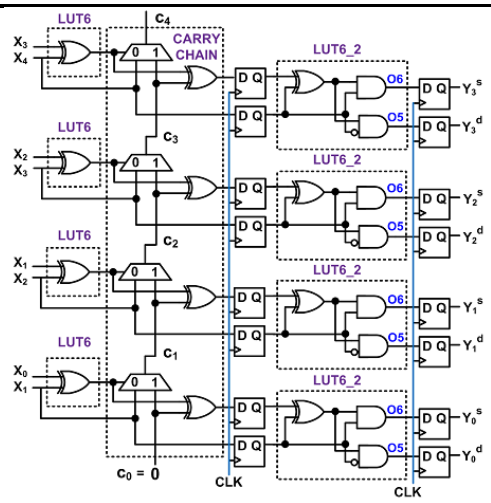

Fig.3. Proposed pipelined architectures for two's complement to CSD recoding using RC

2.2 Redundant SD to CSD Recoding Architecture

Redundant SD to CSD recoding necessitates a two step conversion: redundant binary SD to two's complement number followed by CSD recoding. We assume the input bit representation (S_i, D_i) for the RB digits $X_i \in \{0, 1, -1\}$as $\{(0, 0), (0, 1), (1, 0)\}$ respectively [6]. The circuit may be realized as an adder with initial carry $e_0 = 1$, and input operands $(\overline{S_i}D_i, \overline{S_i})$. The output carry computation $e_{i+1} = \overline{S_i}D_i(S_i + D_i) + e_i(\overline{S_i + D_i})$ is amenable to carry chain implementation. The sum bits are computed as $X_i = (\overline{S_i + D_i}) \oplus e_i$, and are registered prior to sending them as inputs to the two's complement to CSD recoder circuit, which is implemented identically as described in Sec. II-A.2.2.The complete three stage pipelined architecture is shown in Fig. 4.

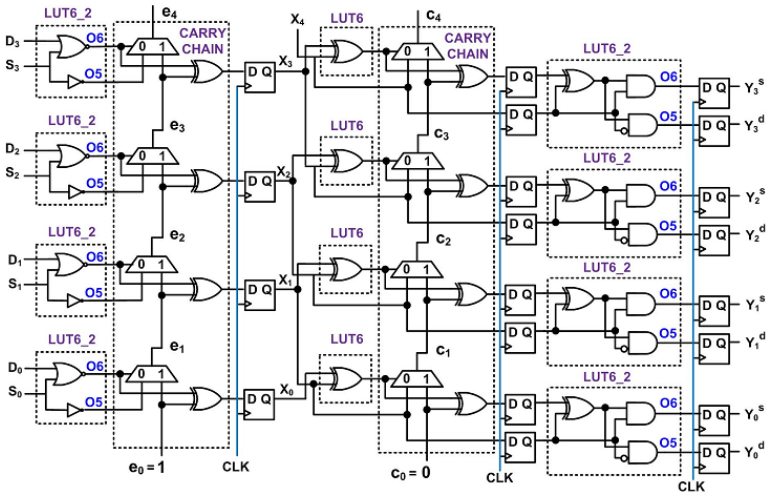

Fig.4. Proposed pipelined architectures for redundant binary to CSD recoding using RC

III. PROPOSED CSD RECODING ARCHITECTURES WITH RC USING FAULT TOLERANT FULL ADDER (FTFA)

3.1 DFT (design for testability) for double fault

In CSD, adder is most important component which perform operations with three inputs. The fault tolerant circuits which are shown further have the ability to detect and correct the faults. Following are some design with can detect faults in adder and subtractor.

The author in [8] proposed a self checking adder which can detect the faults. There is another proposed fault tolerant adder having different functional unit F1 as shown in Fig.5. It can be proposed by using one XOR, four XNOR gates and functional unit. The gate X1, X2 are used to detect the fault in sum output bit and the gate functional unit F1, gate X3 are used to detect the fault in C_{out} output bit. The gate X4 and X5 gives the final outputs F_s and F_c and truth table is show in the table 1.

$$X1 = A \oplus Cin$$
$$X2 = (Sum \oplus B)'$$
$$X3 = (C_{out} \oplus B)'$$
$$F1 = A\ B'\ C_{in} + A'\ B\ C_{in}'$$
$$F_s = (X1 \oplus X2)'$$
$$F_c = (X3 \oplus F1)'$$

Table.1.Truth table of adder with DFT for Double Fault

A	B	C_{in}	Sum	C_{out}	X1	X2	X3	F1	F_s	F_c
0	0	0	0	0	0	1	1	0	0	0
0	0	1	1	0	1	0	1	0	0	0
0	1	0	1	0	0	1	0	1	0	0
0	1	1	0	1	1	0	1	0	0	0
1	0	0	1	0	1	0	1	0	0	0
1	0	1	0	1	0	1	0	1	0	0
1	1	0	0	1	1	0	1	0	0	0
1	1	1	1	1	0	1	1	0	0	0

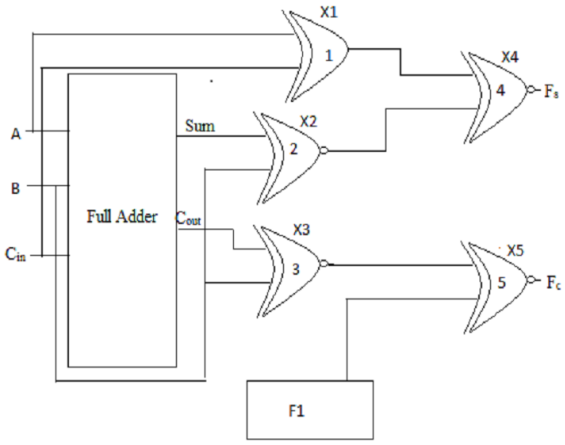

Fig.5 Full Adder with DFT for double fault

In this design, if Fc and Fs is 0 then it indicates fault free condition and if it shows 1 then there is fault in the circuit.

3.2 Fault tolerant full adder

The fault tolerant design is used for repairing the faults which are detected during testing process. The design can repair single and the double faults. The author in [11] designed a self repairing circuit to repair the faults in adder. In fig.6 there is tolerant circuit in which value of Sum output bit is selected by the multiplexer under the control of F_s and value of C_{out} is also selected by the multiplexer according to F_c bit. If value of F_s is 0 then Sum output bit is selected by the multiplexer and Similarly If value of F_c is 0 then C_{out} output bit is selected by the multiplexer and If F_c is 1 then multiplexer selects the inverted value of C_{out} output.

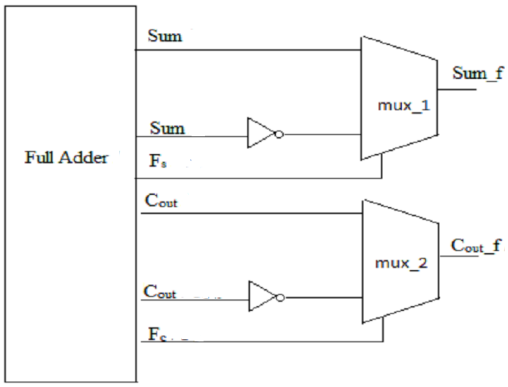

Fig.6. Fault tolerant full adder (FTFA)

3.3 Two's complement to CSD Recoding Architecture using RC scheme with Fault tolerant Full Adder (FTFA)

The redundant SD to CSD with FTFA using RC adder is shown in the figure 7. We are replacing ordinary full adder with fault tolerant full adder only and the remaining circuit is same. The main role of fault tolerant full adder is to detect and correct the outputs if there is any fault present. If the full adder produces the output without fault, the same result is transmitted to the input of CSD. If the full adder outputs are wrong due to the faults present in the circuit, those outputs are given to the separate inverters to get original value and then transmitted to the CSD section with the help of multiplexer operation based of condition.

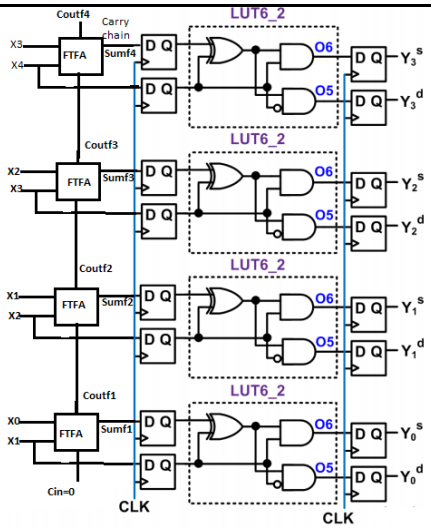

Fig.7. Proposed Pipelined two's complement to CSD recoding circuit with RC using FTFA

3.4 Redundant binary to CSD Recoding Architecture using RC scheme with Fault tolerant Full Adder (FTFA)

The redundant to CSD recoding architecture with RC using FTFA is shown in the figure 8. In the first stage, the binary data with signed digit is given to the binary to two's complement converter same as in existing system. The two's complement result is given to the RC using FTFA in order to detect the faults. If there is a fault present in the RC adder, the FTFA automatically detect and correct the faults and gives exact outputs to the CSD input for conversion.

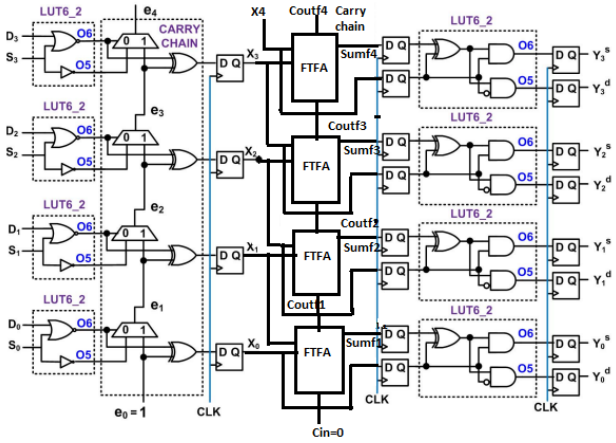

Fig.8. Proposed pipelined architectures for redundant binary to CSD recoding with RC using FTFA

IV. SIMULATION RESULTS AND DISCUSSION

4.1 Fault tolerant full adder (FTFA)

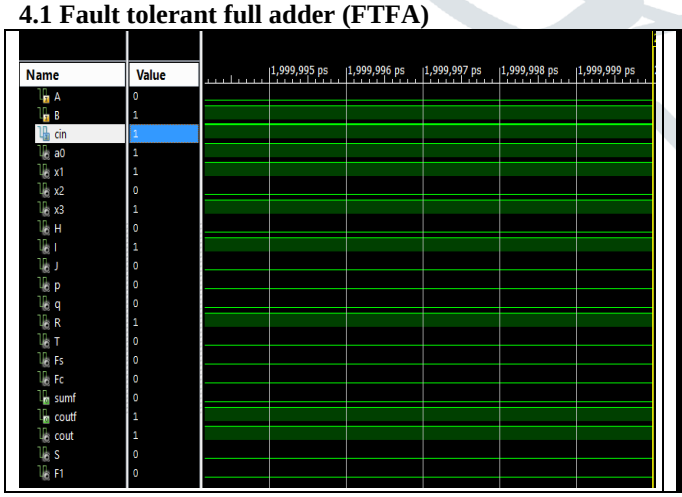

Fig.9. Fault tolerant full adder

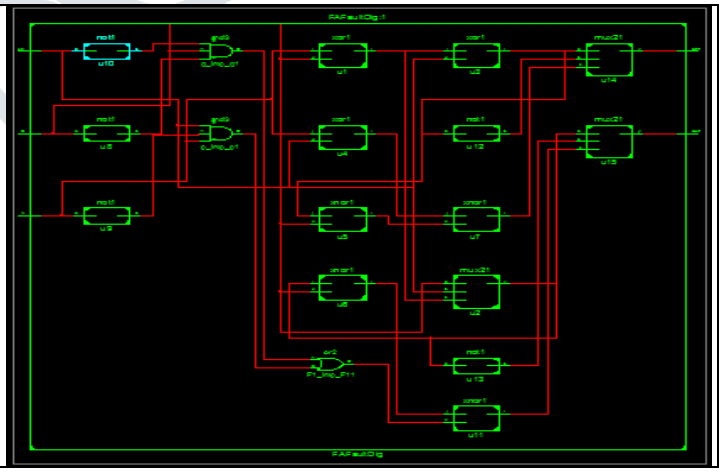

Fig.10. RTL of Fault tolerant full adder

The Fault tolerant full adder outputs sumf and coutf are 0 & 1 when three inputs are 110. In the result, Fs and Fc are 0 for fault free circuit other wise 1.The delay of this design is 5.75ns.

4.2. Redundant 2's complement to CSD Recoding Architecture using RC scheme with Fault tolerant Full Adder

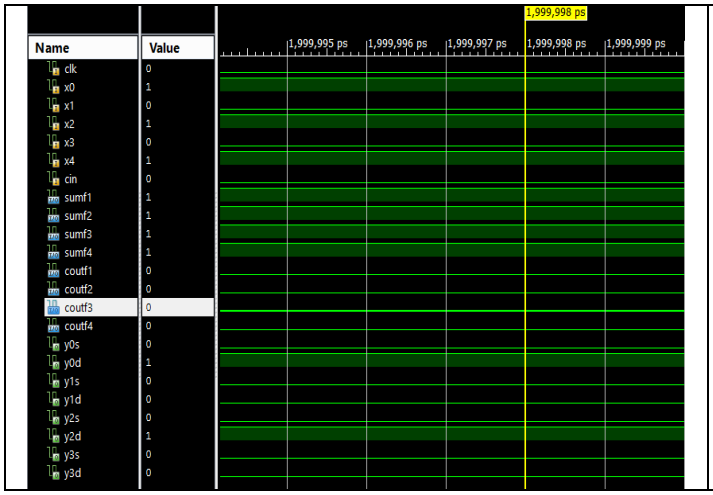

Fig.11. Simulation result of Two's Complement to CSD

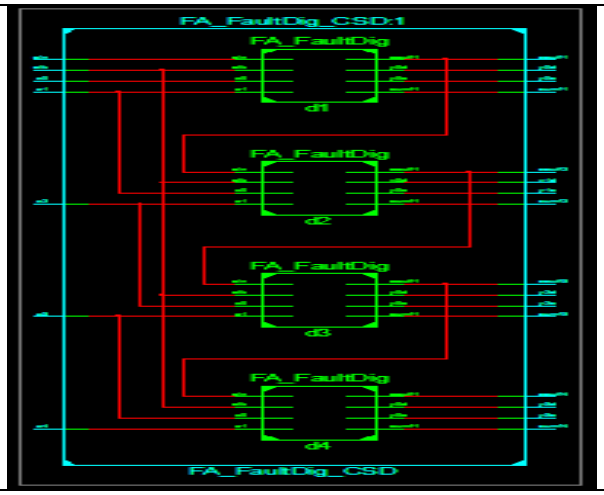

Fig.12. RTL of SD to CSD

In the simulation result, the twos' complement value is 10101 and outputs are 01,00,01,00 for input carry 0.The delay of this design is 7.11ns.

4.3 Redundant binary to CSD Recoding Architecture using RC scheme with Fault tolerant Full Adder (FTFA)

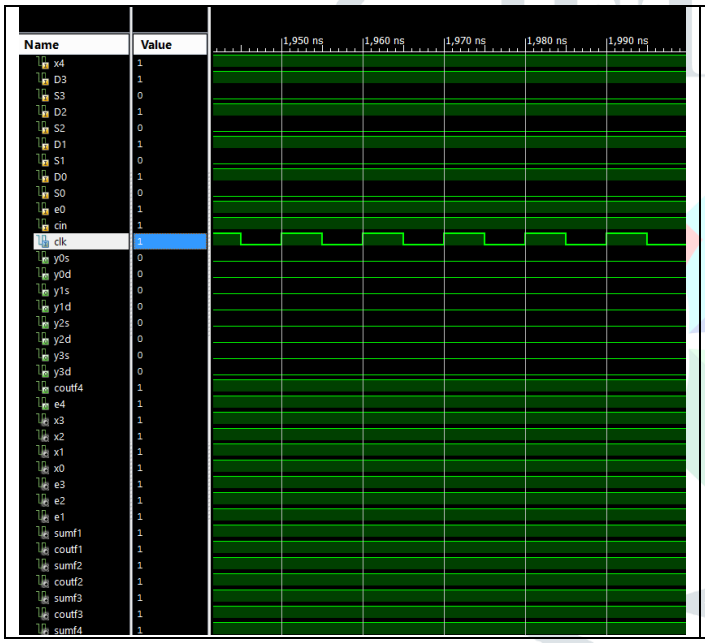

Fig. 13 Simulation result of Binary to CSD

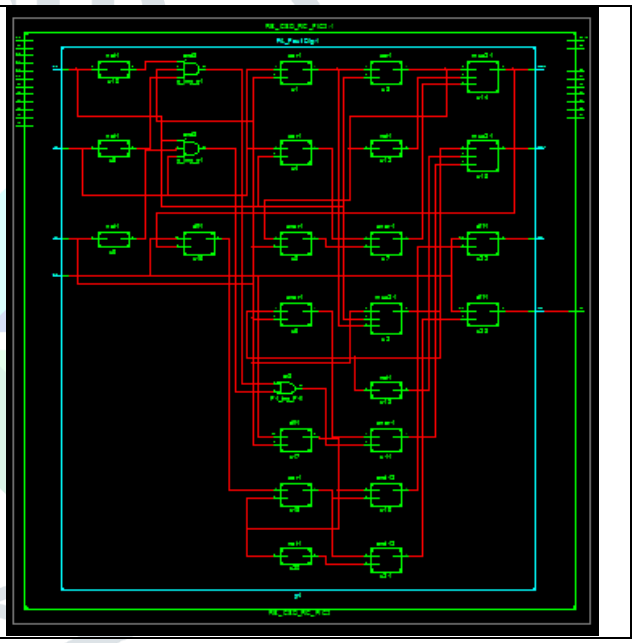

Fig.14. RTL of SD to CSD

In the simulation result, the input is sign with data is 01,01,01,01,01 and outputs are 00,00,00,00 and the delay is 7.19 ns.

Table 2. Design Summary of Proposed and Existing System

	Existing System				Proposed System			
	FA	RCA	2'S COMP TO CSD	Binary to CSD	FTFA	RCA	2'S COMP TO CSD	Binary to CSD
Slices	1	4	9	12	1	5	9	12
FFs	-	-	16	20	-	-	16	20
LUTs	2	8	8	17	1	9	8	17
IOBs	5	14	19	20	5	14	23	22
Delay(ns)	5.77	7.05	7.09	8.84	5.75	7.19	7.11	8.84

The delay of proposed system and existing system of various designs are approximately same as shown in the table 2 From this table, we can conclude that proposed system is more efficient than existing system if the fault are present in the circuit.

V. CONCLUSION

In the existing system CSD design, the faults are unable to detect and correct during the adder operation. So that, the accuracy of the existing system is not good during the faults. To overcome this problem, We proposed CSD recoding circuits with RC using Fault Tolerant Full Adder. This design is simple and attractive in their architectural description. It can be realized from the bit-sliced design paradigm in the form of ILAs and are amenable to forward path pipelining with no requirement of staging delays to synchronize input and output arrival times. The fault tolerant full adder design detect and correct the faults in the outputs with less area overhead. They extensively use the carry chain circuitry leading to high speed realization. The percentage of under-utilization of the inputs to the configured LUTs was optimum to insert fault detection and correction circuitry, which is of emerging importance owing to the susceptibility of modern day ICs to various reliability hazards. Choice of the appropriate fault detection and correction circuitry without incurring logic overhead is strongly dependent upon how the original circuit is configured in the FPGA logic.

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