# Feedback Loop based Energy Efficient Hybrid 1-bit Full Adder

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***Abstract :*** **A new hybrid energy efficient 1-bit full adder is presented in this paper which utilizes feedback loop-based circuit to enhance performance of the 1-bit full adder. The proposed circuit is designed for low delay and power dissipation thereby enhancing overall performance of the adder. The proposed work utilizes feedback-loop based XOR and MOD-GDI (Modified Gate Diffusion Input) technique which requires only 14 transistors. The design is simulated using 180nm MentorGraphics Eldo simulation tool. Simulation results show an improvement of 67% in power dissipation and 2% in PDP ( at 1.0V). Further an improvement of 91% and 85% improvement is observed in power dissipation and PDP (at 5V) respectively.**

***Keywords:*** **Full Adder, Power, Delay, Power-Delay Product (PDP).**

## I. INTRODUCTION

In the last few decades, there is an exponential increase in the battery operated hand-held devices. These devices primarily demands faster operation, lower power dissipation and higher accuracy during mathematical operation such as addition, subtraction, multiplication and division [1-3]. Among all these operation addition plays an important role and used in various other operation such as digital signal processing, Fourier transform, wavelet transform etc. Therefore, researchers are focused in designing low power and high performance 1-bit full adder. This could be achieved by diminishing the count of transistors and optimizing power dissipation by proper logic styles [4-5]. In this paper, a hybrid full adder is design which consists of three modules: Module 1 is feedback based XOR-XNOR gate. Module 2 and Module 3 are MOD-GDI based XOR and multiplexer (MUX) circuits which provides SUM and Cout respectively. The paper consist of 4 sections: Section 1 explains the underlying concept of full adder, section 2 discusses different module used in designing full adder. The results and output waveform are illustrated in section 3 followed by inferences and conclusion in section 4.

## 2. PROPOSED FULL ADDER

1-bit full adder performs addition of three binary number and yields SUM and Cout outputs. The logical structure and equation for designing full adder is given in Fig. 1 and table 1.

TABLE 1
LOGIC EQUATIONS FOR 1-BIT FULL ADDER

| | |
|---|---|
| *SUM* | $(A \oplus B) \oplus Cin$ |
| *Cout* | $HC_{in} + \bar{H}A$ |

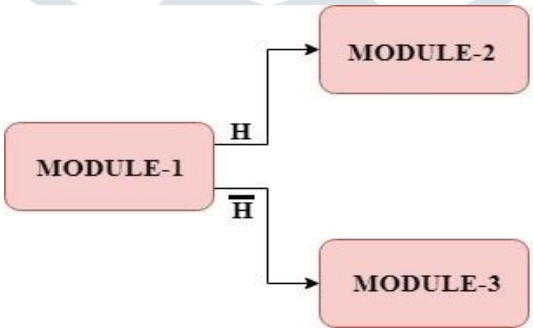


Fig. 1. Logic structure for 1-bit full adder.

It can be assimilated from table 1 that XOR-XNOR cell plays an important role in full adder design and therefore it is important to optimize XOR-XNOR cell. This is achieved through a feedback loop used in traditional XOR-XNOR cell and represented as module 1 [6]. This technique curtails the power dissipation and decreases delay in the circuits during operation. The module 1 takes two inputs namely *A* and *B* and provides *H* and $\overline{H}$ as outputs. *H* is feeded as input to module 2 where it performs XOR operation with *Cin* and provides SUM output whereas $\overline{H}$ is multiplexed with *A* and *Cin* in module 3 to give Cout. Module 3 is also MOD-GDI based multiplexer. Hence both output for full adder is obtained as SUM and Cout by synthesizing all module. The proposed circuit for full adder by synthesizing all the modules is provided in the Fig. 2.

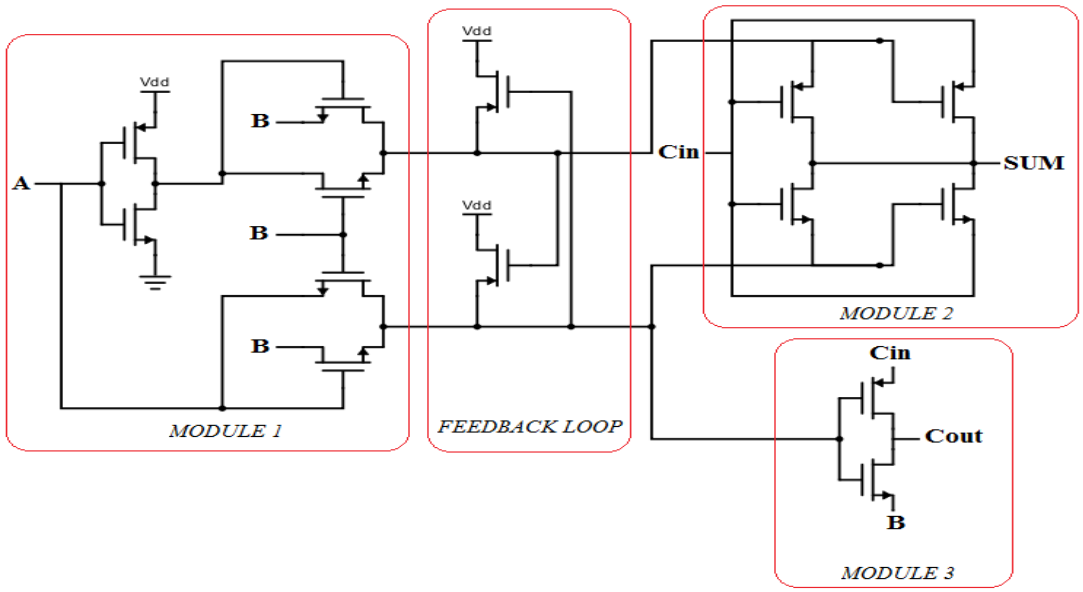


Fig. 2. Proposed circuit of 1-bit hybrid full adder.

## 3. SIMULATION AND RESULTS

The proposed hybrid full adder is simulated using MentorGraphics Pyxis Eldo simulation tool in 180nm technology. The circuit is simulated at 27ºC and at 100 Mhz frequency. The proposed circuit takes only 14 transistors as compared to 14T[7] and 16T [8] full adder which utilizes 14 and 16 transistors respectively. The performance parameter such as power dissipation and delay is taken for voltages ranging from 1V to 5V. It is observed that the 67% reduction in power dissipation and 2% enhancement in PDP (at 1V) whereas 91% reduction in power dissipation and 85% enhancement is observed at 5V power supply. The results for various performance parameters are listed in table 2 and their graphical illustration is provided in Fig. 3 and Fig. 4.

TABLE 2

| Vdd | 1.0V | 2.0V | 3.0V | 4.0V | 5.0V |
|---|---|---|---|---|---|
| **Design** | | | **Power Dissipation (nW)** | | |
| 16T FA | 2.06 | 7.78 | 22.86 | 62.10 | 159.89 |
| 14T FA | 1.38 | 5.23 | 15.66 | 42.87 | 111.82 |
| Proposed | 0.66 | 1.83 | 3.83 | 7.20 | 12.81 |
| | | | **Delay (pS)** | | |
| 16T FA | 5.28 | 1.94 | 1.47 | 1.20 | 1.18 |
| 14T FA | 6.14 | 1.87 | 1.39 | 1.14 | 1.13 |
| Proposed | 16.76 | 4.20 | 3.07 | 2.48 | 2.10 |
| | | | **Power-Delay Product ($10^{-21}$)** | | |
| 16T FA | 10.87 | 15.09 | 33.60 | 74.52 | 187.62 |
| 14T FA | 8.47 | 9.78 | 21.76 | 48.87 | 126.35 |
| Proposed | 11.06 | 7.68 | 11.75 | 17.85 | 26.90 |

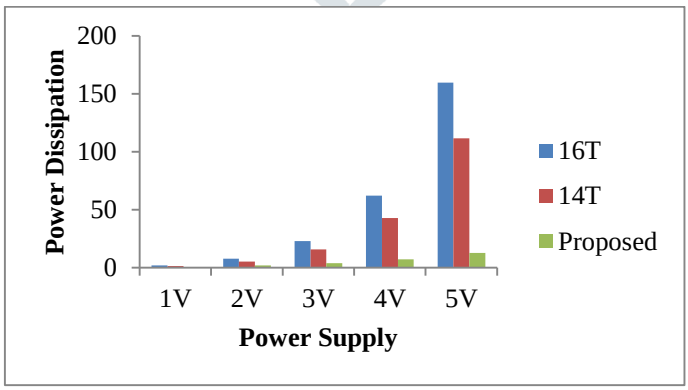


Fig. 3. Power Dissipation of proposed circuit at different supply voltage.

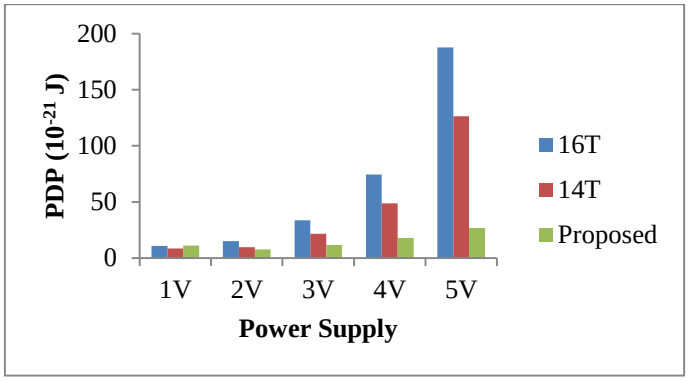


Fig. 4. Power Dissipation of proposed circuit at different supply voltage.

## 4. INFERENCES AND DISCUSSIONS

It is evident from the simulation results that the proposed circuits performs better as compared to previously reported work such as 14 and 16 transistors based full adder. It shows an improvement of 67% in power dissipation and 2% in PDP ( at 1.0V). Further an improvement of 91% and 85% improvement is observed in power dissipation and PDP (at 5V) respectively. As power dissipation and PDP is lessen as compare to other full adder therefore, it can further be utilized in designing higher order compressor.

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