TECHNIQUE TO REDUCE DYNAMIC POWER FOR FPGA

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Abstract

FPGA devices are programmable devices capable of implementing any digital logic circuit. They offer a designer the flexibility of creating a wide array of logic circuits at a low cost, because it is not necessary to manufacture a new custom made integrated circuit each time.

Keywords: VPR, VDDL, VDDH etc.

Introduction

The FPGA devices are bigger and consume more power than their ASIC counterparts [Kuan and Rose (2007)]. The main drawback of FPGAs is that they are less efficient than ASICs due to the added circuitry needed to make them reconfigurable. As a result FPGAs have been found to be a practical platform for medium and low volume applications only. The area overhead, combined with research and development costs, increases the per-unit cost of FPGAs, which makes them less suited for high-volume applications. Moreover, the speed and power overhead precludes the use of FPGAs for high-speed or low-power applications. In more than 20 years since the introduction of FPGA, research and development has produced dramatic improvements in FPGA speed and area efficiency, narrowing the gap between FPGAs and ASICs and making FPGAs the platform of choice for implementing digital circuits.

A significant number of studies include focus on faster and more area efficient programmable routing resources. Some important advancement has also been made in respect of CAD tools that are used to map applications onto the programmable fabric of FPGA. The Versatile Place and Route (VPR) tool described by Betz, Rose and Marquardt (1999), yields significant improvements in performance by improving on the existing clustering, placement, and routing algorithms. Logic-to-memory mapping tools, described by Cong and Xu (1998), Wilton (1998) and in International Technology Roadmap for Semiconductors (ITRS), shows improvement in the area efficiency of FPGAs with embedded memories wherein parts of the application are packed into unused memories before mapping the rest of the application into logic elements. In recent years, the main focus of the research has been shifting to lower the power consumption. Power consumption is an important part of equation determining the product size, weight and efficiency. Unfortunately, the advantages of FPGAs are offset in many cases by their high power consumption and area. The improved reliability, lower operating and cooling costs, and the ever-growing demand for low-power portable communications and computer systems, is motivating new low power techniques, especially for FPGAs, which dissipate significantly more power than fixed-logic implementations.

Indeed, the ITRS has identified low-power design techniques as a critical technology need.

2.3 TECHNIQUE TO REDUCE DYNAMIC POWER

Dynamic power reducing techniques are as follows

2.3.1 Dual Supply of Power

Decreasing the flexible voltage, or voltage scaling is the best method for dynamic force decrease since dynamic force is corresponding to the square of the graceful voltage. This strategy can essentially diminish dispersed force without corrupting pace, by specifically lowering the graceful voltage along non-basic postpone ways or light outstanding tasks at hand and higher flexibly voltage for substantial remaining tasks at hand The fundamental issue of designing double flexibly voltage in CMOS circuits is the expanded leakage current in the high voltage gates when a low voltage gate is driving them [39][40]. Where a low gracefully voltage (VDDL) inverter is driving a high flexibly voltage (VDDH) inverter. To beat the issue of expanded leakage current an extra level converter is required, which has region and force punishment.

2.3.2 Sizing of Transistors

The fundamental idea of transistor measuring is actually equivalent to that of gate estimating aside from that in gate measuring all the transistors in a single gate are estimated along with a similar factor yet in transistor measuring every transistor can be estimated autonomously, subsequently, transistor estimating [45]-[47] investigates the most extreme conceivable improvement space for power decrease absent a lot of execution corruption.

2.3.3 Sizing of Gate

Non-basic ways have timing slack and the postponements of certain gates on these ways can be expanded without influencing the presentation. Since the lengths of devices (transistors) in a gate are normally negligible for a fast application. the gate postponement can be expanded by diminishing the gadget width; thus, the dynamic force is in like manner diminished (this is because of littler stacking capacitance 'CL ', relative to the gadget size). Gate measuring is a method that decides gadget widths for gates [41] [44]. Customary gate measuring approaches use Elmore defers models in a polynomial definition. Heuristics based Greedy methodologies can be utilized to explain such polynomial.

CONCLUSION

As we have seen in this paper that FPGA devices are bigger and consume more power than their ASIC counterparts. In this paper we have also discuss the various types of techniques to reduce power.

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