Performance and estimation of Low Power1-bit Full Adder using Leakage Reduction Techniques

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Abstract: **This article proposes a full CMOS adder cell with techniques for leakage reduction. There are two techniques 1) MTCMOS (Multi-threshold CMOS)technique and 2) The technique for reducing leakage current is proposed for SVL (self controllable voltage level). The results based on MTCMOS and SVL techniques exhibit that ten transistors of leakage current based Full Adder of CMOS are minimized to huge region. For ten transistor-based CMOS Full Adder, Leakage power is also reduced similitude to conventional full Adder. This paper introduces MTCMOS and SVL technologies that reduce the variance of processes on CMOS Full Adder. It compares the key performance of MTCMOS techniques, and SVL techniques are applied on CMOS Full Adder is to exhibit leakage current & leakage power. CMOS Full Adder proposed design is simulated using Cadence tool at 90nm technology.**

Key Words: CMOS, CMOS Full Adder, Leakage Power, Leakage Current, Cadence.

1. INTRODUCTION

In many industrial applications, drive-driven batteries and portable devices need area and low-power potential devices [1, 2]. Gordon Moore discovers the law of Moore's in 1965. He was a co-founder of INTEL Corporation. He has speeded up our modern digital transition and has used power rise and cost reductions of the computer environment. He has forecasted that there will be four times more transistors in an interconnected system every two years. It's known as the Law of Moore. Nanometer range is nowadays used to construct a significant variety of industrial applications. Transistor size is limited by phenomena such as Effects of Short Channel, including tunnelling of oxide thickness and effect of hot transport. A main component of the CPU is an arithmetic logic unit (ALU). A significant unit of ALU is the adder cell. Numbers [3, 4] are added by numerous digital circuit adders. Adders for addresses [5], table markers, and related operations are found in many machines in other areas of the processor. The need for mobile devices (like mobile communications, tablets, laptops, [6, 7]) and requirements for VLSI circuits that provide surface and power efficiency have increased. In low power applications, low power adder cells are used. An enhanced full adder circuit of 1-bit requires a very small number of transistors and the least power present in this paper.

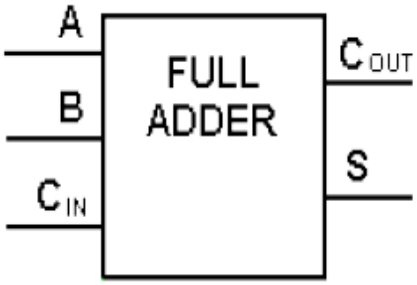

Figure1. Block Diagram of Full Adder of 1-bit

At present, there is an acute no of convenient exertion by a finite number of low-power requires low-power, available power, the circuitry of high throughput, and small area. Thus circuits that consume low power for designing device components and microprocessors become a major concern factor. Research has been accelerated in low power microelectronics, and VLSI systems of low power have appeared tremendously in demand. The most vital element of a CPU (central processing unit), Arithmetic logic unit (ALU), generation of address, and a floating-point unit inclusive of memory access unit or cache is Adder. The urge for power-efficient VLSI circuits and areas emerges from the increasing demand for mobile phones, including PDA (personal digital assistant), mobile phones, and PC Notebooks. In battery-based modules are used for high-speed and low power adder cells. Subsequently, it is critical and very useful in developing a full-adder of high-performance [8]. Figure 2 shows a consistent CMOS full Adder, with 28 transistors being one of the most common full-adders. We present a full-adder I-bit system with ten transistors for required power consumption and delay performance in this paper.

In contrast to less energy consumption, full adders [9], less energy consumption, and lower operating voltage, the simple benefit of 10 transistors are that of low area. Full voltage is getting more difficult and out of date to maintain it moving back backwards and forwards, with designs with a smaller number of transistors and less power consumption[10]. In the logic of pass, the transistor output voltage can be reversed and degraded because of threshold loss problem. This makes it desirable to increase the overall performance of the module[11]-[12]. The fundamental disadvantage of ten complete transistors is that the pass transistors have a threshold voltage drop. In all add output terminals, they have double threshold losses[13]. These

disadvantages were resolved in this paper by using the design technique of 10 transistors I-bit full-adder of Double gate FINFET.

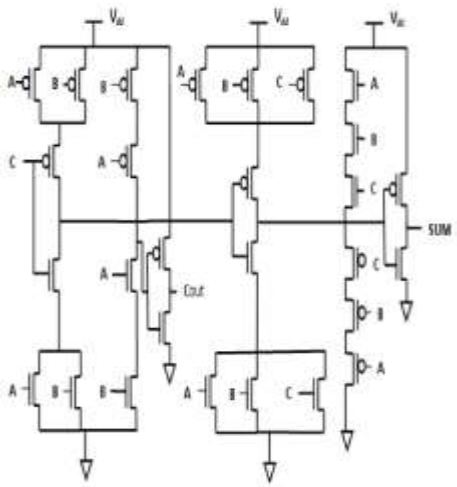

Figure 2. Schematic conventional Full Adder

The MTCMOS (Multi-threshold CMOS technology) offers efficient operation and low leakage by using logic cell transistors, high speed, low-vth, and high-vth sleep transistors, low-leakage. Logic cells from minimizing leakage or power supply in sleep mode are detached by High-vth equipment sleep transistors. This technology is a huge problem for the integrity of power plant and latency and also known as power gating. The figure shows the structure of the MTCMOS Power Gating technique. 2. The logic is applied by transistors with a low threshold voltage. The low voltage transistors are enveloped by using High voltage transistors during standby mode (sleep) from supply and the ground to prevent dissipation.

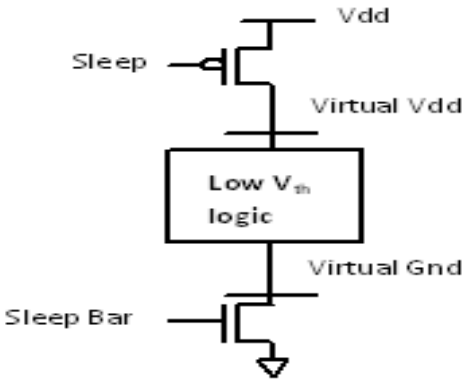

Fig.3. Power gating using MTCMOS technique

Connectivity time becomes a dominant factor in assessing the entire execution of integrated circuits. Since the duration of the retard is quadratic, to minimizing delay by widely used of repeater addition. In the repeaters, the interconnection delay can be suitably separated and sized. In general, the ideal repeater's size is greater than a minor repeater. As millions of repeated machines are inserted, considerable energy is consumed, particularly if the delay-optimal replications are used, to enable global interconnections. Various research used the additional appropriate time to conserve electricity in connections. Authors are presented with research methods to estimate ideal distance per unit length and size of a repeater.

The analysis of power should exactly take into a short circuit, consideration switching and leakage. While technologies are used to scale down the wires are put closely together, the coupling noise capacitive increases the interconnected lines. This will impact both delay and power use in interconnections. The authors have shown, as well to the switching power on the capacities of coupling that power consumption of the short circuit is canty enlarged, suggesting crosstalk noise. Consequently, the specification of optimal repeaters can also have this effect. This effect. Also, a major increase in leakage current has been caused by technology scaling. Leakage capacity exponentially expanded into a significant proportion of the overall energy usage of the chip. Authors researched the applicability of MTCMOS to repeat models to conserve leakage power besides not confer mathematical vindication to the appropriate number of the repetitions, sleep transistors, and the ingression duration. The effect of Crosstalk on power and delay for the optimum design has not been defined from above.

2. CMOS Full Adder Architecture

We present a full-adder CMOS circuit by the correct electricity usage, delay and duty cycles in this article; We have also compared the power dissipation, the hours wasted spread and other parameters on CMOS Full-adders cycle across ten different transistors. In contrast to more fully-added gateways, lower power usage, and lower operating voltage, 10 CMOS transistors' simple benefit is a small area as architectures are followed with lower power consumption and lower transistor counts, which is increasingly impossible along with further obsolescent to maintain maximum voltage running forward and backwards. On the one hand, the reduction of voltage swing is beneficial to the consumption of power. If the operation of cascade acting as moving Adder of ribbon, this can lead to slow switching. During low VDD, degraded performance can also cause circuit malfunctions [14]. Precise consideration also has to be given to solidity of the utilization of speed and power[15] to designs that use a decreased voltage swing. We required four XOR circuits or four XNOR transistors or two to multiplexers to implement separate ten transistor CMOS complete adder circuits. Fig. 5 displays the diagram for CMOS Full Adder, and Figure 6 shows the output waveform and the leakage waves of current is shown in Figure 7.

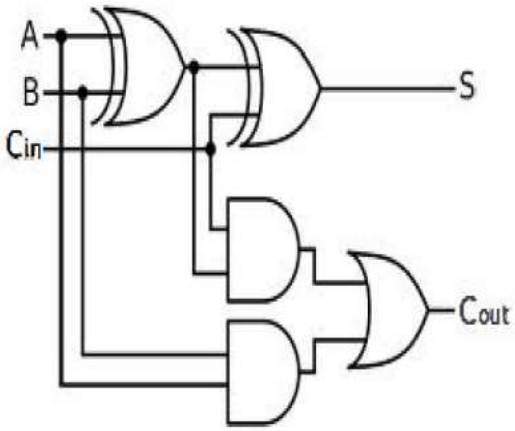

Figure.4 Gate Level Diagram of 1-bit Full Adder

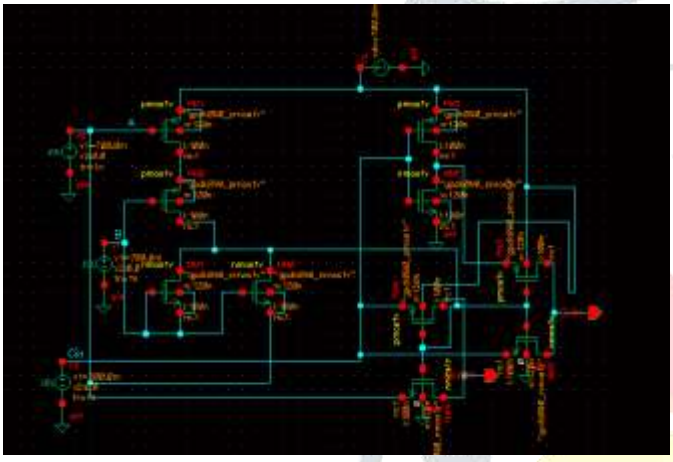

Figure.5 Schematic of CMOS Full Adder

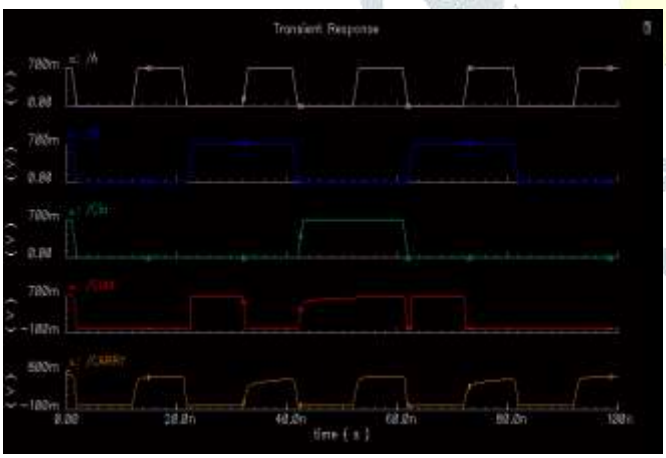

Fig.6 Transient Response of CMOS Full Adder

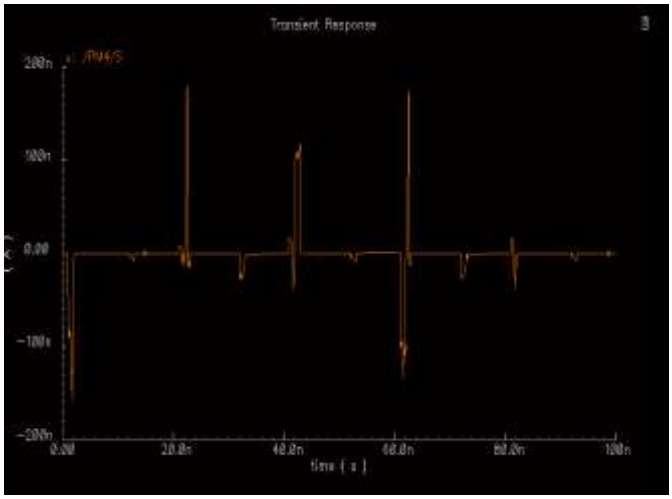

Fig.7 Leakage Current of CMOS Full Adder

A total of 10 transistors are employed in this topology to execute the following logical terms. Take a complete adder for CMOS. There are two input carriages, A and B, in this circuit, Cin. It produces the number

$$SUM = A \oplus B \oplus Cin \quad (1)$$

$$CARRY = AB + BCin + ACin \quad (2)$$

3. Full Adder of CMOS by using MTCMOS Technique

A technique MTCMOS of Full Adder 1-bit in the course of mid-PMOS Vth is attached to the terminal of Full Adder of Vdc 1-bit with a high NMOS Vth associated with the base terminal of Full Adder 1-bit. Fig 5 shows that the MTCMOS illustrative added to the complete Adder of 1-bit. A CMOS processor variation is MTCMOS which has multi-threshold voltage (Vth) transistors to optimize power or delays. The gate voltage is Vth MOSFET, which creates a layer of an inversion at the interface between the transistor's substrate (body) and the insulation layer (oxide). Small Vth machines switch rapidly thus are beneficial to reduce clock times on critical delay paths. The low Vth devices have a greatly improved capability of static leakage is the penalty. In the non-critical road, high-vth devices are used to reduce the static leakage power without a delayed penalty. MTCMOS technique is used in the output waveform of 1-bit Complete Adder output waveform shown by figure 8. The output waveform is shown by fig 9, and Figure 10 shows the leak current waveform. Standard devices of high-vth decrease steady noise by ten times in contrast with small Vth device.
Circuit of Digital CMOS may have three primary sources of dynamics, leakage dissipations and short power. In equation three shows that thus, a complete adder will calculate the total power consumed.

$$Ptot = P\,leak + Psc + Pdyn$$

$$= I\,leakVdd + ISCVdd + CLVddVfclk \quad (3)$$

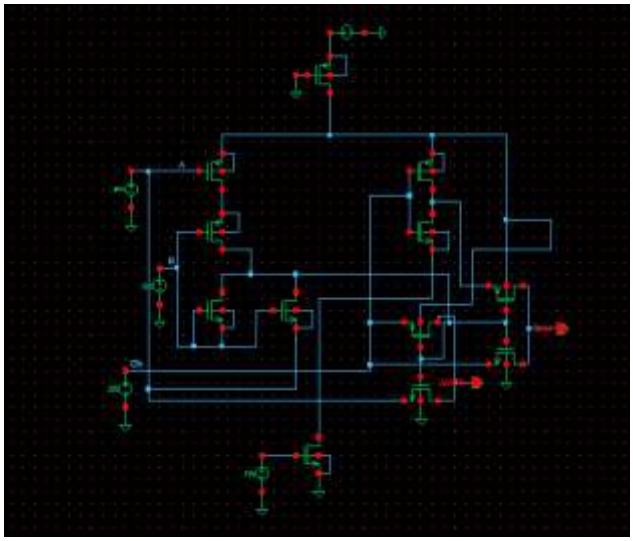

Figure.8 Schematic of CMOS Full Adder using MTCMOS

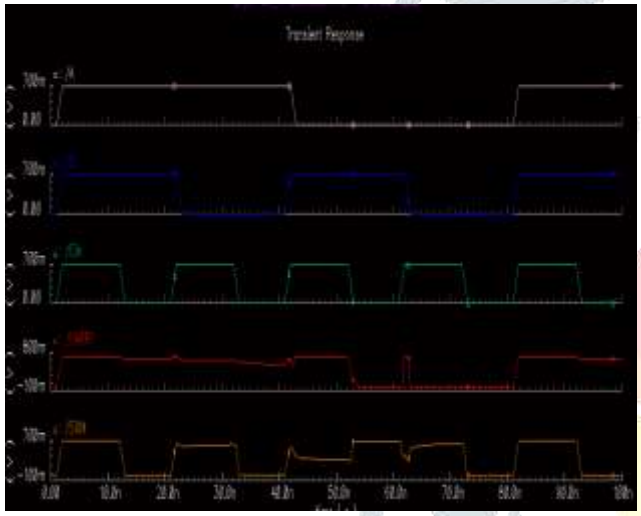

Fig.9 Transient Response of CMOS Full Adder using MTCMOS

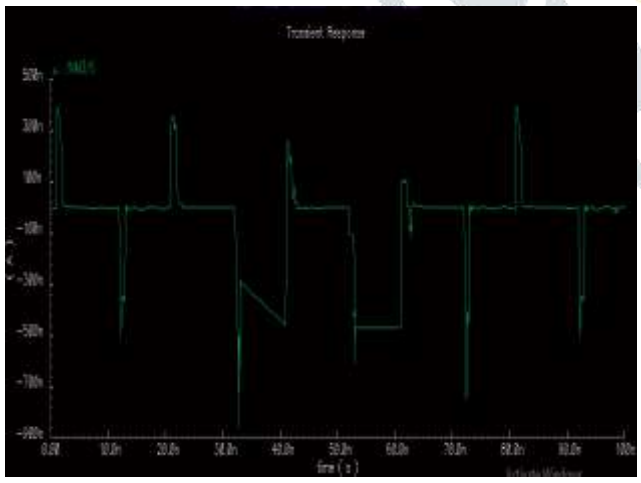

Fig.10 Using MTCMOS, Leakage Current of Full Adder CMOS

Therefore, the main task is to keep the CL Vdd V fClk minimum in low power design while preserving the required features. Pdyn is the first term, the next component the switching power component; is Pleak and PSc is the leakage of power. The loading capacitance is CL, and the time slot is fClk, that is the possibility of transition occurs from logic 0 to 1 (the same activity factor). The current ISC is imputable to the direct current shortening path that happens as all the transistors NMOS and PMOS are simultaneously activated, leading to the current directly from the source to field in the second term. In the second quarter, the current ISC has to be the voltage swing equal to the voltage swing within certain circuitry logic. The supply voltage is Vdd. Finally, leaking current leakage that may occur from injection polymers, and sub-thresholds is mainly determined by manufacturing processes' considerations.

4. CMOS Full Adder Using Technique of self controllable voltage level(SVL)

For CMOS complete adder, SVL is used by two approaches: 1) USVL (upper self controllable voltage level) to supply VDD voltage, 2) LSVL (lower self controllable voltage level) to supply NMOS and PMOS transistors with a load circuit of full Adder along with ground voltage power supply. Figure 11 showed the CMOS full adder transistor-level schematic with SVL technique. A parallel USVL circuit combines unique Switch of PMOSFET (p-SW) with multiple NMOSFET (n-RS) resistors in a parallel and series combination with single NMOSFET Switch (n-SW), and several series NMOSFET (p-RS) Resistors. In n-SW and p-SW, the active mode is "on," while p-RS and n-RS are "off". Therefore, the Active Load Circuit of the complete Adder has a minimum VS (=VSS = 0) of ground-level voltage and maximum VDD = VD supply voltage. For CMOS full adder it also increases the speed of operation. While n-RS and p-RS are 'up, in dormant mode, both n-SW and p-SW are 'off", decreasing the dc voltage's supply by the load circuit and increasing the supply of ground voltage for the load circuit. In this case, because of the implementation of both USVL and LSVL and Back gate bias (BGB) effect, the DIBL (drain induced barrier lowering) effect has also been decreased. Thus, the threshold voltage VTHN is raised, and the overall leakage current is reduced. Figure 12 exhibits the output waveform, and Figure 13 exhibits the current leak waveform.

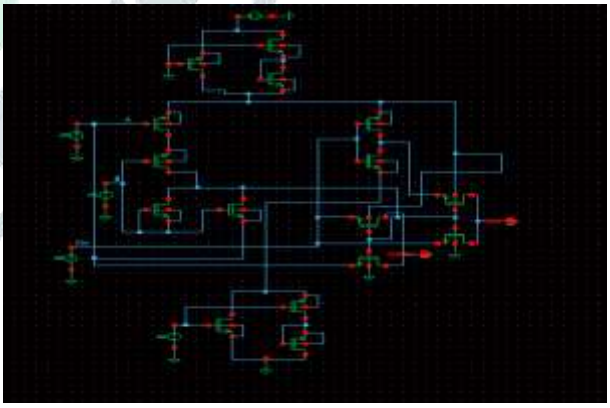

Fig.11 Schematic of CMOS Full Adder using SVL Technique

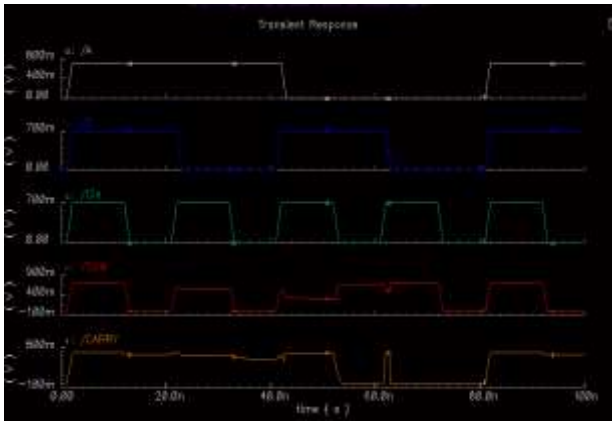

Fig.12 Transient Response of CMOS Full Adder using SVL Technique

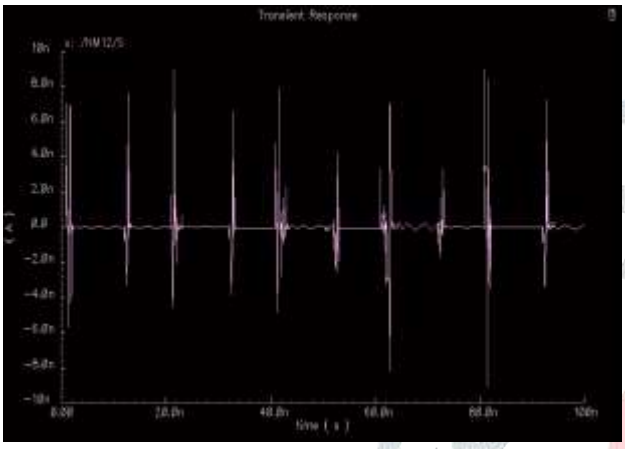

Figure.13 CMOS Full Adder's leakage current using SVL Technique

5. Simulation Result

On a Cadence Tool CMOS, Full Adder Simulation was performed using Nominal Supply Vdd = 0.7 V with the 90nm technology. Different techniques for reducing energy consumption and maintaining CMOS full adders' performance, CMOS full adders using MTCMOS technology and CMOS Full adder using the SVL technology were the only prevalent room temperature mechanism at 27°C. It compares Full Adder of CMOS using MTCMOS technique, Full Adder of CMOS using SVL technique & Full Adder of CMOS the parameter like Leakage Current, leakage power.

TABLE1 SHOWS COMPARISONS RESULT IN SUMMARY OF FULL ADDER OF CMOS WITH MTCMOS FULL ADDER AND FULL ADDER OF CMOS USING SVL TECHNIQUE.

TABLE 1 SUMMARY OF SIMULATED RESULT

Performance Parameter	Full Adder of CMOS	Full Adder of CMOS with MTCMOS	Full Adder of CMOS with SVL
Technology Used	90nm	90nm	90nm
Supply Voltage	0.7V	0.7V	0.7V
Leakage Power	10.4nW	9.2nW	3.02nW
Leakage Current	9.3nA	7.8nA	1.63nA
Transistor count	10	12	16

6. Conclusion

It was suggested that the CMOS Full Adder should be based on MTCMOS and CMOS Full Adder on SVL. The simulated results analysis ratify the viability of SVL and MTCMOS technologies in Full Adder of CMOS configuration and reveal that the leakage current and power dissipation variables are reduced by a voltage of 0.7V relative to CMOS Full Adder. Compared to the MTCMOS technique, the SVL technique with CMOS Full Adder has slightly expanded its area; in general, the lowest power dissipation and the lowest leakage current have been achieved. CADENCE VIRTUOSO Tool measures the result of the simulation. In this article, comparative overview of CMOS Full Adder SVL technique has been provided based on a minimum leakage power and leakage current at supply voltage Vdd = 0.7 V with input regulating the voltage of 0.7V and a threshold voltage. The simulation result is a better SVL technique for CMOS Full Adder than MTCMOS for CMOS Full Adder.

REFERENCES

[1] Sheenu Rana, Rajesh Mehra, "Optimized CMOS Design of Full Adder using 45nm Technology", International Journal of Computer Applications, Volume 142 – No.13, May 2016.

[2] Richa Saraswatal, ShyamAkashe and Shyam Babu," Designing and Simulation of Full Adder Cell using FinFET Technique" Proceedings of 7th Intl. Conf. on Intelligent Systems and Control (ISCO 2013).

[3] Shivani Sharma, Gaurav Soni, "Comparison analysis of FinFET based 1-bit full adder cell implemented using different logic styles at 10, 22 and 32nm", IEEE 2016.

[4] Noor Ain Kamsari, MuhhamedFaizBukheri, Zubaid Yusuf, "A Low Power Multiplexer based pass Transistor Logic Full Adder", 2015 IEEE Regional Symposium on Micro and NanoElectronics.

[5] Bhanu Priya, Randhir Singh and Shyam Babu, "Comparative analysis of Low Power 1-bit CMOS Full Adder Design at 45nm Technology", International Journal of Computer Applications, Volume 113 – No. 19, March 2015.

[6] Anuj Kumar Shrivastava, ShyamAkashe, "Design High Performance and 10T Full Adder using Double Gate MOSFET at 45nm Technology", 2013 International Conference on Control Computing Communication Materials (ICCCMU).

[7] Prasenjit Deb, Alak Majumder explains," Leakage reduction Methodology of 1-bit Full Adder in 180nm CMOS Technology", 3rd International Conference on Devices, Circuits and Systems ICDCS, IEEE 2016.

[8] Rabaey 1. M., A. Chandrakasan, B. Nikolic, Digital Integrated Circuits, A Design Perspective, 2nd 2002, Prentice-Hall, Englewood Cliffs, N1.

[9] Dan Wang, Maofeng Yang, Wu Cheng, Xuguang Guan, Zhangming Zhu, Yintang Yang, "Novel Low Power Full Adder Cells in 180nm CMOS Technology", 4th IEEE Conference on Industrial Electronics and Applications, ICIEA 2009, pp 430-433.

[10] Lu Junming; Shu Yan; Lin Zhenghui; Wang Ling," A Novel IO-transistor Low-power High-speed Full adder cell", Proceedings of 6th International Conference Solid-State and Integrated-Circuit Technology, vol-2, pp. 1155-1158,2001.

[11] Adarsh Kumar Agrawal, Shivshankar Mishra, and R K. Nagaria, "Proposing a Novel Low-Power High-Speed Mixed GDI Full Adder Topology", accepted in Proceeding of IEEE International Conference on Power, Control and Embedded System (ICPCES), 28 Nov.-DEC. 2010.

[12] N. M. Chore, and R N. Mandavgane, "A Survey of Low Power High Speed I Bit Full Adder", Proceeding of the 12th International Conference on Networking, VLSI and Signal Processing, pp. 302-307,2010.

[13] Shivshankar Mishra, V. Narendra, Dr RA. Mishra "On the Design of High-Performance CMOS I-Bit Full Adder Circuits," Proceedings published by International Journal of Computer Applications® (IJCA)2011.

[14] Jin-Fa-Lin, Yin Tsung Hwang, Ming-Hwa Sheu, and ChengCheHo, "A Novel High-Speed and Energy-Efficient 10Transistor Full Adder Design" IEEE Trans. Circuits Syst. I: Regular Papers, vo1.54, no.5, pp.1 050-1 059, May 2007

[15] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power IO-transistor full adders using XOR-XNORgates," IEEE Trans. Circuits Syst. II, Analog Digit SignalProcess., vol. 49, no. I, pp. 25-30, Jan. 2002.
[16] M. O. Simsir, A. N. Bhoj, and N. K. Jha, "Fault modelling for FinFET circuits," in Proc. Int. Symp. Nanoscale Archit., Jun. 2010, pp. 41-46.