# Hardware Implementation and performance evaluation of PLL in FPAA

**Dr. Ramesh Pawase, Bajirao Jawale,**
Assistant Professor, Dept. of E&TC, Amrutvahini College of Engineering, Sangamner, Savitribai Phule Pune University, India,
Post Graduate Student, Dept. of E&TC, Amrutvahini College of Engineering, Sangamner, Savitribai Phule Pune University, 422608,India

***Abstract:*** The Phase Locked Loops being the most important block of signal generation that is used in most of the radio and telecommunication systems. The stable and consistent signal generation with constant peak amplitude and frequency is expected feature of PLL that is achieved through FPAA experimentation. Configurable analog blocks are used for simulation subsequently hardware implementation is completed in this research project and performance evaluation of resources usage is done. It is found that 30% CABs are utilized only from FPAA1 whereas 43% CABs are utilized from FPAA2. The developed chip consumes power of 222.67 mW which is significantly minimum.

***Index Terms*** **- FPAA, PLL, Hardware Implementation.**

## I. INTRODUCTION

In recent times, Field programmable analog arrays (FPAA) are becoming extensive opportunity in ASP (analog signal processing) similar to Field Programmable Gate Array (FPGA) in digital domain. The software Anadigm delivered commercial FPAAs for extensive range of uses in signal processing, biomedical systems and dedicated real time products. All commercial companies are ready to decrease design cycle of any product to minimize the time to market and decreasing associated cost. This new trend of analog design not only save the time and cost but also provide wide scope for analog designers with limited resources. It requires mass scale production for ASIC fabrication of any analog circuit or system to achieve affordable cost; however, FPAA can provide single customized solution with minimum cost [1]. As FPAA has on board dynamic configuration capability, designers got user friendly platform in analog design with less time to market and less cost required for design cycle in integrated circuits. The major contributions of this paper are as follows:
Hardware implementation is completed in this research project and performance evaluation of resources usage is done.

## II. FPAA STRUCTURE:

FPAA has fully differential architecture which is suitable and advantageous for low voltage analog signal processing. AN231E04 being a breakthrough device consist of hardware module with user interface in software. In internal structure of FPAA, four Configurable Analog Block (CAB) blocks have programmable connections can be done and controlled using graphical user interface developed in Anadigm designer2 software and computer. It uses the Switched Capacitance (SC) technology at the backend in which electrical charge through capacitor is controlled.

The main advantages of using FPAA are as follows:

i. The analog design cycle time is condensed from years to few minutes.
ii. Differential configration provides better performance in context of dynamic environment.
iii. Dynamic reconfigration competence gives real time response during run time for changing excitations as well as system parameters.
iv. Simpler analog design and hardware implementation with affordable cost contrary to complex design, simulation, fabrication of ASIC that requires much of the cost for implementation.
v. Top down approach in analog design developes confident designers.

The implementation of analog circuits is simpler, easier and less time taking. Fig. 1 shows the internal basic structure of the FPAA model AN231E04 [13]. The biggest advantage of FPAA is dynamic reconfiguration ability which provides on board parameter changing facility reducing time for development. It has seven configurable input-output cells and two dedicated output for interfacing. The main features including, low input offset through chopper stabilized amplifiers leading to better performance.

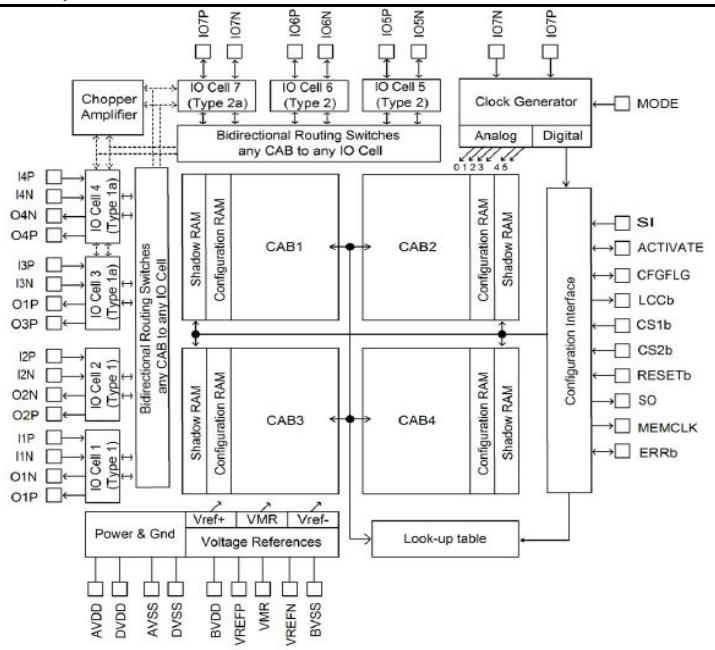


Fig. 1 Internal Block Diagram of FPAA [13]

The main four analog independent modules consisting of the look-up table, input and output interfaces having the analog functions creating facility. Look-Up Table (LUT) having 256 Byte capacities can be more suitable for sensor characteristics linearization and arbitrary signal generation. The typical frequency range for operation is from DC to 2MHz having Broadband Signal to Noise Ratio of 90dB and Narrowband (audio) S/N ratio of 120dB [13].

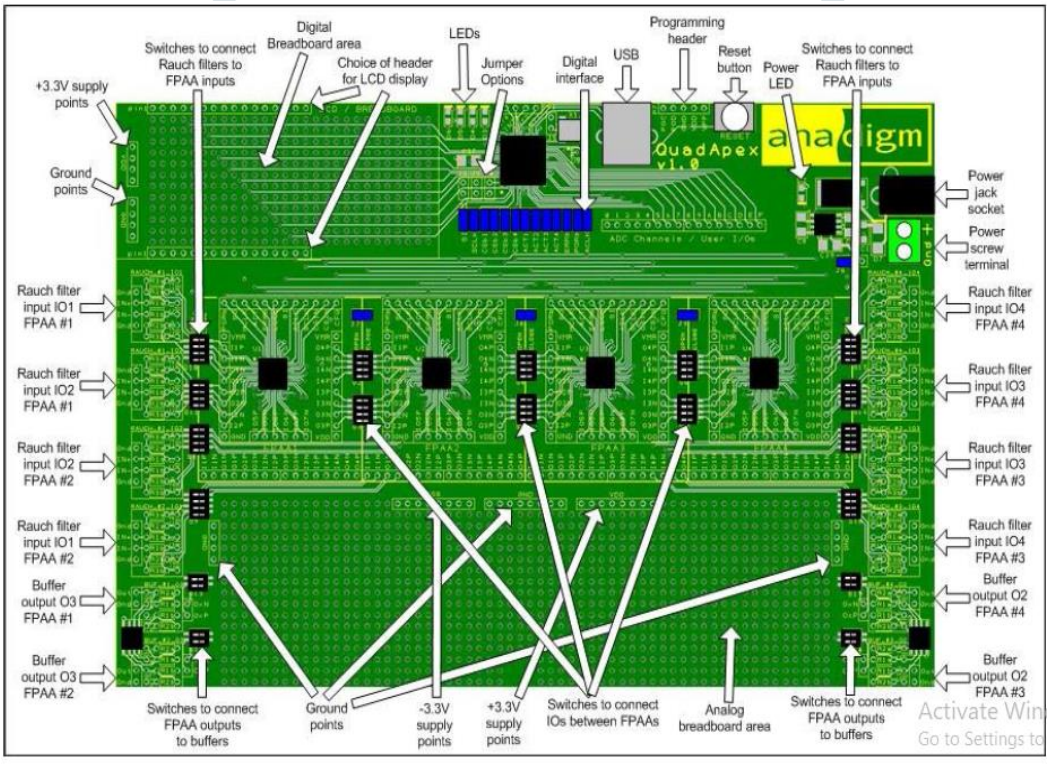


Fig. 2 Anadigm Quad Apex Development Board [13]

These features attracts analog designer for analog signal processing enabling quick updates in design and verification. The newer architecture consists of hardware capacity to develop 8 bit ADC for which digital output can be taken out serially through dedicated output pins. The FPAA (AN231E04) device is an "Analog Signal Processor"; that can be used for development of signal conditioning, amplification, different arithmetic functions like addition, subtraction, multiplication and some special functions like rectification, etc. The important features of FPAA are described in details as follow:[14]

**i.Dynamic Reconfiguration:** Most of the systems require instant updates and their corresponding response resulted in output to be recorded at the same time. This feature enables flexibility to make intelligent decisions for biomedical systems, control systems and real time monitoring systems. FPAA has dynamic reconfiguration facility which allows user to introduce changes in the system while it is working and reduces time of verification. It is one of the important features that attract analog designers to have flexibility in analog domain which is rarely found in analog signal processing.

ii. **Fully Differential Architecture:** All the inputs, outputs and processing blocks are accepting differential signals. The advantage of differential signal is comparatively more capable to avoid common mode interference.

iii. **I/O Configurable Cells:** It has seven configurable I/O cells and two dedicated output cells which have configuration facility either single ended of differential in nature. Another facility of I/O buffering with single ended to differential conversion is also available in FPAA.

iv. **Low Input Offset Through Chopper Stabilized Amplifiers:** Every input has got feature and option for connecting chopper stabilized amplifiers. Typical values of DC Offset via chopper stabilized architecture are <50µV.

v. **Look-Up Table:** It has got 256 Byte Look-Up Table (LUT) which can be used for arbitrary function generation in any experimental setup or linearization of sensor output by inverse modeling method. This method of linearization is not suitable for MEMS gyroscope and Seismic sensor as the output drift is completely random and temperature, process dependent. In this work, 256 byte LUT is used for storing response of Tanh-Sigmoidal activation function.

vi. **Inbuilt Band Gap References:** FPAA AN231E04 has internal band-gap reference generator is used to have temperature compensated reference voltage levels.

vii. **Bandwidth:** Typical signal bandwidth of DC to 2 MHz; however, in detail Bandwidth is CAM dependent as frequency range to be selected before using any CAM in Anadigm Designer Tool.

viii. **Signal to Noise Ratio (SNR):** It provides broadband SNR of 90dB and narrowband (audio) SNR of 120dB in applications.

ix. **Package Size:** It has industry standard 44 lead Quad Flat No-Lead (QFN) Package of size (7x7x0.9mm)..

x. **Supply Voltage:** It operates on supply voltage of 3.3V and hence power consumption is always optimum for design.

xi. **Switched Capacitor Technology:** FPAA operates on switch capacitor technology in which switches are used to perform sampling and high input impedance used for sensing stored quantities with no corruption. The operation is completed in sampling and amplification phases.

## III. SOFTWARE USED FOR FPAA:

### Anadigm Designer2 EDA:

AnadigmDesigner2 is Electronics Design Automation software; in which the designer can develop complex analog functions. The configurable analog modules (CAMs) are the building blocks for design. It has very easy-to-use drag-and-drop interface feature and the design process carried out in very less time that allows whole analog systems to be built quickly, and can be simulated in less time. Further, design is downloaded in to the AN231E04 FPAA chip for verification and testing. [14]

## IV. IMPLEMENTATION OF PHASE LOCKED LOOP:

The Phase Locked Loops being the most important block of signal generation that is used in most of the radio and telecommunication systems. The stable and consistent signal generation with constant peak amplitude and frequency is expected feature of PLL that is achieved through FPAA experimentation. **The** Configurable analog blocks uses Capacitors, Operational Amplifiers, Comparators, and Successive approximation resistors (SAR) for implementation of model.

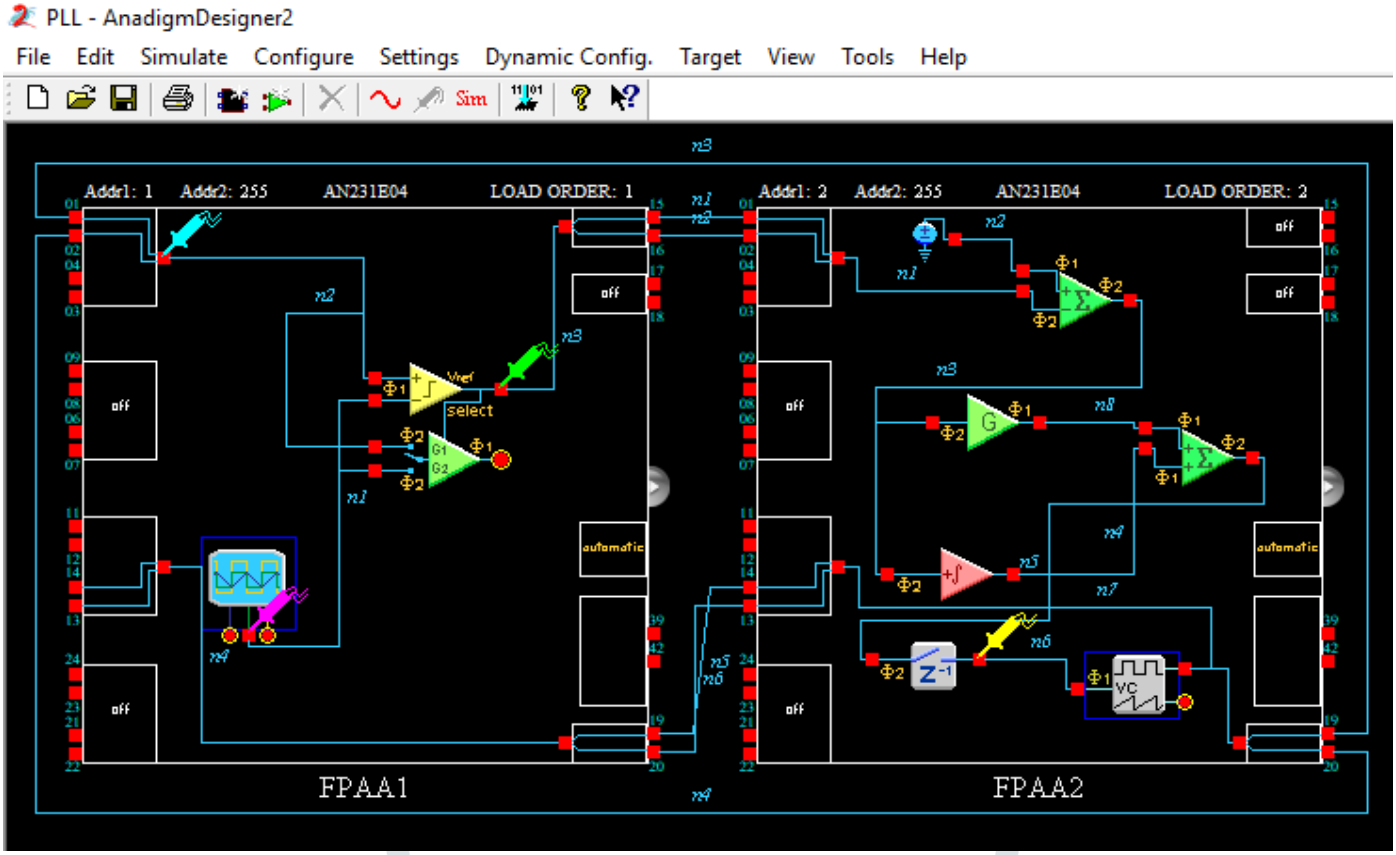


Fig. 3 Implementation of PLL in Anadigm Designer2

Fig. 3 shows implementation of PLL in Anadigm designer2 software with detailed blocks. The probes are attached at various intermediate points for testing the performance of PLL.


Fig.4. Output at various stages of PLL that is implemented in anadigm Designer2.

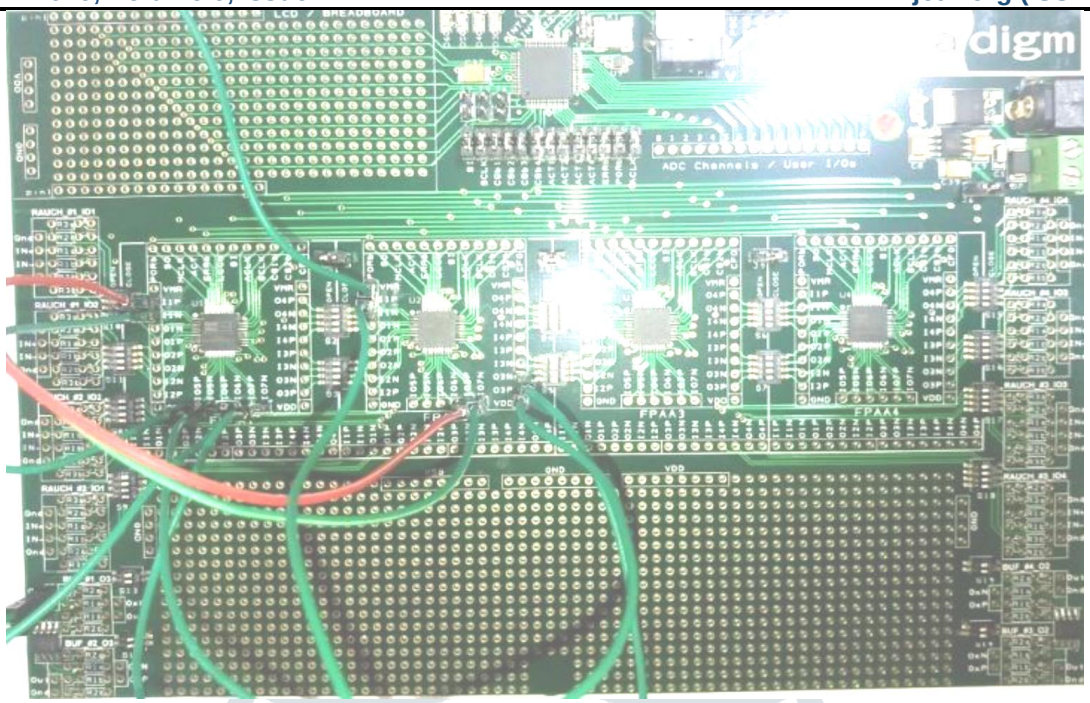


Fig.5. Hardware Implementation using FPAA

## V. RESULTS:

Table 1: Resources Utilization Summary in FPAA

| | FPAA1 | | | | FPAA2 | | | |
|---|---|---|---|---|---|---|---|---|
| **Resources** | **C** | **Op** | **Co** | **SAR** | **C** | **Op** | **Co** | **SAR** |
| CAB 1 | 03 | 01 | 01 | -- | 06 | 02 | -- | -- |
| CAB 2 | 08 | 02 | 01 | -- | 04 | 02 | -- | -- |
| CAB 3 | -- | -- | -- | -- | 08 | 02 | -- | -- |
| CAB 4 | -- | -- | -- | -- | 02 | 01 | 01 | -- |
| Total used | 11 | 03 | 02 | -- | 20 | 07 | 01 | -- |
| Available | 32 | 08 | 04 | 04 | 32 | 08 | 04 | 04 |
| Utilization in % | 37.5 | 50 | 25 | -- | 75 | 62.5 | 50 | -- |
| Power | 76.23 mW | | | | 146.44 mW | | | |

C: Capacitors, Op: No of Operational Amplifiers, Co: Comparators, SAR: Successive approximation resistors,

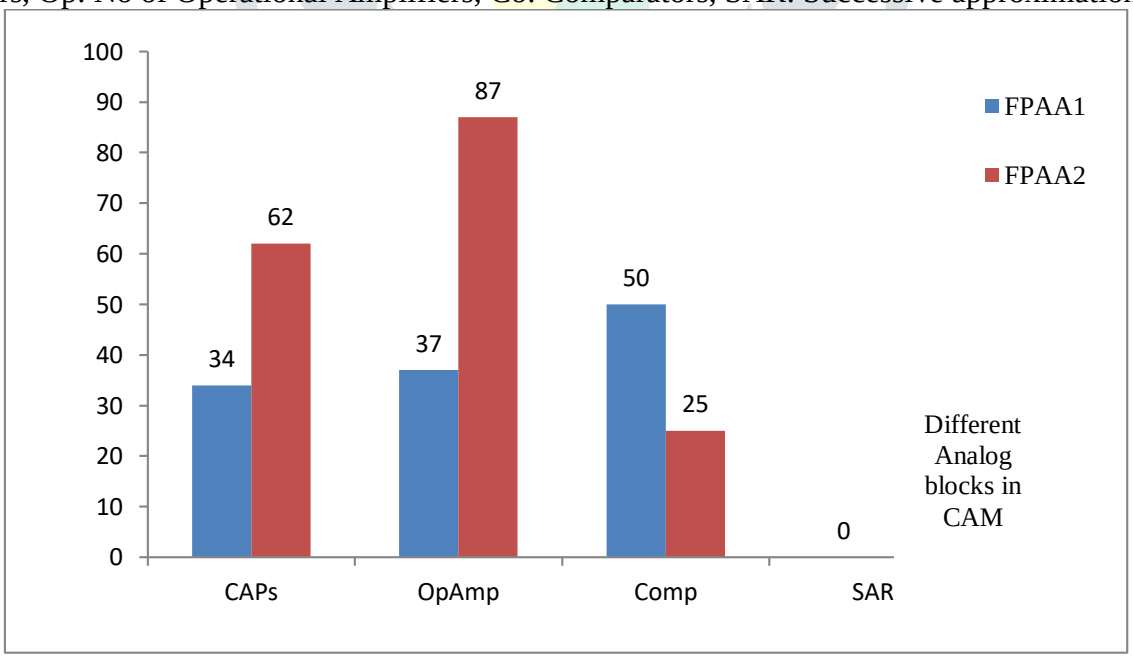


Fig 6. Comparison of FPAA Resource Utilization in Percentage

## VI. CONCLUSION:

This system presents field programmable analog array (FPAA) (Anadigm AN231E04) based hardware implementation of Phase Locked Loops (PLL). Configurable analog blocks are used for simulation subsequently hardware implementation is completed in this research project and performance evaluation of resources usage is done. It is found that 30% CABs are utilized only from FPAA1 whereas 43% CABs are utilized from FPAA2. The developed chip consumes power of 222.67

mW which is significantly minimum. The block wise resources utilization is optimum and very less. The proposed hardware chip uses all analog blocks reducing significant power and size of PLL circuit and enhancing processing speed.

## VII. ACKNOWLEDGMENT

The author would like to give credits of research project for VLSI Laboratory of Amrutvahini College of Engineering, Sangamner and hardware platform of Field Programmable Analog Array (FPAA).

## REFERENCES

[1] Ramesh Pawase, N. P. Futane, "MEMS Seismic Sensor with FPAA Based Interface Circuit For Frequency-drift Compensation Using ANN", March 2018, *International Journal on Smart Sensing and Intelligent Systems (S2IS)*, March 2018 Issue. DOI: 10.21307/ijssis-2018-001

[2] R. Pawase and N. P. Futane, "CMOS Gilbert Mutiplier for Analog Signal Processing and its FPAA Based Implementation," 2018 Int. Conf. Adv. Commun. Comput. Technol., pp. 623–626, 2018. Paper Presented and Published in IEEE Xplore DOI: 10.1109/ICACCT.2018.8529653

[3] A. S. Deese and C. O. Nwankpa, "Design and testing of custom FPAA hardware with improved scalability for emulation of smart grids," *IEEE Trans. Smart Grid*, 2014.

[4] A. Deese, J. C. Jiménez, and C. O. Nwankpa, "Utilization of field programmable analog arrays (FPAA) to emulate power system dynamics," in *Proceedings - IEEE International Symposium on Circuits and Systems*, 2009.

[5] A. Deese, J. C. Jiménez, J. Berardino, and C. O. Nwankpa, "Hardware prototype to emulate the dynamics of power system generators with field programmable analog arrays," in *ISCAS 2010 - 2010 IEEE International Symposium on Circuits and Systems: Nano-Bio Circuit Fabrics and Systems*, 2010.

[6] I. Pandiev, "FPAA Implementation of RMS-to-DC Converter for Analog Signal Processing," in *ICEST, Technical University of Sofia, Bulgaria*, 2011.

[7] R. Kiliç and F. Yildirim Dalkiran, "Programmable design and implementation of a chaotic system utilizing multiple nonlinear functions," *Turkish J. Electr. Eng. Comput. Sci.*, vol. 18, no. 4, pp. 647–655, 2010.

[8] C. Reiser, L. Znamirowski, O. A. Palusinski, S. B. K. Vrudhula, and D. Rakhmatov, "Dynamically Reconfigurable Analog / Digital Hardware - Implementation Using FPGA and FPAA Technologies," *Control*, no. May, 2014.

[9] S. K. Lakshmanan, "Towards Dynamically Reconfigurable Mixed-Signal Electronics For Embedded and Intelligent Sensor Systems," KLUEDO, 2008.

[10] A. K. Pilat, "Study on artificial neuron embedded into the dynamically programmable analogue signal processor," *IFAC-Papers OnLine*, vol. 28, no. 4, pp. 454–459, 2015.

[11] Anadigm Designer2 EDA: http://www.anadigm.com/sup_downloadcenter.asp?tab=ad2

[12] The AN231E04 dpASP Dynamically Reconfigurable Analog Signal Processor: http://www.anadigm.com/an231e04.asp

[13] "Anadigm FPAA, 'AN231E04 datasheet rev 1.1', available at: www.anadigm.com/_doc/DS231000-u001.pdf."

[14] Ramesh Pawase, "Development of CMOS ASIC to Compensate Non-idealities of MEMS-Based Gyroscope and Seismic Sensor" PhD Thesis, Savitribai Phule Pune University, Pune