SINGLE PHASE MULTILEVEL INVERTER WITH REDUCED COMPONENTS

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Abstract: Harmonic content is one of the most important aspects of these inverters. The amount of harmonics, introduced to the system, is lesser as compared with those of common inverters because of the staircase waveform of multilevel inverters. Total harmonic distortion (THD) is directly proportional to the no. of switches used to convert DC to AC and is inversely proportional to no. of levels. In this paper we propose a system in which we are using only 10 switches to generate 15 levels for getting less distorted and smooth waveform, thus reducing cost and complexity, also less switches leads to less switching time and improved system. After doing permutation and combinations on 3 DC voltages (6V, 12V and 24V), we are able to produce 15 output levels.

Keywords: Total harmonic distortion (THD), Multilevel Inverter (MLI), harmonics

I.INTRODUCTION

Staggered Inverters (MLIs) have been improved as important money saving advantage gadgets with a wide scope of utilizations. They have been in the concentration for quite a long time as a result of fascinating highlights, for example, top notch yield voltage, activity in high voltage/control, low weight on switches, and so forth. Staggered converters have a wide scope of uses, which has quickly built up the zone of intensity gadgets with great potential for further innovation. They can be utilized in photovoltaic frameworks, wind ranches, and HVDC frameworks. Staggered converters are diverse courses of action of semiconductor switches with dc connects to make n-level yield waveforms, which are isolated into three principle classifications:

- nonpartisan point clasped (NPC)
- flying capacitor (FC)
- Course H-connect (CHB).

In 1981, NPC was presented as the primary staggered converter that can be utilized in medium-voltage applications. Mid 1990s, FC was displayed and in 1996, CHB was reintroduced. Structure of MLIs relies upon the quantity of voltage levels, number of semiconductors, yield quality, number of dc supplies and dc connect capacitors, THD adequacy, most extreme voltage level, making positive and negative dimension, particularity, switch pressure, and absolute standing voltage (TSV). This paper plans to accomplish 15 voltage dimensions utilizing just 10 Switches. The inverter required 2^N-1 switches for N levels. Here we are utilizing 15 levels which will require 2^15-1=32768-1=32767 switches however in this task we utilize just 10 changes to accomplish 15 dimensions of AC supply. Sea vitality is one of the sustainable power sources. Sea warm vitality is the most inexhaustible in marine vitality, so it has a decent improvement prospect. At present, the fundamental method to utilize sea vitality is control age. In any case, it has hindrances: low productivity and high vitality utilization. In perspective on the above deficiencies, this investigation advances another kind of sea vitality thorough usage arrangement of water–power cogeneration.

II.LITERATURE SURVEY

Bharati S. Mathapati [1] in her paper "Stunned Inverter Based On Switched Dc Sources" illuminates the working rule of A Multilevel Inverter subject to DC traded sources. The proposed topology is looked into through proliferations and affirmed likely on a lab model.

Tekale Anil A. Also, et al [2] in their paper name as "Traded DC Sources Based Novel Multilevel Inverter", disseminated in International Research Journal of Engineering and Technology (IRJET) Volume: 04 Issue: 06 | June-2017 states that a Five-Level inverter are getting thought, exertion are being facilitated toward contracting the device mean extended number of yield levels. A story topology for Five-Level inverter has been proposed in this paper to decrease the contraption check. The working rule of the proposed topology has been appeared numerical plans fitting to yield voltage, source streams, voltage loads on switches, and influence disasters have been take out. Examinations of the proposed topology with existing topologies perceive that the proposed topology on a very basic level lessens the amount of force switches and related door driver circuits.

Durga Prasad G et al. [3] In their paper "Cross breed stunned DC interface inverter with lessened power electronic switches", analyzed A symmetrical MLI with diminished power semiconductor contraptions has been discussed in this paper where the required number of levels can be viably cultivated by

duplicating one source, dynamic and standoffish switch in LGM. The execution of the topology is trustworthy as it works only a solitary high repeat switch for each measurement age. The topology is emulated to watch the execution for R, and RL loads; and the results show that the rate THD diminishes to a sufficient standard. The proposed topology is inquired about probably for a comparative stacking condition and the test result affirms the proliferation results. The topology is striven for different control philosophies and reenactment results exhibit that IPD-SPWM control method is most suitable for the topology.

G.LourdsSajitha and C.R.Balamurugan [4] takes a gander at a work named as "A Novel Dc Link Coupled VL QZ Source Based Reduced Switch Multilevel Inverter". The proposed circuit has two blends of switches that are low and high repeat switches. The VL Quasi Z Source inverter is related amidst these two switches. To analyze this circuit two references with PDPWM approachs with triangular transporters are used for time of entryway movement for switches. The proposed circuit is worked in three modes specifically over modification, under guideline and common parity region. In the midst of these change areas the execution with respect to THD and Vrms are gotten. Shape the results its saw that the two references almost gives less THD and Vrms is higher because of third consonant imbuement reference. The results are worthy. Reenactment is performed through MATLAB/SIMULINK programming. Unmistakable amended reference philosophies with two references and triangular transporters have been made using MATLAB-SIMULINK and strove for different guideline records stretching out from 0.6 to 1.5 for new topologies of VL qZ source based amazed inverter. The proposed circuit may be used for variable speed drives. By changing the modification list in three unmistakable zone like over, normal and under change regions the proposed circuit perform better for third symphonious implantation reference the extent that THD and root infers square estimation of voltage. All most the two references gives less total symphonious reshaping for both reference yet the Vrms is more for THI reference. The results are adequate.

G Bhaskar Rao1 and et al [5] proposed A New Multilevel Inverter Topology Based on Switched Capacitor for Power Quality. Both 9-level and 13-level circuit topology are examined start to finish. Differentiated and customary fell amazed inverter, the proposed inverter can altogether reduce the amount of trading contraptions. A lone conveyor balance named by symmetrical PSM, was given the low trading repeat and fundamental utilization. The concurring delayed consequences of proliferation and examination further attest the attainability of proposed circuit and change method. For instance, the amount of voltage levels extends twice into equivalent amounts of cycle of 9-level circuit, and the amount of voltage levels assembles on various occasions down the center cycle of 13-level circuit. With the exponential addition in the amount of voltage levels, the sounds are basically cleaved down in staircase yield, which is particularly great in light of essential and versatile circuit topology and total consonant curving is diminished in 17 and 13-level inverter when appeared differently in relation to 9-level inverter the Meanwhile, the size control can be polished by heartbeat width course of voltage level, so the proposed stunned inverter can fill in as HF control source with controlled size and less music. This endeavor mainly explores nine-level ,13 and 17-level inverters. The strategy for examination and setup is furthermore appropriate to various people from the proposed inverter. The proposed inverter can be associated with lattice related photovoltaic structure and electrical arrangement of EV, in light of the way that the various dc sources are open viably from daylight based board, batteries, ultra capacitors, and vitality units.

E. Pavitra and M. S. Giridhar [6] proposed a novel topology for MLI in their paper "A Novel Multilevel Inverter Based on Switched DC Sources" to diminish the contraption check. The working standard of the proposed topology has been illuminated, and logical definitions contrasting with yield voltage, source streams, voltage loads on switches, and influence hardships have been delivered. Reenactment contemplates performed on a five-level inverter reliant on the proposed structure have been endorsed probably. Examination of the proposed topology with Conventional topology reveals that the proposed topology in a general sense decreases the amount of power switches and related passage driver circuits. Logical examinations dependent on adversities and switch cost demonstrate that the proposed topology is extraordinarily forceful. The proposed topology can be sufficiently used for applications where withdrawn dc sources are available. The upside of the reduction in the device count, in any case, powers two obstructions: 1) need of isolated dc sources simply like the case with the CHB topology and 2) diminished disengagement and accuse tolerant limits when stood out from the CHB topology.

Ambili R and Fareeda A Kareem [7] proposed an amazed inverter topology in their paper "A Novel Multilevel Inverter with Reduced Dc Sources" so as to secure all possible included substance and subtractive mixes of the information DC levels in the yield voltage waveform. It has less baffling control methodology, less related cost and lesser THD. The structure and standard of movement of the topology is low down. Modification of Phase Opposition Disposition (POD) technique sine beat width balance system for the proposed composed is furthermore illuminated. An examination of gave topology the customary and common topology shows that the device check is through and through diminished for a given number of levels in the yield. The proposed thought is presented by proliferations and affirmed likely for a single stage nine-level inverter.

NakulThombre and et al [8] proposes another topology for 21 levels with decreased number of switches and DC sources. Thusly, this new circuit will require lesser hardware space, lesser cost; moreover the multifaceted idea of the circuit will reduce.The FFT examination completed with the focal trading repeat achieved the THD of 12.69%. From the FFT examination, it is found that PDPWM strategy gives smallest THD. The new circuit is investigated in MATLAB/Simulink. It is seen that even after the decline in switches and sources, the perfect yield is gotten.

Subramanian Annamalai and JaisivaSelvaraj [9] in their paper "Novel Multilevel Inverter Topologies for Cascaded Voltage Source Architectures" proposed upside down topology MLI is having capacity of creating all the voltage levels with less voltage push and lessened conduction hardships on least conduction devices in any conduction method for each measurement than exchange topologies, similar to the cross breed MLI got from symmetrical MLI which is fitting for high impact applications with diminished standing voltages. From the above trade the extent that number of switches in conduction way, bypassing diode and total number of switches and diodes the proposed new amazed topology is having most insignificant starting cost than interchange topologies. The proposed topology has the dimension of chance on picking either PWM errand or fundamental trading mode depending upon the essential of variable speed and high voltage applications.

MithunKuriakose and Anooja [10] elucidates the working guideline of single stage five measurement traded DC sources inverter and single stage five measurement fell H-associate inverter in their work named as "Relationship of Performances of Switched DC Sources Inverter and Cascaded H-interface Inverter". Presentations of single stage five measurement traded DC sources inverter and single stage five measurement fell H-associate inverter are pondered dependent on number of switches used, voltage transversely over switches, capability, indicate consonant distortion(THD) of yield voltage waveform and multifaceted nature of gateway drive circuit. Single stage five measurement traded DC sources inverter and single stage five measurement fell H-interface inverter are reproduced using MATLAB/Simulink instrument. Displays of single stage five measurement traded DC sources inverter is differentiated and that of single stage five measurement fell H-interface inverter dependent on voltage across over switches, adequacy, mean consonant twisting (THD) of yield voltage waveform using MATLAB/Simulink mechanical assembly. Models of both single stage five measurement traded DC sources inverter and single stage five measurement fell H-associate inverter are made in the lab with two data DC voltage wellsprings of 12V each.

III.PROPOSED SYSTEM

Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low output of Electro Magnetic Interference (EMI). The term multilevel starts with the three-level inverter introduced by Nabae et al (1981). Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM).

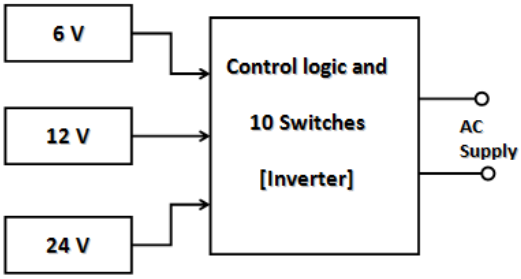

Fig 1 block diagram of proposed system

6V, 12V and 24V are separate DC sources used in this system. This are fed to the control logic and a series of switches which comprises the inverter. The output is 15 different levels of AC output. Inverter consists of

1. Switches: there are 10 switches present in this system. The MOSFET switches are used in this system since they can handle large power and are more accurate than any other type like IGBT or conventional transistor type (NPN or PNP).
2. Control logic: control logic is used to control the state of switch.

This output is then given to the oscilloscope as shown in fig 2 below.

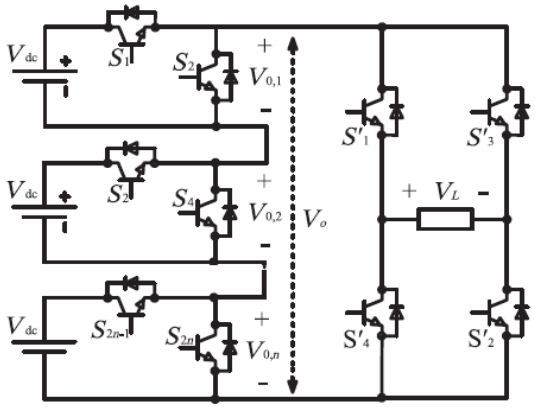

Fig 2 circuit diagram of proposed system

Fig .2 shows the circuit diagram of An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters with Reduced Components. The circuit diagram includes 10 Switches namely Mosfet1, Mosfet2 ... Mosfet10. The switches are made up of Mosfet (metal

oxide semiconductor field effect transistor), we are using this switches to convert input to 15 levels AC output. Letters DC represents DC power supply in proposed circuit diagram where DC=6Volt, DC1=12 Volt and DC2=24 Volt. The 10 subsystem represented as Dut1 are used to feed as logic to switch i.e. to control switch.

Control Circuit: We have used Arduino Uno for controlling purpose. The Arduino Uno is a microcontroller board based on the ATmega328. It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz ceramic resonator, a USB connection, a power jack, an ICSP header, and a reset button. It contains everything needed to support the microcontroller; simply connect it to a computer with a USB cable or power it with a AC-to-DC adapter or battery to get started. The Uno differs from all preceding boards in that it does not use the FTDI USB-to-serial driver chip. Instead, it features the Atmega16U2 (Atmega8U2 up to version R2) programmed as a USB-to-serial converter.

In the circuit diagram there are 10 switched. For switching purpose we have used MOSFET IRF540., who has Dynamic dV/dt Rating, Repetitive Avalanche Rated, 175 °C Operating Temperature, Fast Switching, Ease of Paralleling, Simple Drive Requirements, Compliant to RoHS Directive 2002/95/EC

After that circuit we have attached on Transformer:

Specifications:

- input voltage = 20V
- Output voltage = 230V
- Power = 1kW
- Winding ration = 2:23

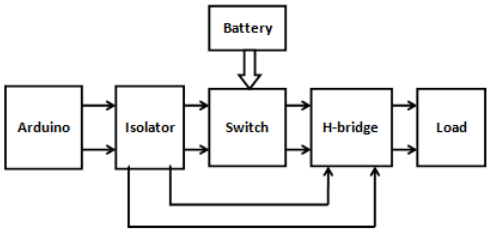

Fig 3 control circuit of proposed system

Gate Circuit

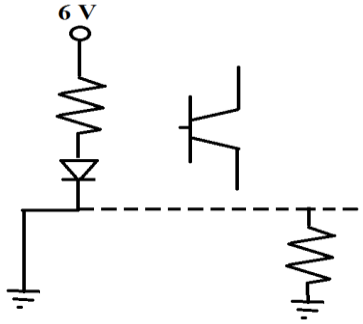

Fig 4 gate circuit

The dotted line is an opto-coupler who separates switches from load and source.

Switching Sequence

Table 4.1 switching sequence of proposed system

Volt	S1	B1	S2	B2	S3	B3
0	0	1	0	1	0	1
6	0	1	0	1	1	0
12	0	1	1	0	0	1
18	0	1	1	0	1	0
24	1	0	0	1	0	1
30	1	0	0	1	1	0
36	1	0	1	0	0	1
48	1	0	1	0	1	0

IV.SIMULATION MODEL

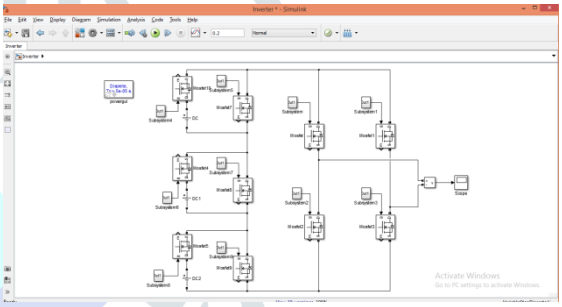

Fig 5 simulation diagram

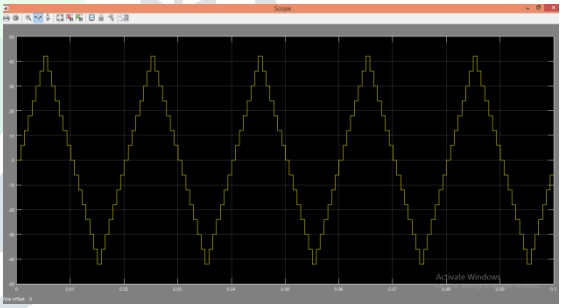

Fig 6 output waveforms

V.CONCLUSION

This paper presented a new MLI topology that can generate 15 levels with reduced components. It can be used in high-voltage high-power applications with unequal dc sources. It uses 3 unequal DC sources to generate 15 levels. It uses only 10 switches to obtain this many output levels hence reduces components. As this module can be easily modularized, it can be used in cascade arrangements to form high-voltage outputs with low stress on semiconductors and lowering the number of devices. Modular connection of these modules leads to achieve more voltage levels with different possible paths. It causes an improvement in the reliability of the modular inverter that enables it to use different paths in case of malfunction for a switch or a driver. The main advantage of proposed module is its ability to generate both positive and negative output

voltages without any H-bridge circuit at the output of the inverter. THDv% is 4% in experimental results that satisfy harmonics standard (IEEE519). The system is applicable in applications like Dynamic Voltage Restorer, Static VAR compensator,active power filters and high-power motor drives.

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