DESIGN OF A MULTI-MODE POWER-GATING ARCHITECTURE FOR STATIC POWER REDUCTION

[1]P.Meenakshi Vidya, [2]Dr.S.Sudha
[1]Associate Professor, [2]Professor,
[1]Department OF Electronics and Communication Engineering
[1]Easwari Engineering College, Chennai, India

Abstract :Multithreshold CMOS is very effective for reducing standby leakage power during long periods of inactivity. Recently a power-gating scheme was presented to support multiple power off modes and reduce the leakage power during short periods of inactivity. However, this scheme can suffer from high sensitivity to process variations, which impedes manufacturability. We propose a new power-gating technique that is tolerant to process variations and scalable to more than two intermediate power-off modes. The proposed design requires less design effort and offers greater power reduction and smaller area cost than the previous method. In addition, it can be combined with existing techniques to offer further static power reduction benefits. Analysis and extensive simulation results demonstrate the effectiveness of the proposed design.

IndexTerms **- Leakage power, multi-mode power switches, power consumption reduction, process variation, reconfigurable power-gating structure**

I. INTRODUCTION

As Chip density increases relentlessly along Moore's law power consumption is emerging as a major burden for contemporary systems [1]. Dynamic power is tackled nowadays by the reduction of the supply voltage level. Dynamic energy is proportional to the square of the supply voltage. Thus, a lower voltage level yields a quadratic reduction in the energy consumption. To further reduce the dynamic power systems-on-chip (SoCs) are partitioned into voltage islands with separate supply rail and unique power characteristics [2]–[4]. Separate power management policies (such as dynamic supply voltage scaling) can be applied in each region thereby further reducing dynamic power.The reduction of the power supply voltage level adversely affects the execution time. In order to maintain system performance, the transistor threshold voltage (Vt) is reduced. The reduction of the threshold voltage however adversely affects.

Many techniques have been presented in the literature for reducing static power. One common approach is to synthesize the circuit using dual V_t libraries [6]. High-Vt cells reduce the leakage current at the expense of reduced performance; thus their use on noncritical circuit domains reduces the leakage power considerably without affecting circuit performance. Another technique exploits the fact that the leakage power consumed by each gate strongly depends on the input vector applied at the gate. Therefore, in order to reduce static power, it controls the input vector and the internal state of the circuit during periods of inactivity [7]–[11].

II. MULTI-MODE POWER-GATING ARCHITECTURE

A. Proposed Architecture

The proposed design consists of the main power switch transistor M_P and two small transistors M_0 and M_1, each corresponding to an intermediate power-off mode (M_0 corresponds to the dream mode and M_1 corresponds to the sleep mode). Transistor M_P is a high-Vt transistor and it remains on only during the active mode

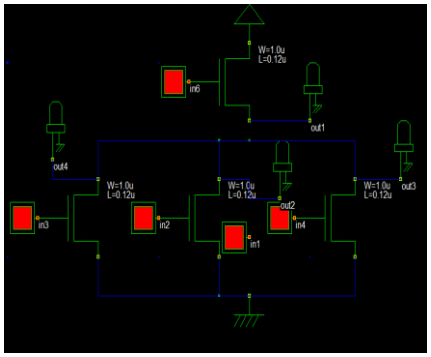


Figure 2.1 Proposed design architecture

. Transistors M_0 and M_1 are small low-Vt transistors that are turned on only during the corresponding power-off mode. (i.e., M_0 is turned on during the dream mode and M_1 is turned on during the sleep mode). The various modes of operation are as follows.

1) **Active Mode:** Transistors M_P, M_0, M_1 are on.

2) **Snore Mode:** Transistors M_P, M_0 and M_1 are off as shown in Fig. 2(a). In this case, the leakage current of the core, ILcore, is equal to the aggregate leakage current flowing through transistors M_0, M_1, M_P (ILcore = IL_{M0} + IL_{M1} + IL_{MP}), which is very small (note that M_0, M_1 are small transistors and M_P is a high Vt transistor). Thus the voltage level at V_GND is close to $V_{dd}$and the circuit consumes a negligible amount of energy, but the wake-up time is high.

3) **Dream Mode:** Transistor M_0 is on and transistors M_P and M_1 are off as shown in Fig. 2(b). In this case, the current flowing through transistor M_0 (and thus the aggregate current flowing through M_0, M_1,and M_P) increases because M0 is on (I_{M0}> IL_{M0}). The exact value of I_{M0} depends on the size of transistor M_0,and it sets the virtual ground node at a voltage level which is lower than Vdd (i.e., V_{V_GND} <V_{dd}). Thus the static power consumed by the core is higher compared to the snore mode, but the wake-up time is less.

4) **Sleep Mode**: Transistor M_1 is on, and M_P, M_0 are off as shown in Fig. 2(c). Provided that transistor M_1 has larger aspect ratio than M_0 (W_{M1}/L_{M1}> W_{M0}/L_{M0}), the aggregate current flowing through M_0, M_1,and M_P increases even more when M1 is on (note that I_{M1}> I_{M0}). Consequently, the voltage level at the virtual ground node is further reduced compared to the dream mode and thus the wake-up time decreases at the expense of increased power consumption.

B. Design Method

The correct operation of the proposed design depends on the correct sizing of transistors M_0 and M_1. For simplicity, as in [42], we model the core with a single equivalent nMOS transistor, and we consider only the subthreshold leakage current (we note that this structure is used only for the mathematical analysis in this section). Considering the very low transistor threshold voltage levels (V_{THC}) in nanometer technologies and the intermediate voltage levels at the virtual ground during the various intermediate power-off modes (excluding the complete power-off mode), the corresponding power-off transistors M_0 and M_1 are in the linear region of operation when they are active (V_{gs} = V_{dd}). This is because V_{ds} = V_{V_GND} <V_{gs} − V_{THC} = V_{dd} − V_{THC},whereVgs and Vds are the gate-source and drain–source voltages, respectively, for M_0 and M_1 [44].

Let us consider the dream mode shown in Fig. 2(b). In this mode, transistor M_0 is on. Let $V^0_{V\_GND}$ be the voltage at the virtual ground node at this mode. As stated above,$V^0_{V\_GND}$<V_{dd} − V_{THC} (V_{THC} is the threshold voltage of the low-Vt transistors M_0, M_1) and taking into account that V_{gs} −V_{THC}> 0 we can deduce that M_0 operates in the linear region when it is on. Therefore, the current flowing through M0 is given by the following equation:

$$I_{M0} = \mu_n C_{ox} \frac{W_{MO}}{L_{MO}} \left((V_{dd} - V_{THC}) V^0_{V\_GND} - \frac{(V^0_{V\_GND})^2}{2} \right) \quad (1)$$

Where W_{M0} , L_{M0} are the width and length, respectively, of M_0.

The nMOS transistor representing the core is in the sub threshold region of operation, since I to its source): V_{gs} − V_{THC} = 0 − V_{THC}< 0. The subthreshold leakage current is equal to

$$IL = I_0 e^{\frac{V_{GS} - V_{th0} - \eta V_{DS} + \gamma V_{BS}}{n V_T}} \left[1 - e^{\frac{-V_{DS}}{V_T}} \right] \quad (2)$$

where I_0 is a constant, which depends on the width and length of the transistor. V_{th0} is the zero-bias threshold voltage, VT is the thermal voltage, and n is the subthreshold swing coefficient. η is the DIBL coefficient and γ is the linearized body effect coefficient.

In our case, for the diode-connected transistor that represents the core (in Fig. 2), V_{GS} = 0, V_{DS} = V_{dd} − $V^0_{V\_GND}$, V_{BS} = 0, and the subthreshold leakage current of the core is calculated as

$$ILcore = I_0^{core} e^{\frac{-V_{THC} - \eta(V_{dd} - V^0_{V\_GND})}{\eta V_T}} \left[1 - e^{\frac{V^0_{V\_GND} - V_{dd}}{V_T}} \right] \quad (3)$$

The leakage current of power switch M_P and transistor M_1 can be calculated in the same way. Based on Kirchhoff's current law, we can obtain I Lcore = I_{M0} + I L_{M1} + I L_{MP} . Note that W_{M1} /L_{M1}<< W_{MP} /L_{MP} ; thus I L_{M1}<< I L_{MP} . Therefore, the equation above is simplified to

$$IL_{core} = I_{M0} + IL_{MP} \quad (4)$$

Substituting (1)–(3) into (4), we get the size of M_0 as

$$\frac{W_{M_0}}{L_{M_0}} = \frac{2(IL_{core} - IL_{M_P})}{\mu_n C_{ox} (2(V_{dd} - V_{THC}) V^0_{V\_GND} - (V^0_{V\_GND})^2)} \quad (5)$$

By using (5) we can adjust the voltage level $V^0_{V\_GND}$ to any value in the range (0, V_{dd}− V_{THC}) and calculate the aspect ratio of transistor M_0. The wake-up time is calculated by the equation Twake−up = Ctotal · Req, where Ctotal is the parasitic capacitance of the virtual ground and Req is the equivalent resistance of transistor M_P when it discharges the virtual ground node. Note that Req is the average resistance of M_P for the conducting time duration [44, pp. 104–105]. Thus, the wake-up time is provided by the following equation:

$$T_{wake-up} = C_{total} \cdot \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} \frac{V^0_{V\_GND}(t)}{I_{D(t)}}\, dt \qquad (6)$$

or equivalently

$$T_{wake\_up} = C_{total} \times \frac{1}{-V^0_{V\_GND}} \int_{V^0_{V\_GND}}^{0} \frac{V}{I_D(V)}\, dV \qquad (7)$$

Since MP is in the linear region during the wake-up operation (VGS = Vdd), (7) is written as follows:

$$T_{wake-up} = C_{total} \times$$

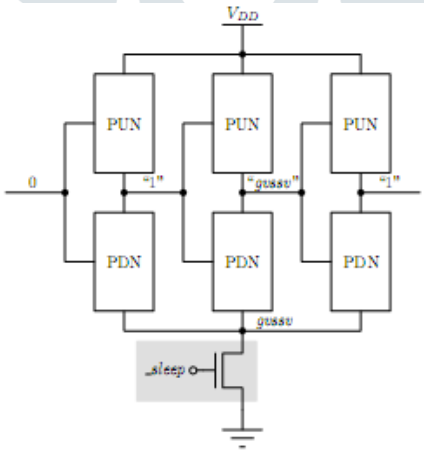
$$\frac{-2L_{M_P}}{\mu_n C_{ox}\, W_{M_P} V^0_{V\_GND}} \times \int_{V^O_{V\_GND}}^{O} \frac{1}{2(V_{dd} - V_{THC}) - V}\, dV \qquad (8)$$

The same analysis can be used for calculating the size and the related wake-up time for transistor M1 (in that case, the voltage at virtual ground node is equal to $V^1_{V\_GND}$).

Equation (5) can be used for calculating the transistor size required to set the virtual ground rail at any particular voltage level in the range (0, Vdd − VTHC). Thus the extension of the design to more power-off modes is straightforward. Note that in the above analysis, we considered only the subthreshold leakage current for every device that is turned-off. For a more accurate estimation, however, the total leakage current of the core and the power switch MP must be used in (5). During the transition from any power-off mode to the active mode, spurious glitches may occur in the internal circuit nodes that are not captured by the above simplified mathematical model. As a consequence, a detailed ramp-up analysis is needed for every circuit and every intermediate power-off mode.

III. POWER GATING TECHNIQUES

Power gating is the single most important tool circuit designers have to combat leakage. These techniques essentially increase the effective resistance of leakage paths by adding sleep transistors between logic stacks and power supply rails. Power gating also enjoys many of the properties from transistor stacking. Oftentimes, these power gating or sleep transistors are shared among multiple logic stacks to reduce the number of leakage paths as well as area overheads. Sharing the transistors effectively creates two new power nets: Gated-Vdd (gvddv) and Gated-Ground (gvssv), which replace VDD and GND for power-gated logic stacks. gvddv is connected to VDD using a head sleep transistor and gvssv is connected to GND using a foot sleep transistor.



. Figure 4.1: Cut-Off (CO) power gating using a foot sleep transistor, which is shared by several logic blocks

The output nodes tend to drift to gvssv, which itself drifts towards VDDdimensionally. If you must use mixed units, clearly state the units for each quantity in an equation.

The SI unit for magnetic field strength *H* is A/m. However, if you wish to use units of T, either refer to magnetic flux density *B* or magnetic field strength symbolized as $\mu_0 H$. Use the center dot to separate compound units, e.g., "A·m^2."

IV. RESULTS AND DISCUSSION

The target of system first, to evaluate the proposed method when it is applied to large logic cores that are comparable in size to real designs from industry. To this end, we present simulation results on a large logic core consisting of 9 million transistors. This core consists of multiple inverters of various sizes which are driven by various input vectors. Even though it is not a real circuit, it is representative of a realistic industrial circuit in terms of static power consumption during dc operation in power-off mode. We used the45-nm predictive technology with 1.1-V power supply. The leakage power consumption of the core in idle mode with no power gating is equal to 10 mW. All simulations were done using the HSpice simulation engine.

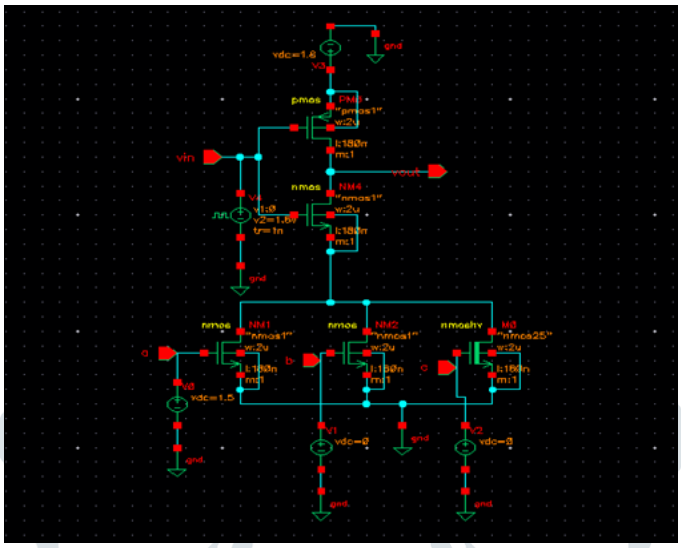


Figure 3.1 Proposed Multimode power gating Technique

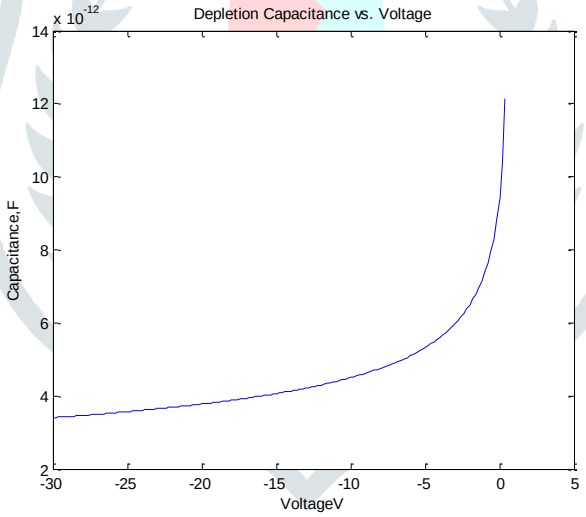


Figure 3.2 Depletion Capacitance Vs Voltage

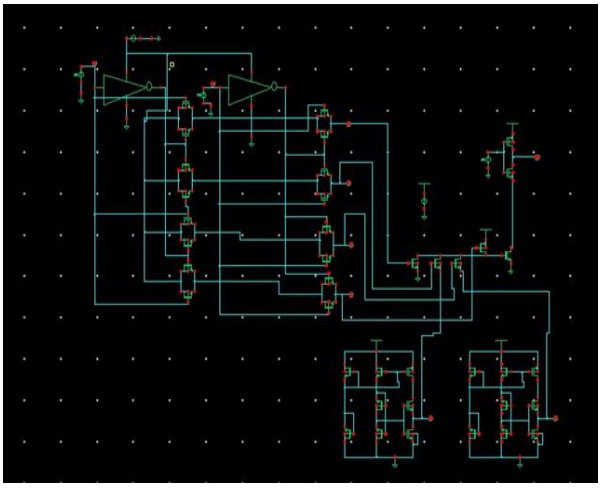


Figure 3.3Static power reduction technique model

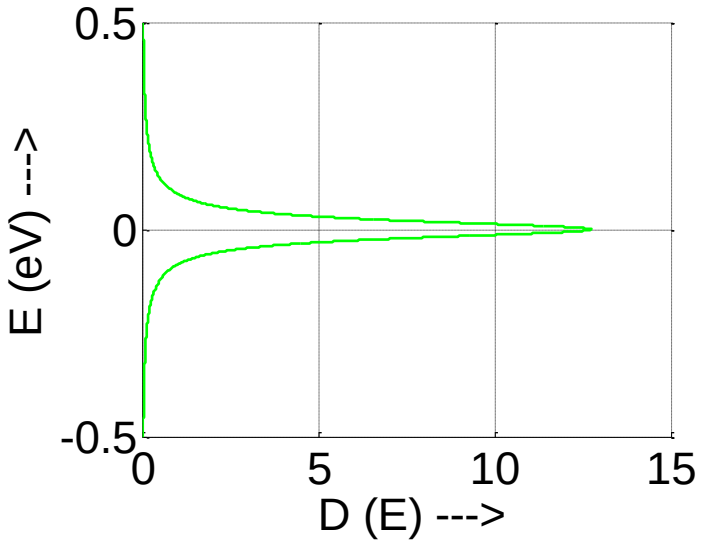


Figure 3.4 Carrier Concentration Vs Energy

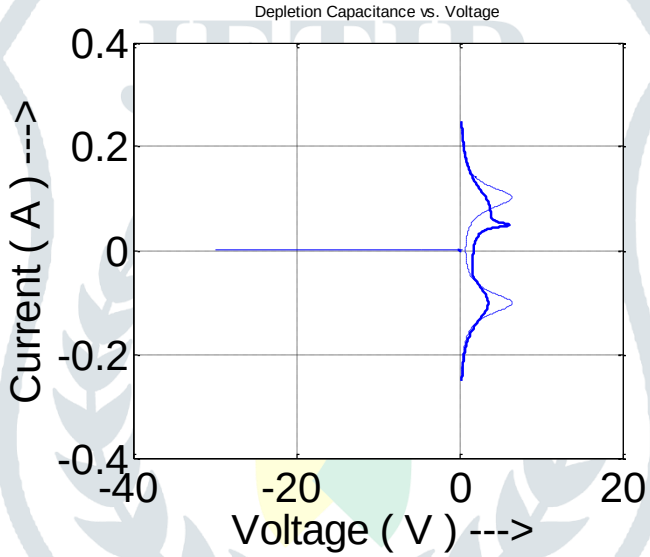


Figure 3.5 Quantum Transport

V. CONCLUSION

A new power-gating scheme that provides multiple power-off modes was discussed. The proposed design offered the advantage of simplicity and required minimum design effort. Extensive simulation results showed that, in contrast to a recent power-gating method, the proposed design is robust to process variations and it is scalable to more than two power-off modes. Moreover, it requires significantly less area and consumes much less power than the previous design. Finally, a reconfigurable version of this method can be used to increase the manufacturability and robustness of the proposed design in technologies with larger process variations.

References

[1] Semiconductor Industry Association. (2007) [Online]. Available:http://www.itrs.net/Links/2007ITRS/Home2007.htm
[2] D. Lackey, P. Zuchowski, T. Bednar, D. Stout, S. Gould, and J. Cohn,"Managing power and performance for system-on-chip designs usingvoltage islands," in Proc. IEEE/ACM Int. Conf. Comput. Aided Design,Nov. 2002, pp. 195–202.
[3] R. Puri, D. Kung, and L. Stok, "Minimizing power with flexible voltageislands," in Proc. IEEE Int. Symp. Circuits Syst., May 2005, pp. 21–24.
[4] R. Puri, L. Stok, J. Cohn, D. Kung, D. Pan, D. Sylvester, A. Srivastava,and S. Kulkarni, "Pushing ASIC performance in a power envelope," inProc. Design Autom. Conf., Jun. 2003, pp. 788–793.
[5] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leak-age current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327,Feb. 2003.
[6] S. Idgunji, "Case study of a low power MTCMOS based ARM926 SoC:Design, analysis and test challenges," in Proc. IEEE Int. Test Conf.,Oct. 2007, pp. 1–10.
[7] A. Abdollahi, F. Fallah, and M. Pedram, "Leakage current reduction inCMOS VLSI circuits by input vector control," IEEE Trans. Very LargeScaleIntegr. (VLSI) Syst. vol. 12, no. 2, pp. 140–154, Feb. 2004.
[8] Y. Alkabani, T. Massey, F. Koushanfar, and M. Potkonjak, "Input vectorcontrol for post-silicon leakage current minimization in the presenceof manufacturing variability," in Proc. 45th ACM/IEEE Design Autom.Conf., Jun. 2008, pp. 606–609.
[9] K. Kim, Y.-B. Kim, M. Choi, and N. Park, "Leakage minimizationtechnique for nanoscale CMOS VLSI," IEEE Des. Test Comput., vol. 24,no. 4, pp. 322–330, Jul. 2007.
[10] S. Mukhopadhyay, C. Neau, R. Cakici, A. Agarwal, C. Kim, and K. Roy,"Gate leakage reduction for scaled devices using transistor stacking,"IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 11, no. 4,pp. 716–730, Aug. 2003.
[11] H. Suzuki, W. Jeong, and K. Roy, "Low-power carry-select adder usingadaptive supply voltage based on input vector patterns," in Proc. Int.Symp. Low Power Electron. Design Conf., Aug. 2004, pp. 313–318.
[12] M. Anis, S. Areibi, and M. Elmasry, "Design and optimization ofmultithreshold CMOS (MTCMOS) circuits," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 22, no. 10, pp. 1324–1342,Oct. 2003.
[13] M. Anis, S. Areibi, M. Mahmoud, and M. Elmasry, "Dynamic andleakage power reduction in MTCMOS circuits using an automatedefficient gate clustering technique," in Proc. 39th Design Autom. Conf.,Jun. 2002, pp. 480–485.
[14] M. Anis and M. Elmasry, Multi-Threshold CMOS Digital Circuits—Managing Leakage Power. Norwell, MA: Kluwer, 2003.
[15] J. Kao and A. Chandrakasan, "MTCMOS sequential circuits," in Proc.27th Eur. Solid-State Circuits Conf., Sep. 2001, pp. 317–320.
[16] J. Kao, S. Narendra, and A. Chandrakasan, "MTCMOS hierarchicalsizing based on mutual exclusive discharge patterns," in Proc. DesignAutom. Conf., Jun. 1998, pp. 495–500.
[17] H. Kawaguchi, K. Nose, and T. Sakurai, "A super cut-off CMOS(SCCMOS) scheme for 0.5 V supply voltage with picoampere stand-bycurrent," IEEE J. Solid-State Circuits., vol. 35, no. 10, pp. 1498–1501,Oct. 2000.
[18] S. Kosonocky, M. Irnmediato, P. Cottrell, T. Hook, R. Mann, andJ. Brown, "Enhanced multi-threshold (MTCMOS) circuits using variablewell bias," in Proc. Int. Symp. Low Power Electron. Design Conf., 2001,
pp. 165–169. [19] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, andJ. Yamada, "1 V power supply high-speed digital circuit technology with
multithreshold-voltage CMOS," IEEE J. Solid-State Circuits, vol. 30,no. 8, pp. 847–854, Aug. 1995.
[20] S. Shigematsu, S. Mutoh, Y. Matsuya, Y. Tanabe, and J. Yamada, "A1 V high-speed MTCMOS circuit scheme for power-down applicationcircuits," IEEE J. Solid-State Circuits, vol. 32, no. 6, pp. 861–869,Jun. 1997.
[21] P. Heydari and M. Pedram, "Ground bounce in digital VLSI circuits,"IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 11, no. 2,pp. 180–193, Apr. 2003.
[22] S. Kim, S. Kosonocky, and D. Knebel, "Understanding and mini-mizing ground bounce during mode transition of power gating struc-tures," in Proc. Int. Symp. Low Power Electron. Design, Aug. 2003,MTCMOS circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57,no. 8, pp. 2053–2065, Aug. 2010.

Author(s) Bibliography

Meenakshividya P pursued her B.E. Degree in Electronics and Communication Engineering at University of Madras, Chennai, and received her M.E. Degree in VLSI Design from Anna University, Chennai, India. She is currently working as Associate Professor at Easwari Engineering College, Chennai, India. Ms.Meenakshi Vidya has published more than 25 papers in National and International Conferences and 5papers in International journals. Her research interests includes low power VLSI design, Electromagnetic Interference reduction and ASIC design. She is a member of IEEE, IET & ISTE.

Dr. S. Sudha. received her B.E degree in Electronics and Communication Engineering from Madurai Kamaraj University, Tamil Nadu, India, in 1996 and M.E degree in Applied Electronics from Madurai Kamaraj University, Tamil Nadu, India, in 2000 . She received Ph.D degree in Medical Imaging from Anna University, Chennai. She is working as Professor in Department of Electronics and Communication Engineering at Easwari Engineering College, Chennai, India. She has 22 years of teaching experience at college level. She has published twenty papers in International, national journals. Her area of interest includes image processing, Signal processing. She is a member of ISTE, IETE and IET.