Design and Analysis of Low Power and High Speed Hybrid 1 bit full adder circuit

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Abstract- Full adder circuit is a digital circuit that performs an arithmetic operation in computer and other kind of processor for calculating addresses, table indices, increment and decrement operator and in other similar operations. In this paper low power and high speed 1 bit full adder circuit is proposed 130 nm technology. The performance parameter power consumption , propagation delay and power delay product are compared with previous existing full adder circuit and achieve the better power dissipation as well as delay with respect to my proposed full adder circuit. The power dissipation of full adder circuit is improved in comparison to 14 T FA and Conventional CMOS FA circuit. All simulation are done at a temperature of 27 ^{0}C by using Mentor Graphics Pyxis EDA Tools.

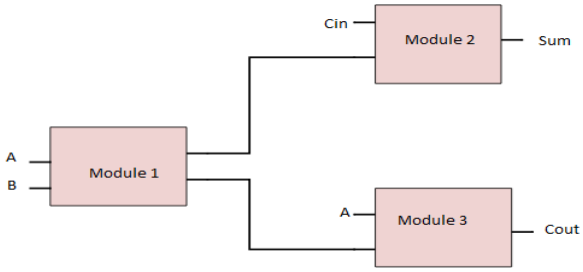
Keyword – power dissipation, delay, GDI, Conventional CMOS

Introduction – Full adder is a building block for most of the VLSI applications, such as video processing microprocessor, digital signal processing and in different arithmetic operation. [1] The performance of the digital circuits can be optimizing with the help of using different logic styles. The different designing are in the form of 14T FA and conventional CMOS circuit.

14 T FA – it is a full adder circuit [2] that containing the three input signal A, B and C_{IN} and the output contains sum and Cout. In this FA there has no threshold loss of sum and Cout signals and creating a problem of output glitches and a sub threshold leakage power component. Incomplete voltage swing of the XOR gate output signal for the case of A = B =0, where the PMOS transistor will be ON while the NMOS will not be totally OFF, leading to a larger sub threshold current.

Conventional CMOS - : This full adder [3] is designed by using the XOR gate of four transistor and multiplexer of 2 : 1 by using two transistor the performance is totally improved on the basis of XOR gate this full adder designing is focused on power improvement.

Proposed Methodology - The proposed full adder circuit is representing by three blocks which is given in the fig 1. Module 1 representing the XOR-XNOR [4] circuit using GDI technique, Module 2 generate the SUM signal and Module 3 generate the carry out signal. The complete proposed full adder circuit is optimized the propagation delay and power consumption due to this, low power and better delay is achieved.



Module - 1

Full adder has been derived with various structure for the improvement of power consumption, propagation delay, power delay product as well as complexity. In the frist module the XOR- XNOR MODULE are used using GDI Technique [5-6] to achieve the better delay. In this , there are 8 transistor are used to generate the balance XOR-XNOR functions.

Where,

XOR = A·B + A B·

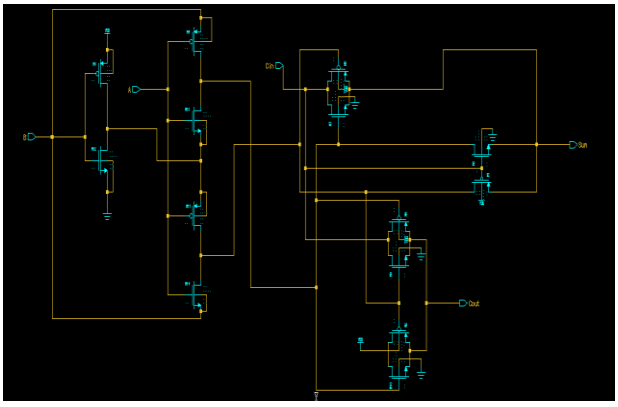
XNOR =AB + A· B·

This stage is giving the full swing with low voltage this module is cascading with 2^{nd} and 3_{rd} module and producing sum and carry signal.

Module – 2&3

The module 2 and 3 are based on transmission function theory [6] this logic is providing a better performance for high speed. In module 2 there are four transistors used and in module 3 the four transistor are used from the module 2 and module 3 sum and carry signal are achieved. This transmission logic gate providing the better speed**.**

Proposed FA circuit



Result and observation-

The full adder circuit is designed and simulated using Mentor Graphics Pyxis EDA Tools. This designed circuit are simulating in 130 nm CMOS technology at temperature of 27 ^{0}C this designed proposed circuit is analysed and compare with some existing hybrid full adder on the basis of performance parameter such as propagation delay, power delay product as well as power consumption by using Mentor Graphics Pyxis schematic EDA tools. Which of them the better delay has achieved in compare to other existing full adder using transmission gate with full swing and better driving capability.

Table 1. Performance comparison at v_{DD}= 0.6

Design	*Power dissipation*	*Delay*	*Power delay product*
14 T FA	16.215 uw	22.930 ns	371.809 *10^{-15} w-s
Conventional CMOS	36.214 uw	25.930 ns	939.029*10^{-15} w-s
Proposed FA	16.520 nw	21.625 ns	357.245 10^{-18} w-s

Table 2. Performance comparison at V_{DD} =0.8 V

Design	*Power dissipation*	*Delay*	*Power - delay product*
14 T FA	73.634 uw	22.561 ns	1661.25*10^{-15} w-s
Conventional CMOS	95.342 uw	26.9309 ns	2567.56*10^{-15} w-s
Proposed FA	589.44 nw	21.648 ns	1276.18* 10^{-18} w-s

Table 3. Performance comparasion at V_{DD} = 1 V

Design	*Power dissipation*	*Delay*	*Power delay product*
14 T FA	184.085uw	23.314 ns	4291.021 *10^{-15} w-s
Conventional CMOS	135.674uw	26.9309 ns	3653.70* 10^{-15} w-s
Proposed FA	10.447 nw	21.654 ns	226.219* 10^{-18} w-s

Table 4. Performance comparasion at V_{DD} =2 V

Design	*Power dissipation*	*Delay*	*Power delay product*
14 T FA	1.163mw	24.561 ns	28.564* 10^{-12} w-s
Conventional CMOS	216.451uw	26.109 ns	5651.29 *10^{-15} w-s
Proposed FA	1.464 uw	23.876 ns	34.9541 0^{-15} w-s

Table 5. Performance comparison at V_{DD} = 3 V

Design	Power dissipation	Delay	Power delay product
14 T FA	10.163mw	37.659 ns	382.636* 10^{-12}w-s
Conventional CMOS	2.456 mw	31.9309 ns	78.420*1 0^{-12} w-s
Proposed FA	10.231 uw	24.654 ns	252.23*1 0^{-18} w-s

Conclusion - The proposed full adder circuit has an improvement in low power and better propagation delay comparison with some existing full adder circuits. The designed FA circuit This proposed FA circuit is suitable for low power and high speed applications.

References –

[1] P. Bhattacharya, B. Kundu , S Ghosh, V. Kumar, and A Dandapat, "Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit'', IEEE Transactions on Very Large Scale Integration Systems, vol. 23 (10), pp. 2001-2008, 2015.

[2] Z. Abid, H. E. Razouk, D. A. El-Dib, "Low power multipliers based on new hybrid full adders", Microelectronics journal, vol. 39 (12), pp. 1509 -1515, 200

[3] S.Wairya, R. K. Nagaria, and S. Tiwari, "Comparative performance analysis of XOR- XNOR function based high-speed CMOS full adder circuits for low voltage VLSI design", International journal of VLSI Design & communication systems, vol.3 (2), pp. 221-242

[4] Pankaj Kumar, and Poonam Yadav, "Design and Analysis of GDI based full adder circuit for low power applications", International journal of engineering research and applications, vol. 4 (3), pp. 462-465, 2014.

[5] Alireza Saberkari Shahriar B.Shokohi. "A novel low-power low voltage CMOS1 bit full adder cell with the GDI technique, IJME intertech Conference vol. 34 (5) pp.501-12 2006

[6] A. Maheshwari, and S. Luthra, "Low power full adder circuit implementation using Transmission gate", International journal of advanced research in computer and communication engineering, vol. 4 (7), pp. 183-185, 2015.

[7] A. Morgenshtein , I Shwartz and A. Fish, "Full swing gate diffusion input logic: Case study for low power CLA adder design'', Integration, the VLSI Journal, vol. 47(1), pp. 62-70, 2014.