Optimization Of Domino Logic In Terms Of Power dissipation And Delay For High Speed Applications using CMOS

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Abstract: Propagation delay and power dissipation is the measure concern in designing of a VLSI circuit at 90nm or 45nm technology. For high performance circuit designing with ability of high speed with low power dissipation the existing technology is modify using an extra NMOS circuit in the existing technology for decreasing the power and delay of the circuit. This research is done in term of decreasing the power and delay of the domino logic circuit using EDA tanner tool. The modified domino logic circuit using CMOS technology is design at s-edit and simulation is done at t-edit and w-edit for getting the result in form of delay, average power, EDP and PDP at various supply voltages from 1v to 0.5v.

1. Introduction

Dynamic logics are preferred for high speed processor due to smaller area and high speed characteristics as compared to the static CMOS logic circuits[1] [2].Since domino logic circuit has high speed as compared to static CMOS logics ,its achieves high speed due to lower noise margin but due to the downscaling of the technology noise immunity of domino logic increases. Due to increasing noise immunity
power consumption also increased. So to decrease the power consumption of the circuit voltage scaling should be done but due to voltage scaling increase leakage current due to short channel effects[9].The desire to optimize the design metrics of performance, power, area, cost, and time to market (opportunity cost) has not changed since the inception of the IC industry. In fact, Moore's Law is all about optimizing those parameters. [5] [4] However, as scaling of manufacturing nodes progressed towards nm, some of the device parameters could not be scaled any further, especially the power supply voltage, the dominant factor in determining dynamic power and optimizing for one variable such as performance automatically translated into big compromises in terms of power[3]. In terms of power scaling of technology reduces the thickness of gate oxide that cause an exponential increase in and gate leakage current. That's why it degrade the performance of a domino circuit at high frequency.
To reduce the power consumption of a domino logic circuit many techniques has been proposed

in the various papers. These techniques are the modified forms of a footerless domino logic circuit (FDL)[6]. In this paper the existing technology has been discussed and compare with the proposed
domino technique in terms of average power, delay, EDP and PDP.

2. Domino Techniques.

For high speed processor the domino logic circuit is preferred over dynamic logic since it consist of a single PMOS circuit in pullup network which reduces area and as well as power consumption as compared to dynamic logic CMOS. So there are many existing domino logic circuits for improving performance of domino circuit in terms of power dissipation and delay.
So the first technique is domino logic circuit.
The circuit consist of a PMOS circuit and a evaluation logic cicuit which is an OR gate. In pre-charge to the PMOS phase the PMOS transistor is on and output is generated due to it. In evaluation logic circuit the output is depend on the input of NMOS. The circuit is shown in fig 1.

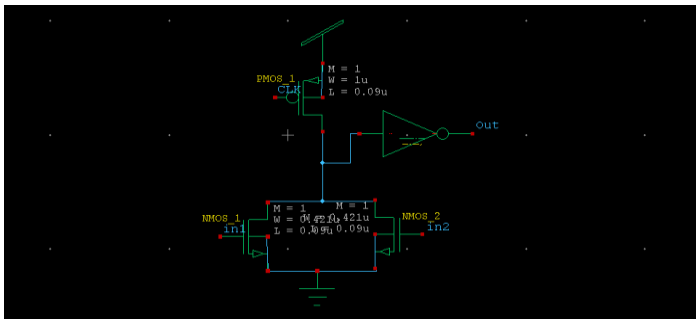


Fig1: domino logic circuit.

Since it cannot hold the output until the next input applied power dissipation is larger in the circuit. So to improve the performance a new technique is imposed i.e. footer domino logic circuit as shown in figure 2.
It consist of a keeper circuit which hold the circuit at dynamic node. The pull up circuit consist of two PMOS circuit one pre-charge and keeper circuit when the clock is low during the pre-charge phase, the pre-charge transistor (P2) turns ON and dynamic node charges to supply voltage (vdd) through P2. When the clock becomes high in the evaluation phase, the output of the circuit changes according to the inputs applied in pull-down network. At this time, keeper transistor turns on and connects the dynamic node to supply. Thus, prevents any undesirable discharge of the dynamic node due to charge
sharing problem of pull down network. Therefore, increase in the size of keeper transistor improves the robustness of FLDL logic·

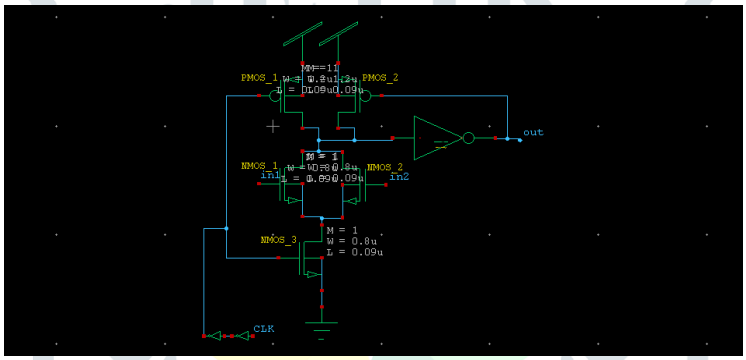
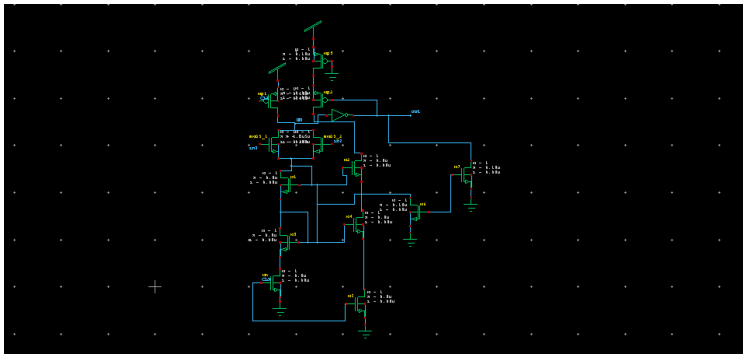


Fig 2: footer domino logic circuit.

FLDL has drawback i.e. when all inputs are low during the evaluation phase, a leakage current flow through pull down network due to sub-threshold and gate tunnelling current.
So the another technique is introduced that is Footed Domino Logic (FDL)[] technique, the leakage current is reduced by inserting a footer transistor N1in series with evaluation network as shown in the figure 2. But FDL technique has the drawback that footer transistor introduces a delay in the circuit that reduces the speed of the circuit. The Robustness of FDL decreases for high Fan-in gates. To reduce the delay, current mirror transistors N2 and N3 are inserted in the FDL logic shown in fig 2. But by inserting these transistor reduce delay but increase discharging current. In order to stop discharging of the dynamic node, transistor N4 provides a feedback path from the gate of the current mirror.
Another technique to improve the power and delay of the circuit a new approach is shown in figure 3. In this circuit a new approach is used for the modification of circuit along with the pre-charge phases and evaluation phase.



The past method demonstrate a little power delay and configuration in 90nm CMOS innovation and with 1v power supply. Footer current mirror utilized in such a way that any noise signal generate at it spill from the transistor M4 and M5 since it create stacking effects because of which voltage drop diminishes at M2 transistor.

3. Modified domino logic circuit.

So these all technique has not provided so much satisfication in terms of power and delay so the circuit is further modified for reducing delay and power consumption. The circuit has precharge phase and evaluation phase which gives the property of an OR modified domino logic circuit.

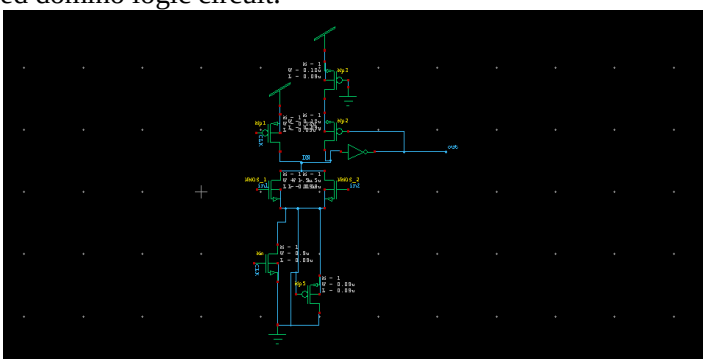


Fig 4: modified domino logic circuit.

The simulation of the circuit is done at different voltages from 1v to 0.5v and the circuit shown the behavior of an OR modified domino logic. The output waveform of the circuit is shown in figure 5.

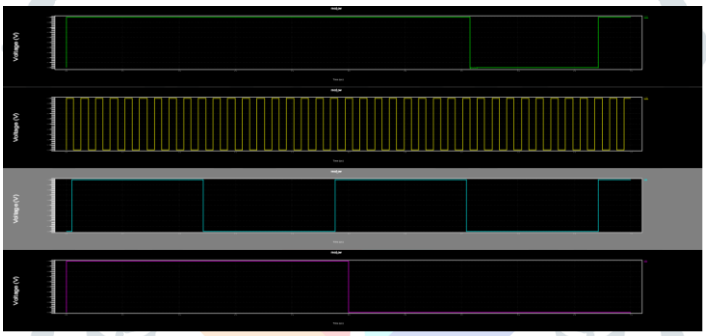


Figure 5: waveform of OR modified domino logic

4. Result

In the given table we compare the results of all the existing models at 1v using 90nm technology. The results are compared in terms of delay, average power and PDP.

The comparison all models of domino logic is shown in table 1.

Domino logic	Average power(uw)	Delay(*10^-10)	PDP(*10^-19)
Footerless	78.4	155	1215.2
footer	3.9	103	328.5
Domino logic at shiksha	0.074	2.55	118.3
Modified domino logic	0.063	0.635	40.004

Table1: comparison of previous domino logic and modified domino logic in terms of power, delay and PDP.

Another table is given in terms of power delay and PDP for modified circuit by changing there supply voltage from 1v to 0.6v. the comparison is shown in table 2.

Supply voltage	1v	0.9v	0.8v	0.7v	0.6v
Average power(uW)	0.063	0.048	0.035	0.026	0.019
Delay(*10^-10)	0.635	0.709	0.911	1.292	2.275
PDP(*10^-19)	40.0	34.0	31.9	33.6	43.2

Table 2: power, delay and PDP at different power supply.

5. Conclusion and Future Work

In the paper, we have shown different diverse techniques and modification circuits of domino logic which simulated on IBM 90nm. The proposed domino logic gives the maintainability power supply and less power and delay in the domino logic circuit. So the circuit is useful for low power dissipation domino circuit in low power VLSI circuits. The circuit can be further modified for getting lower complexity and less power delay using different techniques.

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