Effect of W/L Variations on SRAM Read-Write Timing Cycle in Deep Nano Process Technology

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Abstract: **In current scenario of the scaling to the CMOS in deeper nano process technology, read-write stability of SRAM cell has become a challenging task. The need of compact and the low power VLSI circuit is highly desirable. The SRAM cell static noise margin (SNM) has to be improved, to enhance the power performance. With respect to the future technologies, SRAM cell read-write stability has become a primary concern in deep nanometer regime due to transistor-dimension variability and decreasing power supply voltages. 6T-SRAM can be enhanced for significant stability by deciding the cell structure, device threshold voltages, word line voltages, and the cell ratio. In this paper, the read and write timing cycle has analyzed by varying W/L ratio of 6T SRAM cell. By varying the cell ratio, we keep observation on read and write stability upto a certain W/L ratio and then after, analyzed flipping in timing cycle at 16nm process technology. All the simulations have been carried out using cadence tool and legend MSIM tool.**

Index Terms **- Static Random Access Memory (SRAM), Bit Line (BL), Bit Line Bar (BLB), Width/ Length Ratio (W/L Ratio), NMOS access transistor (NAX), NMOS Pull Down transistor (NPD), PMOS.**

I. INTRODUCTION

VLSI research field has emerged at large extent that consistently moves towards the growth in direction of research. As in the field of VLSI, the process technology and supply voltages continuously moderates and hence its impacts on the dimension of the circuits and its performance stability have become a tremendous concern. In such a case, the SRAM voltage does not scale with technology and could even be increased as variability intensifies. With advancement of the technology towards size of the devices, the analysis of various parameters become very tedious. In present scenario, industry works on 14nm process technology and have fabricated devices successfully. Further, this process technology is keep on going more deep. Static Random Access Memory (SRAM) is a category of semiconductor memory, to store one bit data. In the field of multimedia applications, system on chip (SOC), high-performance memory unit, SRAM become faster memory unit in a wide range of microelectronics applications. As per the Moore's Law, the number of transistors fabricated per square inch on integrated circuits has doubled every year since their invention. With the enhancement of new technology, transistor size is reduced by the large factor and due to this transistor scaling, it takes significant consideration in the performance and cost of integrated circuits. The growth of the device count per chip and its applications in microelectronics increased exponentially and due to this reason, faster memory unit is required to handle the performance. The SRAM has frequently used in the integrated systems where high integration density and reliability in performance are required.

II. STANDARD 6T SRAM CELL

Before starting the analysis, the basic operation of SRAM cell is taken into consideration. The schematic diagram of 6T SRAM cell is shown in Fig.1. During read operation, the WL voltage (V_{WL}) is raised, and the memory cell discharges through either BL (bit line) or BLB (bit line complement), depending on the stored data on nodes Q and QB. A potential difference is created on these nodes. A sense amplifier converts this differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, V_{WL} is raised and the BLs are forced to either V_{DD} (depending on the data), overpowering the contents of the memory cell. During hold, V_{WL} is held low and the BLs are left floating or driven to V_{DD}.

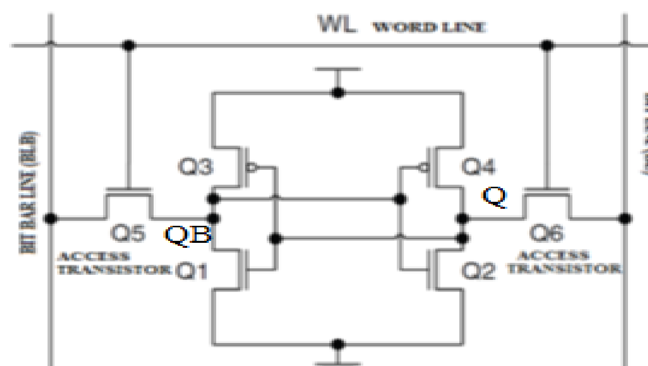

Fig.1 Conventional 6T SRAM Cell

III. THE OPERATION OF SRAM CELL

i. **Standby Mode: Idle State of the circuit**

If the word line is not asserted, the access (Pass) transistors will disconnect the cell from the bit lines. The two cross coupled inverters formed by two inverter connected back to back, reinforce each other as long as they are disconnected from the outside world and they will retain the data which they have already stored in the memory cell.

ii. Read Mode: Request of the data

Assuming that the content of the memory is a 1, stored at node 'Q' as shown in fig.2. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line signal with the high voltage pulse enabling both the access transistors. The second step occurs when the values stored in Q and are transferred to the bit lines, one of the bit line will discharge through the driver transistor and the other bit line will be pulled up through the load transistors toward V_{DD}, a logical 1. If the content of the memory was a 0, the opposite would happen if the memory cell was stored the logic 1.

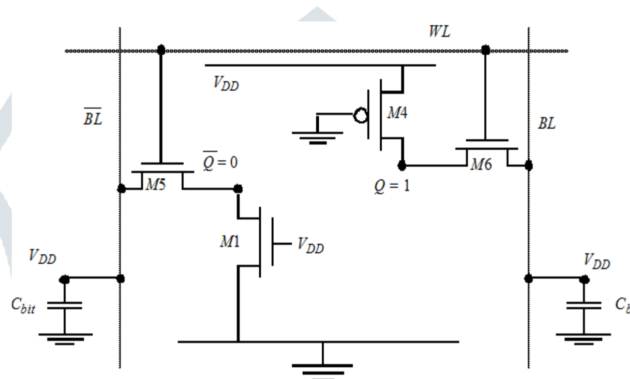

Fig. 2: Read Mode Equivalent Circuit of SRAM cell

iii. Write Mode: Updation of cell contents

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit line, i.e. setting BL to 0 and to 1 in the fig.3. This is similar to applying a set pulse to a SR-latch, which causes the flip flop to change state. '1' is written by inverting the values of the bit lines. Word Lines is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled 2 inverters. The complete obtained read / write timing cycle is shown in fig.4.

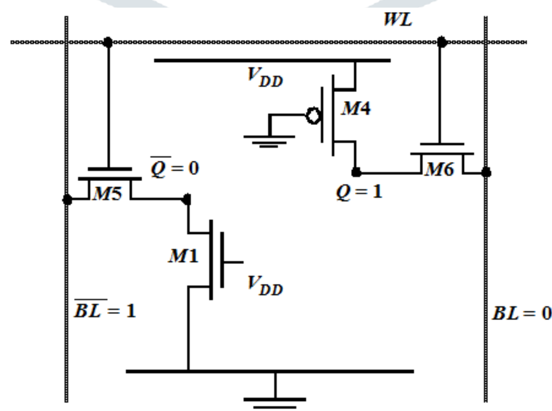

Fig.3: Write Mode Equivalent Circuit of SRAM cell

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IV. SIMULATION RESULT OF SRAM CELL USING TOOLS

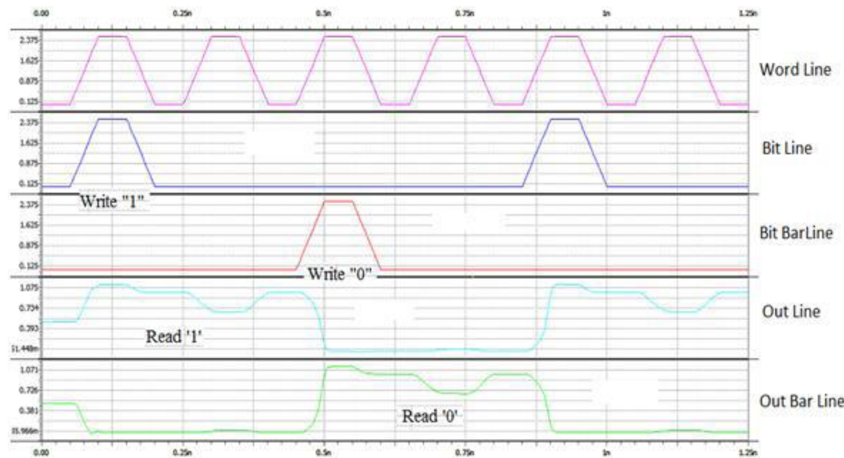

Fig.4: Read-Write timing cycle of SRAM cell

The simulated waveform of SRAM cell before on-die variations in W/L ratio of transistors is shown above in fig.4. Both bit line and bit bar line are showing their complemented nature of data storage. The potential difference created between these lines are sensed by sense amplifier and accordingly it provides logical output as a result.

V. MECHANISMS BEHIND FAILURE OF AN SRAM READ-WRITE CYCLE WITH TRANSISTORS W/L VARIATIONS

On-die variations in the process parameters (e.g., threshold voltage, channel length, channel width, etc., of the transistors) result in the mismatch in the strength of the different transistors in an SRAM cell. This device mismatch can result in the failure of the SRAM cell. The parametric failures in an SRAM cell (fig.5) are principally due to:

Destructive read (i.e. flipping of the stored data in a cell while reading —known as read failure)

- Unsuccessful write (inability to write to a cell—defined as write failure)
- An increase in the access time of the cell resulting in a violation of the delay requirement—defined as access- time failure
- The destruction of the cell content in standby mode with the application of a lower supply voltage (primarily to reduce leakage in standby mode)—known as hold failure.

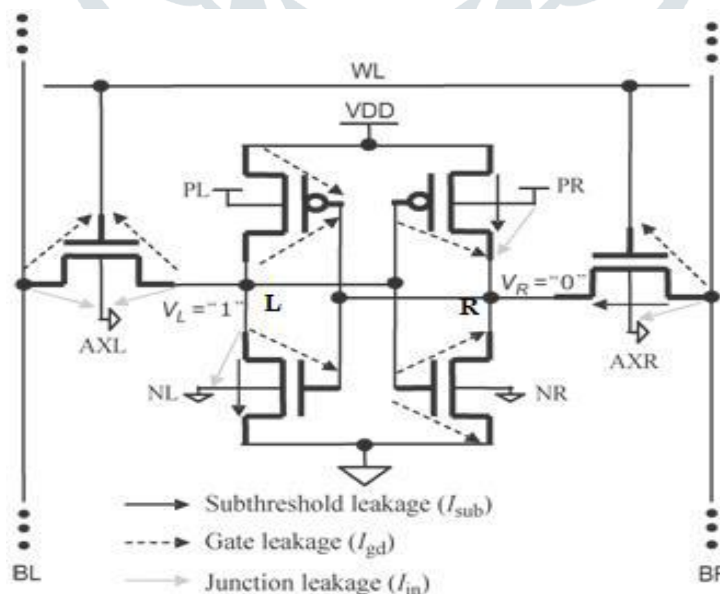

Fig.5: SRAM Cell with Various Leakage Currents Causing Read and Write Failures

A measure of the relative strength of the AXR (right access transistor) and NR (right NMOS transistor) is the ratio of the "ON" current [known as the beta-ratio ($BR_{npd-nax}$)] of these two transistors and is given by-

$$BR_{npd\text{-}nax} = \frac{\beta npd}{\beta nax} = \frac{\frac{\mu_{eff}\, Cox\, W_{npd}}{L_{npd}}}{\frac{\mu_{eff}\, Cox\, W_{nax}}{L_{nax}}}$$

Where μ_{eff} is the effective mobility, Cox is the oxide capacitance. W_{nax} and W_{npd} are the widths of the access transistor and the pull-down NMOS respectively and L_{nax} and L_{npd} are the lengths of the access transistor and the pull-down NMOS respectively. A decrease in beta-ratio ($BR_{npd-nax}$) increases V_{READ}, thereby facilitating read failure. Hence, while designing an SRAM cell, the size of the access transistor is usually reduced from that of the pull-down NMOS to increase $BR_{npd-nax}$.

VI. CONSIDERABLE EFFECT OF W/L VARIATIONS

- By variations in Access Transistor (NMOS) W/L Ratio -

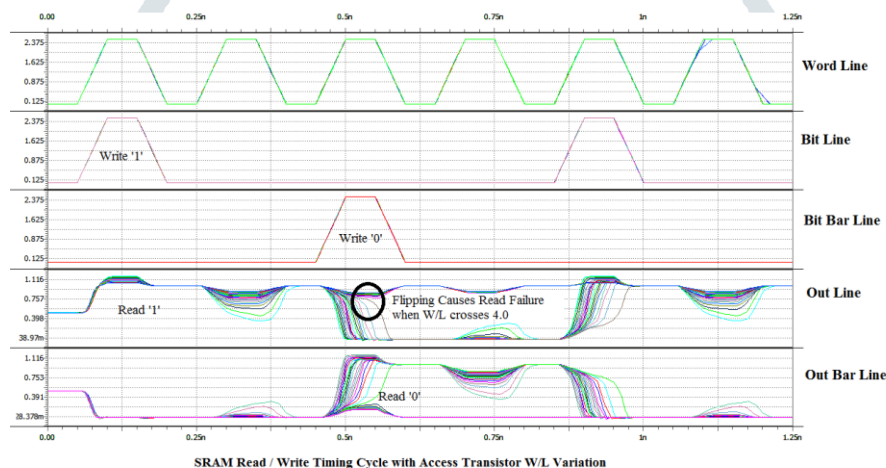

Fig.6: Occurrence of flipping in NMOS transistors causing read-failure

- By variation in PMOS W/L Ratio -

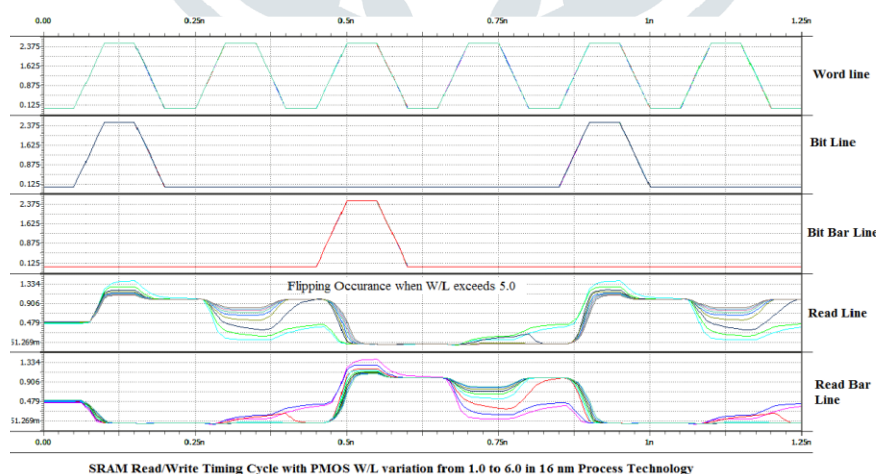

Fig.7: Occurrence of flipping in PMOS transistors causing read-failure

In the simulated waveform shown in fig.7, it has been observed that there are more flipping occurrences for W/L variations in PMOS transistor using 16nm Process Technology. The theory behind the more flipping in the W/L ratio of PMOS transistor is similar to that of NMOS transistor but one of the reason is the lesser hole mobility. So, it must be avoided to vary in PMOS transistor dimension.

VII. CONCLUSIONS

This paper presents a read and write timing-cycle analysis of a static random access memory (SRAM) cell having 6T SRAM cell architecture with variations in W/L ratio of transistors. The designing of SRAM 6T cell has been performed using 16nm process technology. Various analysis such as read failure, write failure, hold failure, access time failure and delay in access time are being analyzed in this paper in context with SRAM. Effects of on-die variations of MOS transistor dimensions (length and width) have been observed and analysed mathematically. Occurrences of flipping during read and write operation as failure are also observed and removed by restricting the on-die variations of MOS transistors.

VIII. ACKNOWLEDGEMENT

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