DESIGN OF 32- BIT CARRY SELECT ADDER USING FULL SWING GATE DIFFUSION INPUT (FS- GDI) TECHNIQUE FOR DIGITAL SIGNAL PROCESSING APPLICATIONS.

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Abstract-Designing of Low Power digital circuits is the challenging task in VLSI Industries. In this Paper we design low power & high speed 32 bit carry select adder using swing restoration buffer in gate diffusion input technique which is called full swing gat diffusion input techniques. Large number of carry select adder structures are available, we are designing carry select adder using Brent Kung adder and Binary to excess 1 converter instead of previous Ripple carry adder. This design drastically reducescarry propagation delay as well as power consumption of carry select adder. This design is prepared using Tanner EDA tools 15.1 and 180nm process technology.

***Index Terms*- Full-SwingGDI, CSLA, Brent Kung Adder, Binary to Excess 1 Converter, Multiplexer**

1. INTRODUCTION

Design of less occupied area, less delay, low power consumption and high speed adder logic systems are very important factors in the field of VLSI designing. Adder being one of the most popularly used components in digital circuitry as it performs an addition process and generates a carry and Sum. In conventional digital adder circuits, carry propagation delay being major hurdle that limits the speed of the addition process.

To resolve the problem of carry propagation delay, carry select adder was brought into existence that sorts the problem of propagation delay by generating partial sums and carry by taking into account both the carries viz. is Cin=0 and Cin=1, designed and assisted with Brent kung adder and binary to excess 1 converter to get better results . To further improve performance more in aspects of power consumption and delay, another technique introduced was Gate diffusion input technique which is even more improvised using swing restoration buffer called full swing gate diffusion input technique. Thus an efficient adder with less delay and less power consumption performing large no.of additions can be designed using above suggested method.

1.1 Gate Diffusion Input Technique:- Gate diffusion input technique works for low power and less area in VLSI digital circuits. This technique was found more efficient over all previously used techniques of CMOS, Transmission gate and Pass Transistor due to its better results in terms of power and delay. This technique uses very less number of transistors as compared to others and even design many complex functions using only 2 transistors.

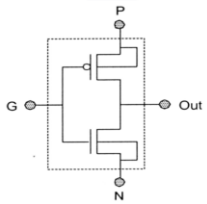


Fig1:- Basic GDI Cell

This logic style undergoes a disadvadvantage of reduced output voltage swing. The reason behind this drawback is threshold drops i.e. the output is either high or low voltage or deviates from VDD or GND. This in turn results in poor performance and also increases short circuit power.

Table 1: Different Logic Function Realization using GDI Cell.

N	P	G	OUT	Function
0	B	A	$\bar{A}$B	F1

B	1	A	$\bar{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
$\bar{B}$	B	A	A ⊕ B	XOR
C	B	A	$\bar{A}$B+AC	MUX
0	1	A	_	NOT

2. Construction of CSLA Adder

A[31:28]B[31:28] A[15:12]B[15:12] A[11:8]B[11:8] A[7:4]B[7:4] A[3:0] B[3:0]

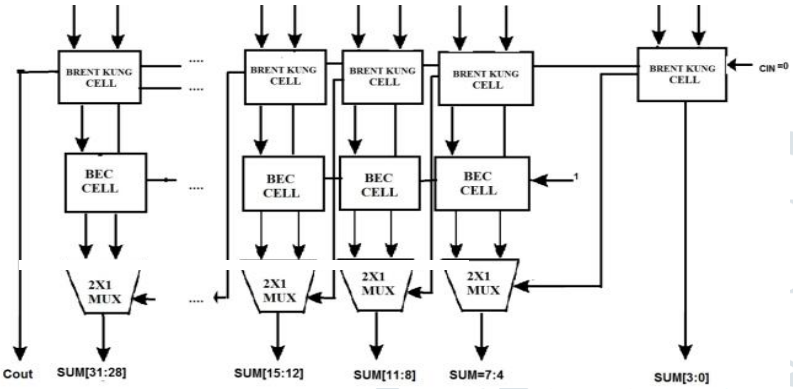


Fig 2: - Architecture of CSLA Adder

2.1 Brent Kung Adder

Brent kung adder is a type of Parallel prefix adder which is proposed and widely used over other prefix adders in spite of its long critical path and slow speed addition due to its capability of connecting gates in a way that minimize chip area.

The adder designed performs addition using Generation signal Gi and propagation signal Pi which finally evaluate sum through three stages :-

Initial Processing Stage.

Prefix Carry Stage.

Final -Processing Stage.

***Initial-Processing Stage*:-** This is an initial stage which gives two important signals called generation signal and propagation signal Gi and Pi respectively.

***Prefix Carry Stage* :-** This stage further simulate the two signals coming from previous stage using three cells namely black cell, gray cell and buffer which all combines to generate carry at the output.

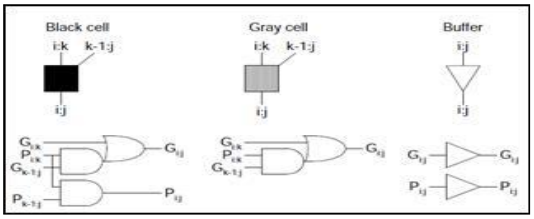


Fig 3:- Prefix Carry Unit.

Black Cell:- This cell of the circuit is formed with a combination of one OR gate and two AND gate. As a result gives Gij and Pij as output.

Gray Cell:- This cell of the circuit is made using one OR and one AND gate resulting generation signal Grj as its output.

Buffer Cell:- This cell is simply used to amplify the strengths of the two signals.

Final Processing Stage:- This is the final stage of Brent Kung adder that finally produces sum by performing an Ex-OR operation between carry of the previous stage and the propagation signal.

2.2. Binary to Excess 1 Converter

This is simply a digital device that adds an excess 1 to its input and gives an output accordingly. This feature of the device proved beneficial to reduce area and power consumption of the CSLA earlier designed using Ripple Carry adder by replacing the same with BEC.

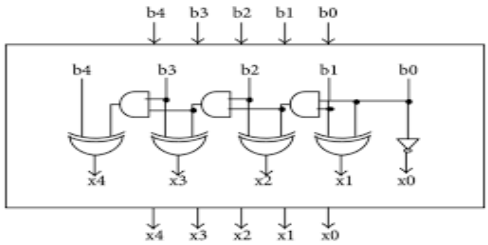


Fig 4:- Binary to Excess Converter

TABLE 2:- Binary to Excess 1 Converter

Binary Logic $B_0\ B_1\ B_2\ B_3$	Excess-1 Logic $X_0\ X_1\ X_2\ X_3$
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

2.3. Multiplexer

To design a 32 bit carry select adder, this paper uses 2:1 Multiplexer which has two input lines and one select line. Select line of each multiplexer receives previous carry at its input line in accordance to which desired Sum is displayed as output.

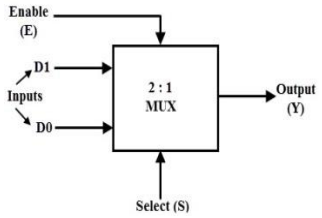


Fig 5:- 2X1 Multiplexer

Table 3:- Truth Table of 2:1 Mux

A	B	S	Y
0	0	0	0
0	1	0	0
1	0	1	0
1	1	1	1

3. Implementation of Carry Select Adder

This paper we have designed CSLA using Brent Kung Adder ,Binary to Excess-1 Converter and 2X1 Multiplexer. All components are designed and implemented by Full Swing Gate Diffusion Technique.

3.1. Designing of Brent Kung Adder:-

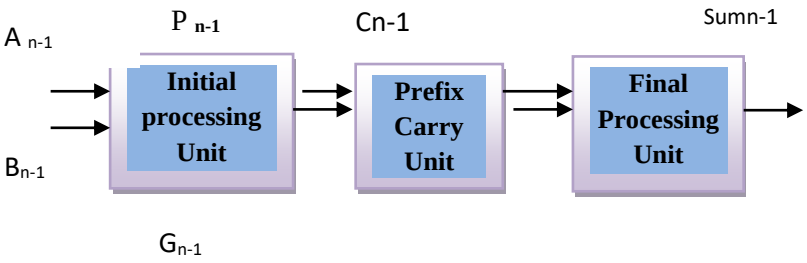


Fig 6:-Block Diagram of Brent Kung Cell

Initial Processing Stage:-

$Gi = a.b$ (1)

$Pi = a \oplus b$ (2)

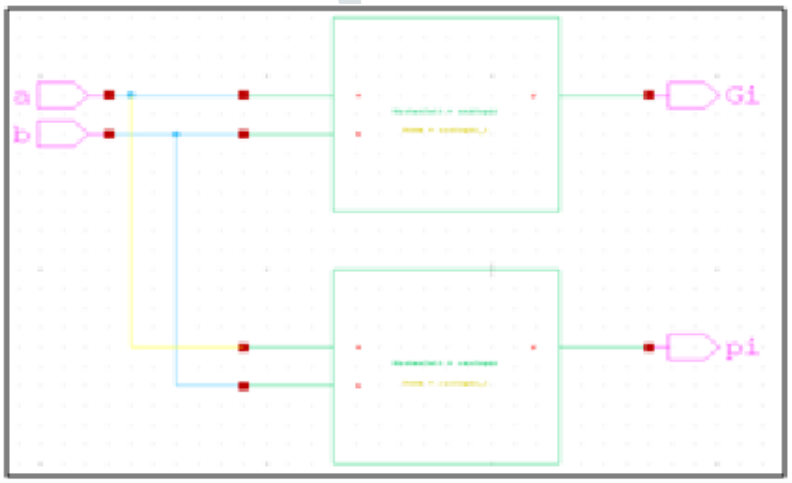


Fig7:- Logic diagram for Initial Processing Stage

Prefix Carry Stage:-

$Gij = Gik + (Pik.Gjk)$ (3)

$Pij = Pik.Pjk$ (4)

$Grj = Gk + (Pk.Gkj)$ (5)

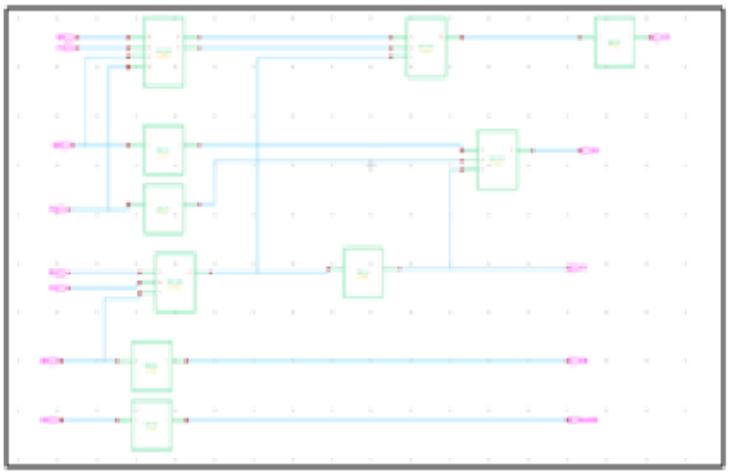


Fig 8:-Logic diagram of Prefix Carry Stage

Final Processing Stage:-

$$S0 = Cin \oplus P0 \quad (6)$$
$$S1 = C0 \oplus P1 \quad (7)$$
$$S2 = C1 \oplus P2 \quad (8)$$
$$S3 = C2 \oplus P3 \quad (9)$$

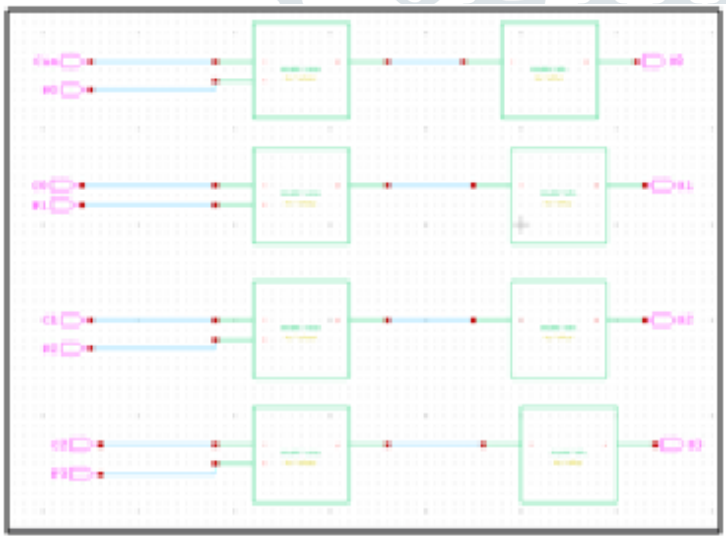


Fig9:- Logic Diagram of Final Processing Stage

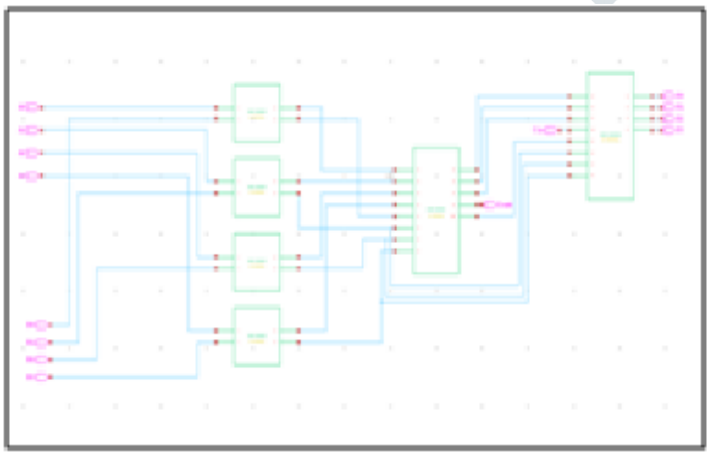


Fig10:-Logic Diagram of 4-Bit Brent Kung Adder

3.2. Binary to Excess 1 Converter:-

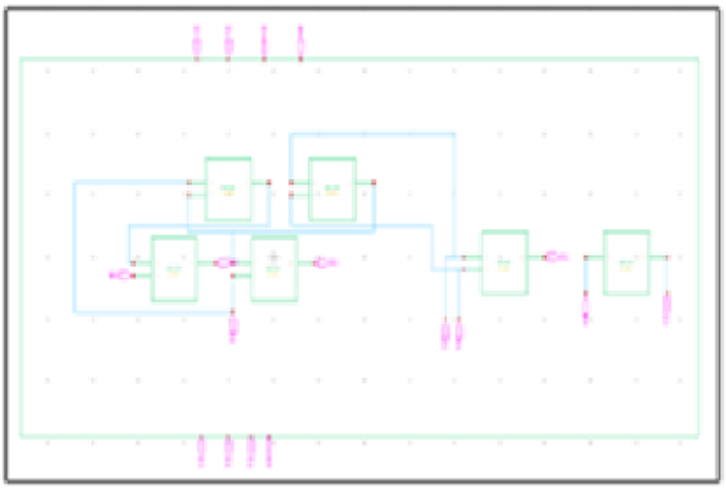


Fig11:- Logic Diagram of 4-Bit Binary to Excess 1 Converter

3.3 . 2:1 Multiplexer:-

$Y = A.\overline{S} + B.S$ (10)

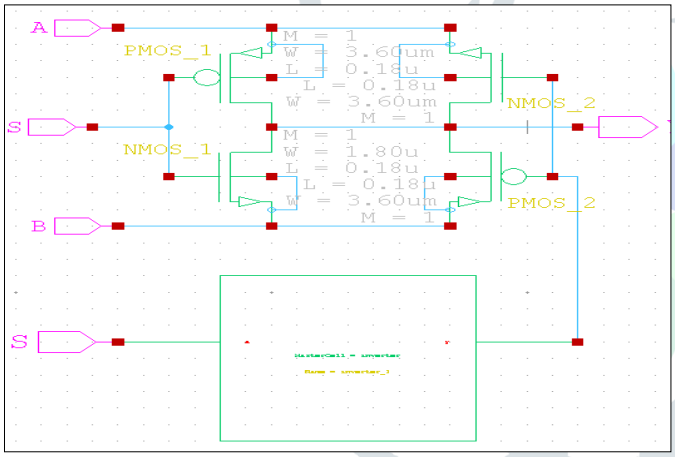


Fig12:- Logic Diagram of 2:1 MUX

3.4. 32 Bit Carry Select Adder:-

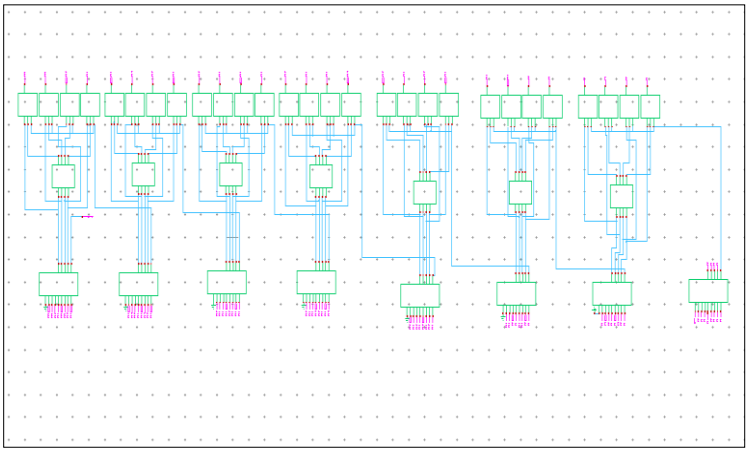


Fig13:- Logic Diagram for 32- Bit CSLA

4. Simulation Results & Discussion

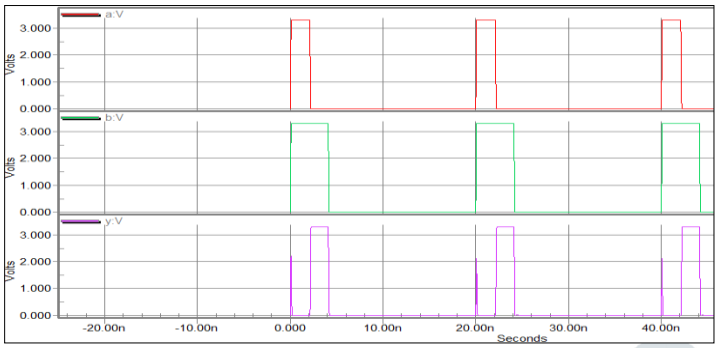


Fig 14: - Output Waveform of XOR Gate using FS- GDI

- For inputs at a= 0 & b=1 , o/p obtained y =1b/w 10ns- 20ns of max. up to 3.3 V.
- For inputs at a=1 & b= 1, o/p y=0 b/0ns- 10ns and hence verified the truth table.

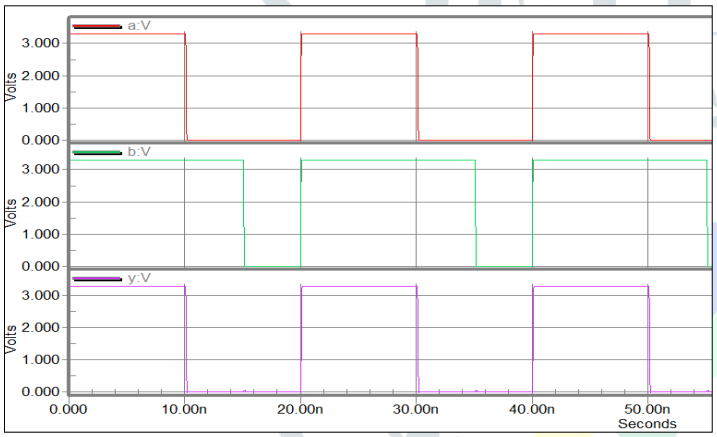


Fig15:-Output Waveform of AND Gate using FSGDI

- For inputs a= 1 & b=1, o/p obtained is y = 1 b/w 0- 10ns up to max. of 3.3 V
- For inputs a=0 & b= 1, o/p obtained is y=0 b/w 30ns- 40ns up to max. of 3.3 V

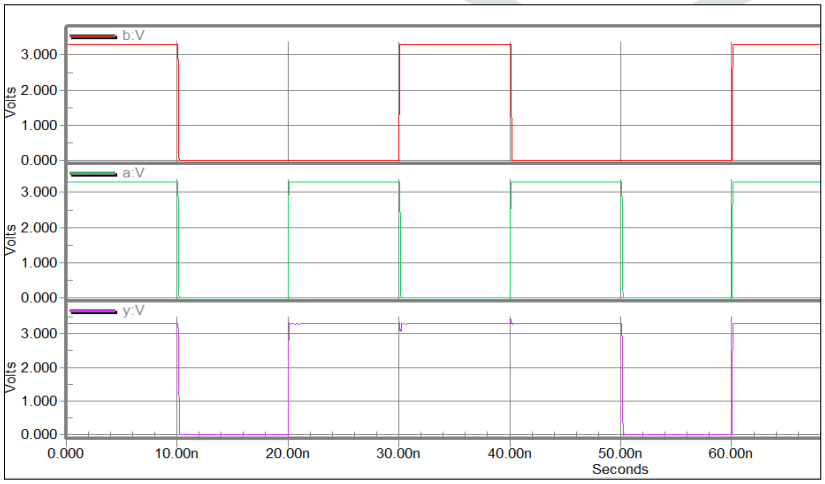


Fig16:- Output Waveform of OR Gate using FSGDI

- For inputs a= 1 & b=1, o/p y=1 obtained b/w 0ns- 10ns up to max. of 3.3 V
- For inputs a= 0 & b=1, again o/p obtain is y= 1 b/w 10ns-20ns which verifies truth table

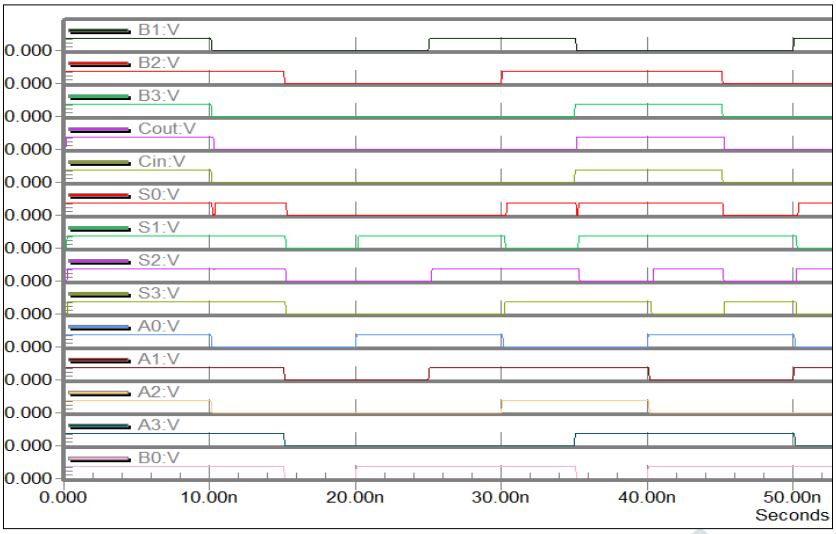


Fig20:-Output Waveform of Brent Kung Cell

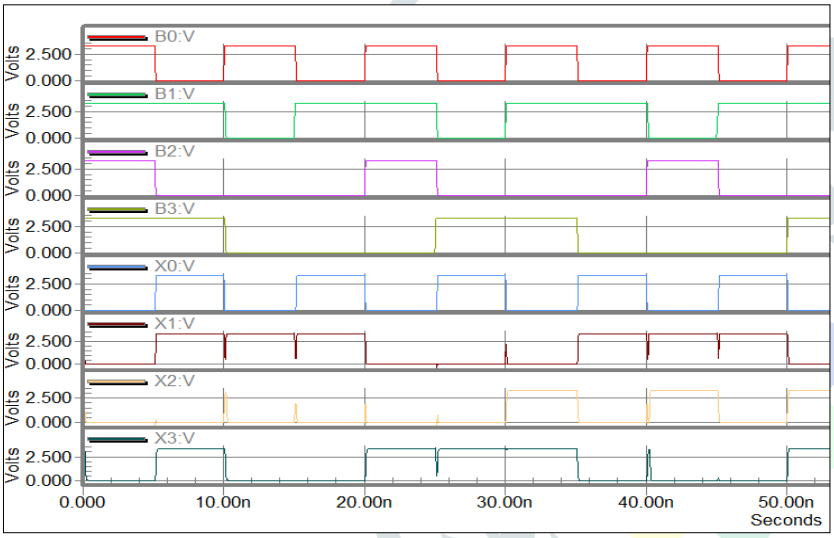


Fig21:- Output Waveform of Binary to Excess 1 Converter

- For input values B0= 1, B1= 0, B2 = 0, B3 = 0, the output X0= 0, X1= 1, X2= 0, X3= 0 seen & verified on time scale at 10ns.
- For input values B0= 1, B1= 1, B2= 1, B3=0, the output obtained X0 = 0, X1 = 0, X2 = 0 X3 = 1 seen & verified on time scale at 20ns.

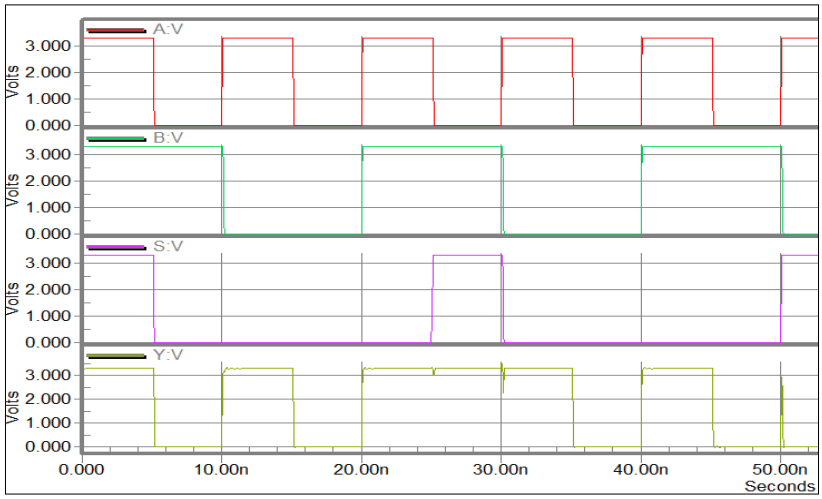


Fig22:- Output Waveform of 2:1 Multiplexer

- For inputs A=0, B=1& S=0, the o/p y=0 on time scale b/w 5ns-10ns, hence verify the truth table.
- For inputs A=1,B=1 & S=1, the o/p obtained y=1 on time scale b/w 0ns-5ns & hence verified.

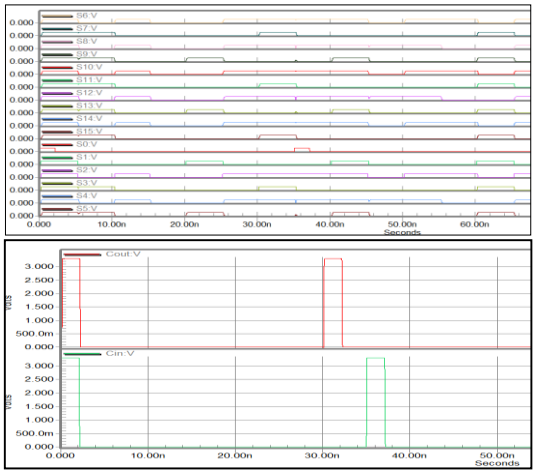


Fig23:- Output waveform of 32-bit Carry Select Adder

- The o/p Sum(S0-S31) of 32-bit carry select adder is checked & verified at time scale of 60ns for input values of A(A0-A31) , B(B0-B31), cout=1 & cin = 0.

5. Graphical Comparisons in terms of Delay & Power Consumption.

5.1 Delay Comparison:-

Firstly, Average Delay for AND, OR & XOR Gates were calculated using Trans Delay Measure of Spice Command available as tools in S- Edit of Tanner EDA Tools in 15.1 & 180nm technology.

Further, Avg. delays of these three logic gates are than compared with the delays obtained for these gates designed using various other logics as shown below: -

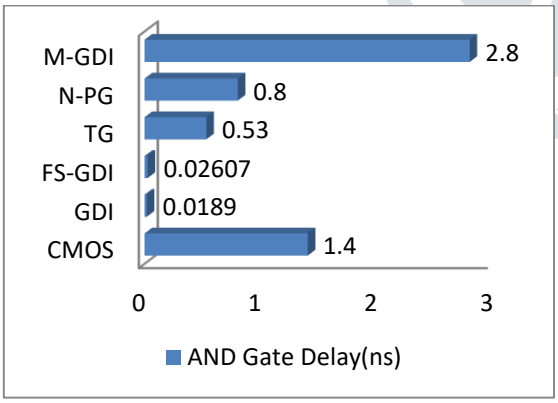


Fig 24: - AND Gate Delay

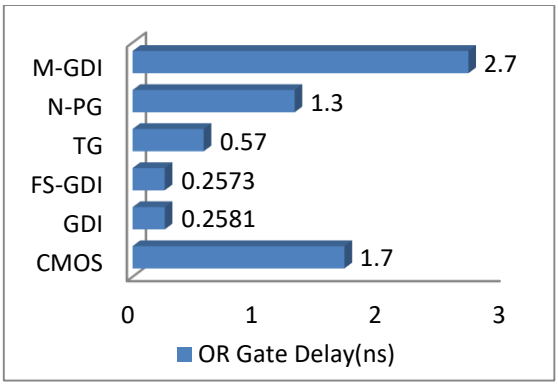


Fig 25: - OR Gate Delay

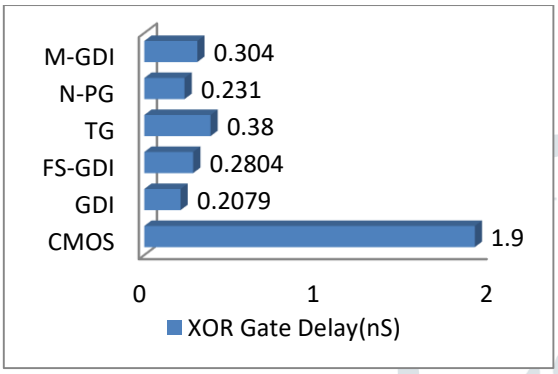


Fig 26: - XOR Gate Delay

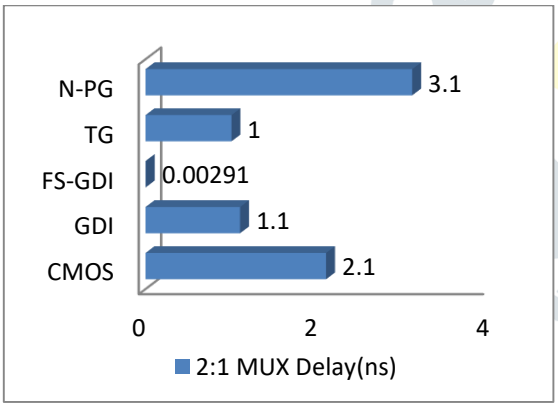


Fig 27: - 2:1 MUX Delay

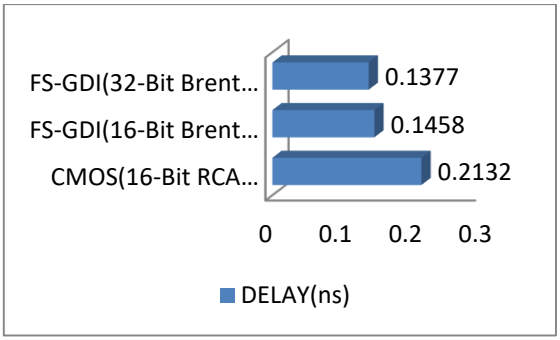


Fig 28: - 32-bit CSLA Delay

5.1 Power Consumption Comparison:-

Power is calculated using ".POWER ''formula by writing in T- Spice. The power of these gates are than compared with the powers of the Gates designed in other logics are shown below:-

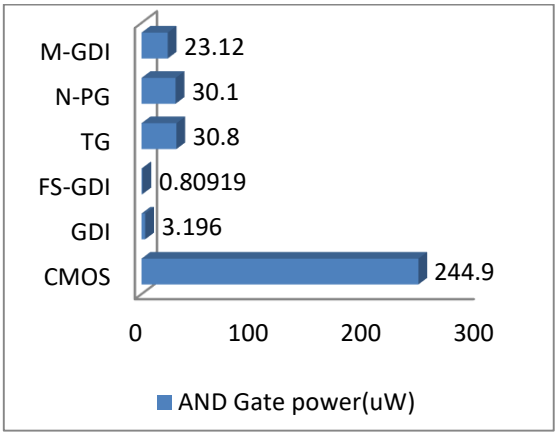


Fig 29: - AND Gate Power

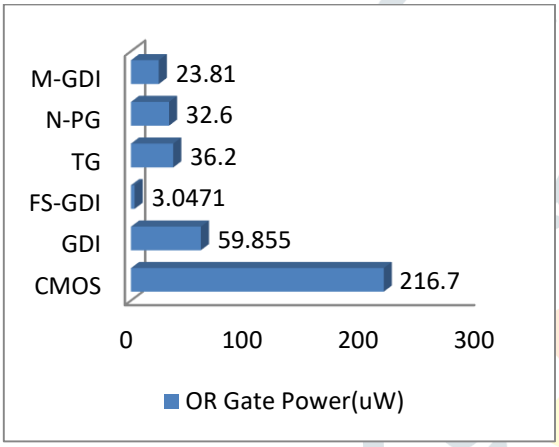


Fig 30:- OR Gate Power

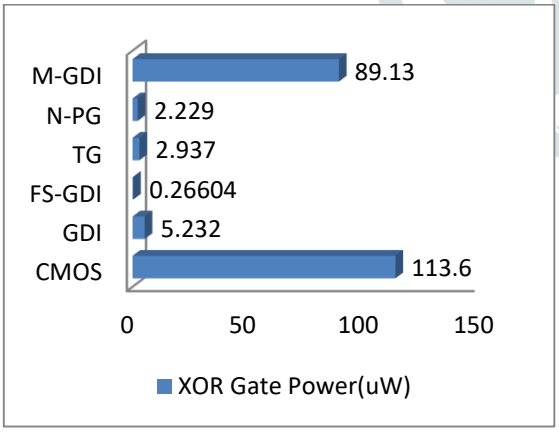
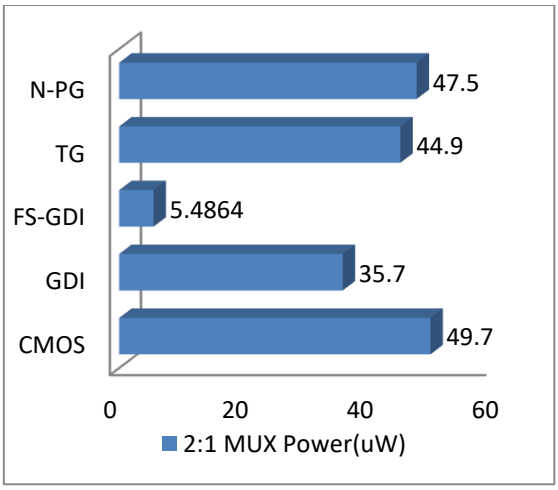


Fig 31: - XOR Gate Power



`Fig 32: - 2:1 MUX Power

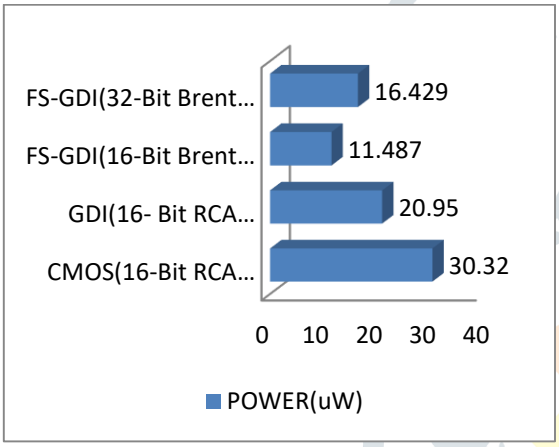


Fig 33: - 32- bit CSLA Power

6.Conclusion:-

In this design of 32 bit Carry Select Adder with a special Brent Kung Adder developed using Full Swing Gate Diffusion Technique (GDI). The proposed design is simulated using Tanner EDA Tool 15.1 and designed in 180nm technology, the obtained results and comparison gave fantastic improvement in delay and Power consumption over earlier 32-bit CSLA.

In FSGDI based 32-bit CSLA has a propagation delay of around 0.1377nsec which is quite less compare to previous designed techniques .Likewise, Power consumed by 32-bit CSLA designed using FS GDI is only 16.429uW.

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