OPTIMIAL DECODER ARCHITECTURE FOR POLAR CODES USING BELIEF PROPAGATION TECHNIQUE

[1] K.Hanisha, [2]CH.V.M.S.N.Pavan kumar
[1]Student of M.Tech., [2]Associate Professor
[1]Department of ECE, Research Centre for VLSI and Embedded Systems,
[1]Sree Vidyanikethan Engineering College,
Tirupati, India

Abstract : Polar codes are presenting high impact in coding theory, since they are giving channel capacity in memory less channels likely binary input memory less channel and arbitrary discrete input memory less channel. We can find its application in wireless communications like speech communications etc. In this paper, we proposed approximate belief propagation (BP) decoder for polar code for the first time with efficiency in delay. Successive Cancellation Decoding (SCD), as of having serial nature depicts latency problem even though computation complexity is less compared with Belief Propagation Decoder (BPD). BPD computation performs with parallel nature with low latency. Adder is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. as technology improves many research work have been developing among those some research adders such as kogge stone adder and Brent kung adder. By introducing the approximate computation schemes by using above mention adders, we observed delay reduction and the comparatively hardware consumption of the conventional BP decoders. However area and speed are two conflicting constraints which present efficiency in architecture.

IndexTerms **- Polar code, belief Propagation, Approximation computation, hardware consumption**

I.INTRODUCTION

Unusual capacity-advance towards codes, such as turbo codes [1] and low-density parity-check (ldpc) codes [2], are designed and used for wireless communication and data storage etc, for gaining high data rate. Recently, the first provable capacity-achieving codes, called polar codes, were invented by arikan [3]. As the first invention in codes which achieved channel capacity and hardware efficient architectures, polar codes gained lots of popularity. Polar codes comprise to attain the capacity for binary-input symmetric memory less channels [3] as well as discrete and continuous memory less channels [4]. Method for constructing or designing this polar codes have been implemented which gives efficient encoding and decoding process with complexity *o (n* log *n),* n gives length or width of code. Variant techniques are given for decoding process of polar codes [5]–[20]. The coding theory is impacted highly based on two algorithms named SCD and BPD. As SCD works on serial process, as of it providing less computation process it also having low latency. As we find the latency problem in sc decoders, different methods are proposed to overcome the latency problem [9]–[10]. Error correcting methods for polar codes have been proposed namely list decoding and stack decoding, of SCD with short code lengths [11]–[14].

The random noisy channel theorem which shows being of capacity- gaining negligence of sequence called Shannon's proof for coding theory. unambiguous probability capacitance gaining can be achieved for code sequences with low encoding and decoding complexities which maintains a side Channel polarization for coding technique it is given for binary input discrete memory less channel [13]. Polar codes are competent of getting the 'symmetric capacity' of any binary input channel, by means of encoding and decoding of code with less complexity. The recently invented polar codes are provably capacity attaining, and their regular structure promises energy-efficient code designs. Adders having impacted role in electronic applications, which can also be used in multipliers i.e. in arithmetic applications. Along with multipliers DSP applications like FFT, FIR and IIR algorithms also needed adders.

This says that adders impact more for maximum digital circuits. So speed of operation or hardware requirement comes in consideration while giving betterment in efficiency [5]-[6]. Since a single adder cannot exhibit all the above mentioned characteristics, certain adders usurp over other based on the requirement of user. In order to make the selection of adders appropriate and not a laborious one, the comparison among various four bit adders has been done extensively. Although adders play a crucial role, based on speed, power dissipation and area consumption, the choice of adder changes from one programe to other. Low power consumption, low power dissipation, low area i.e., less number of transistors, High speed.

This paper presents, architectural change of BP decoding with approximation by changing different adders in place of addition operation of BP decoding, and proposed an efficient approximate BP de- coder. The comparison of area, delay parameters of this architecture are presented in results section.

II. RELATED WORK

BP Decoding Computation

Channel polarization is main achievement in communications, this polarization can be achieved by polar codes which are trendy concept to. To perform this individual components are dividing to two and the mutual data is passed either 0 or 1. Here we can observe that some channels are noise free while other are noisy. Apart from decoding by SCD or its variants, one technique is polar codes can be decoded either using BP computation over the factor graph [15]. This graph is representated as (n,k) polar code where n is 2m ,here m is the identification of m stage. which consists of *n. (m + 1)* nodes. The factor graph contains two types of nodes: F and G.? Directed towards left to right and right to left. These nodes can be viewed as column and row indexes as I and j. For a BP decoder, scheduling refers to the method of information dissemination and updating the data between the two ends of factor graph. There is considerable effect of speed in BP decoder factor graph. The major nodes F node and G node architectures are modified for better efficiency.

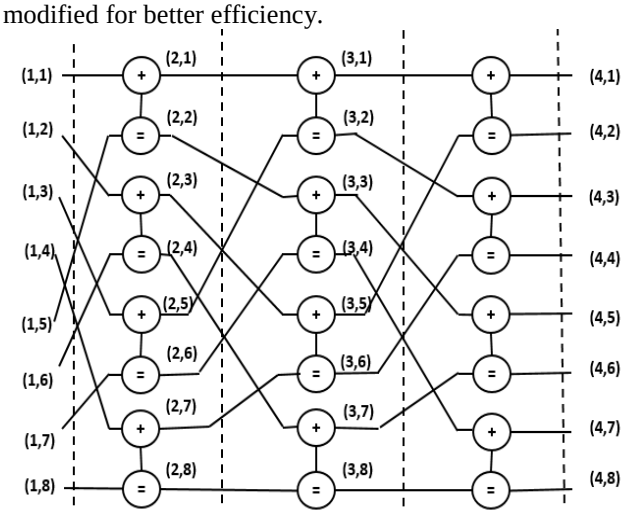


Fig. 1. Factor graph of BP decoding with $N = 8$.

Conventional Architecture for G Node

G node is used for magnitude comparison by giving two binary inputs to comparator which compares LSB to MSB of binary data. For this comparison approximation is given for better efficiency. To get this approximation in comparison total bits are not compared they are spitted to two n-k bits and n bits. N-k bits are compared and remaining n bits are unnoticed. The below figure 2 gives the example with k as 2.

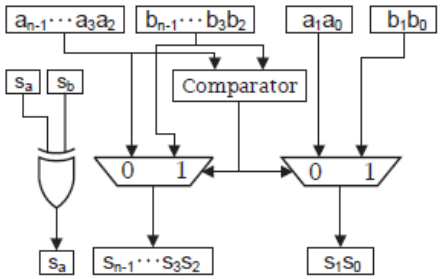


Fig. 2. Existing Approximate architecture for G node.

Here we follow the process as s[n-1:k] bits are selected based on a[n-1:k],and b[n-1:k] bits. If a[n-1:k] is greater than b[n-1:k], then s is assigned by b values. In other case s is a. Here we can easily achieve the approximation as the remaining bit's ignored since they may produce wrong result. The below equations gives the probability for getting a equal to b and a less than b.

$$\begin{cases} P(a_{[n-1:k]} = b_{[n-1:k]}) = (\frac{1}{2})^{n-k}, \\ P(a_{[k-1:0]} < b_{[k-1:0]}) = \frac{2^k-1}{2^{n+1}}. \end{cases}$$

So the error rate for this is given as

$$ER = (\frac{1}{2})^{n-k} \cdot \frac{2^k-1}{2^{k+1}} = \frac{2^k-1}{2^{k+1}}.$$

for a specific *n*, a larger *k* will cause greater performance loss and less hardware consumption. We use half-rate polar codes with code length $N = 64$ for simulation. The quantization scheme is (1-5-3), including 1 sign bit, 5 integer bits, and 3 fractional bits.

Conventional Architecture for F Node

To get updated values of F node firstly the data bits are complemented before they given as input to adders and multipliers. With this architecture comparator and adder one circuit is given to this which gives high critical path delay and hardware complexity high. Fig 3 gives the efficient hardware architecture for F node. Sa, Sb, and Sc represents the sign bits of inputs a and b with output S. The magnitudes are represented by Ma, Mb and Ms. Here subtraction is done directly. So that only one data node conversion sufficient for F node. A parallel computation is performed for *Ma +Mb* and *Ma –Mb* along with the magnitude of the final result *s* is chosen from these two values.

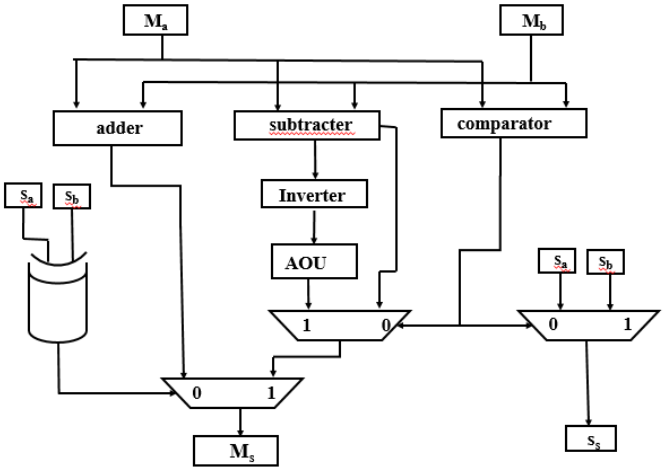


Fig. 3. Existing approximate architecture for F node

Here approximation method is given to Add one circuit (AOU), because this gives impact towards the final output of F-node. The approximate Add one unit is given below

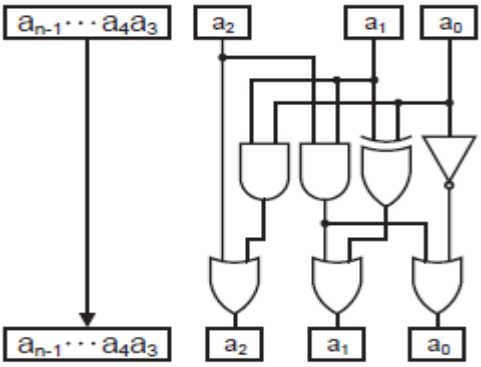


Fig. 4. Existing approximate AOU with $m = 3$.

III. PROPOSED WORK

The main modules of polar codes are G node and F node as illustrated in previous work. The conventional G node and F node are area efficient. The same architectures are considered and are further reduced in terms of area and delay for making more efficient. For Such reduction we are changing the architectural designs of G node and F node by replacing adder in F node to Brent Kung adder or kogge stone adder. First let we discuss about this adders. Computation is the major thin followed in arithmetic operations. These arithmetical calculations cover addition, subtraction, multiplication, division etc. Among this we are discussing adders.

Adders perform addition operation. In digital circuit theory this addition can be performed by using two basic adders called half adder and full adder. This Half adder is used for 2 bits and full adders are used for 3 bits. Now if we want to add a set of numbers different adders are used called Binary parallel adder, carry look ahead adders, carry save adders etc. here high propagation delay problem is reaching as to pass the carry to different stages. Therefore, in current technology, Parallel Prefix Adders (PPA) is the paramount amongst the obtainable adders. Parallel prefix adder, itself describes that it is an outcome of the parallel execution of the operation depending on the initial inputs (prefix). Practically this is obtained by segmenting the process to two parts and performs computed parallel [6]-[8]. This adders gives faster execution.

Brent Kung adder

Brent Kung adder performs the computation in 3 stages for producing sum result. The initial stage consists of a Pre-processing unit.

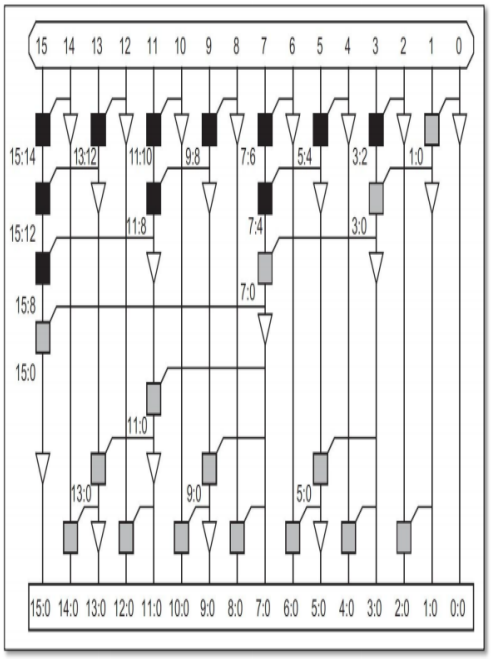


Fig 5. Brent Kung adder

Using inputs propagate and generate signal are generated. Carry generation happens in intermediate stage, here outputs of pre processing signals are used for carry generation by assigning them as inputs to second stage. The last stage is post-processing where the final Result is obtained using the Carry signal from the intermediate stage and propagates a signal from the initial stage.

Kogge stone adder

Peter M. Kogge and Harold S. Stone created this The Kogge-Stone adder concept which published in 1973 in a seminal paper titled. This adder performs with high speed. Three blocks namely pre processing, carry generation and post processing develops this adder architecture. In KSA, carries are computed fast by computing them in parallel at the cost of increased area.

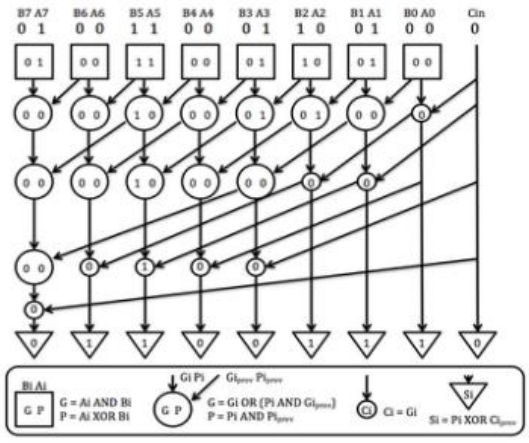


Fig 6. Kogge stone adder

By placing the above discussed adders the modified architectures of G node and F node of BP decoder are as follows

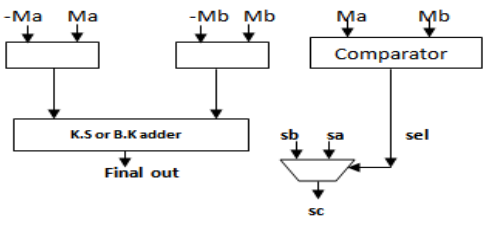


Fig 7. Proposed architecture of F node

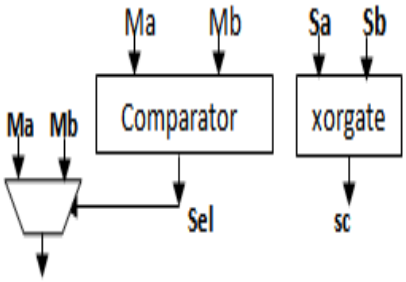


Fig 8. Proposed architecture of G node

The proposed architecture of G node and f node of Bp decoder are efficient in terms of area and delay. By using the different parallel prefix adders in architecture the parameters vary by giving efficient. Let have short discussion in results and comparison about the parameter variations.

IV. RESULTS AND DISCUSSIONS

To present the advantage of proposed architecture of BP decoder is demonstrated as, the speed can be increased by using this adders Kg adder and Brent kung adder compared to existing one. If we want minimal speed is minimal area we can use BG adder based BP decoder. If we want High speed with minimal area we can use KG adder. The results, schematic figures and comparison table are presented below. Block Figure for KG adder based BP decoder, the block diagrams illustrates the number of inputs and outputs used for our designs as like a chip with input and output pins.

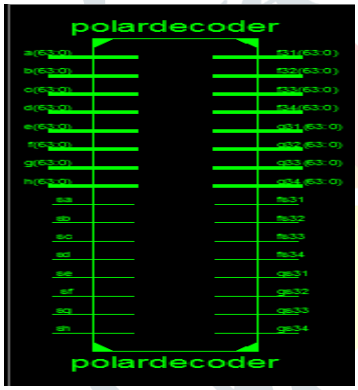


Fig 9. Block Diagram of KG adder based BP decoder

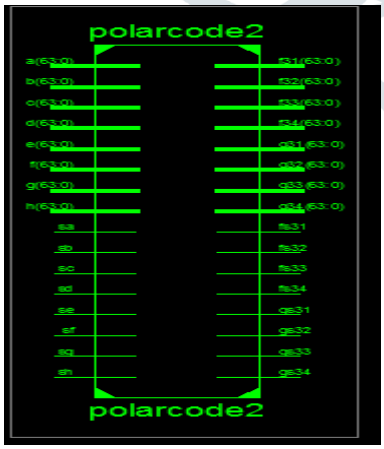
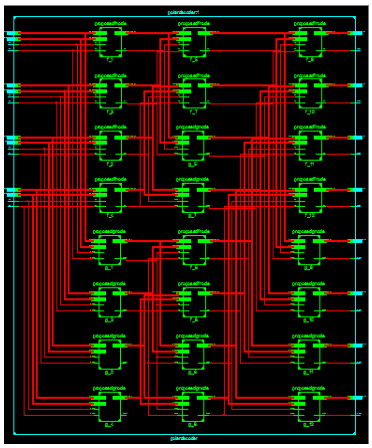
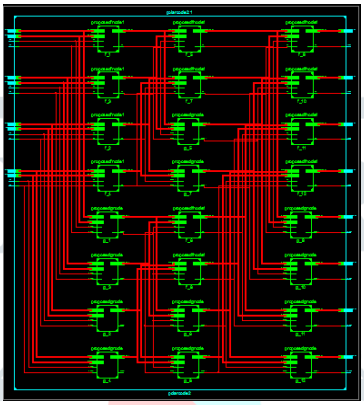


Fig 9. Block Diagram of BK adder based BP decoder

The schematic figure of this block figures are presented below the schematic figure gives the internal architecture of the block figures.



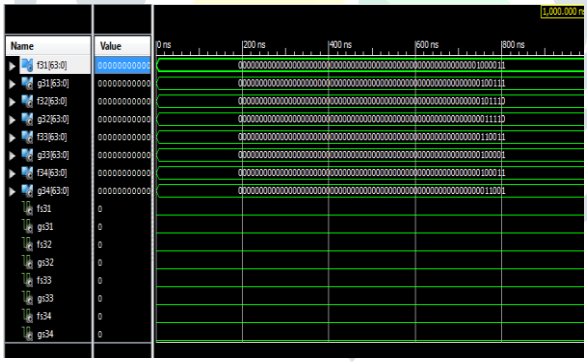
10.a)



10 b.)

Fig 10 a. Kg adder based decoder, b. Bk adder based decoder

The output waveforms of this designs are



The comparison table is presented below
This comparison table gives the comparison between the area and delay representation which gives the efficiency of the designs

Table 1. Parameters comparison table

designs / Parameters	Polar decoder existing	Polar decoder Proposed(KG adder)	Polar decoder Proposed(BG adder)
Area	4825 (LUT's)	9369 (LUT's)	7189 (LUT's)
Delay	143ns	65ns	120ns

V. CONCLUSION

The BP decoders are used where high data reduction is needed in like during communication etc. G node and F node are the major blocks used for designing the BP decoder. Such nodes are with approximation are modified in this paper. A new architecture are designed based on the usage of parallel prefix adders like Brent Kung adder or kogge stone adder which gives more speed efficient designed along with minimal area efficient too.

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