

Design of Energy Efficient Level Shifter Using Dual Current Mirror in 45nm CMOS Technology

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Abstract : This paper proposes a design of energy efficient level shifter using dual current mirror in 45nm CMOS technology. The proposed level shifter can convert low logic levels, even subthreshold voltage levels to higher acceptable levels. The proposed dual current mirror structure consisting of a modified wilson current mirror based virtual current mirror section and cascoded current mirror based auxiliary current mirror section. The pre-layout and post-layout (DRC and LVS) simulations are done using cadence® EDA tool. From the transient analysis, it is evident that the proposed design achieves 0.3V to 1.1V conversion. It exhibits an average propagation delay of 34.6 pS and a total power dissipation of 1.4 pW, for a 300mV, 50MHz input signal. The total area of the proposed design is 49.2 μm^2 . The proposed energy efficient level shifter using dual current mirror exhibits an improvement of power and delay compared to conventional level shifter designs.

IndexTerms – Level shifter, Dual current mirror, Cadence, Subthreshold to above threshold level conversion.

I. INTRODUCTION

The dynamic power dissipation of a circuit is directly proportional to the supply voltage in CMOS circuits^[1]. That means, if the supply voltage is higher, the power dissipation is also higher. Thus the dynamic power dissipation of a circuit can be reduced through voltage scaling technique. This gained lot of popularity and the electronic industry started using multiple supply voltage (MSV) technique for the design of advanced system on chips (SoC). In the early days MSV technique is implemented by partitioning the SoC designs in to separate voltage islands and separate power supply is provided for each voltage island. Instead of using separate power supply, the industry currently uses level shifters for optimizing the power dissipation, area and propagation delay. Almost all of the systems in today's VLSI world is based on system on chip technology.

In SoC designs, the entire system will be fabricated on a single chip. The SoC design contains both digital blocks and analog blocks, all of them are fabricated on a single chip. The generalized illustration of SoC design is given in figure 1.1. The blocks inside an SoC chip always works on different voltage levels. Thus the major concern is that the output from a low voltage block inside an SoC should drive the next high voltage block. Hence SoC designs requires an interface (level shifters) between different blocks. There comes the use of Level shifters. Several level shifter designs were proposed recently. The generalized block diagram for understanding the application of level shifters inside an SoC is given in figure 1.2.

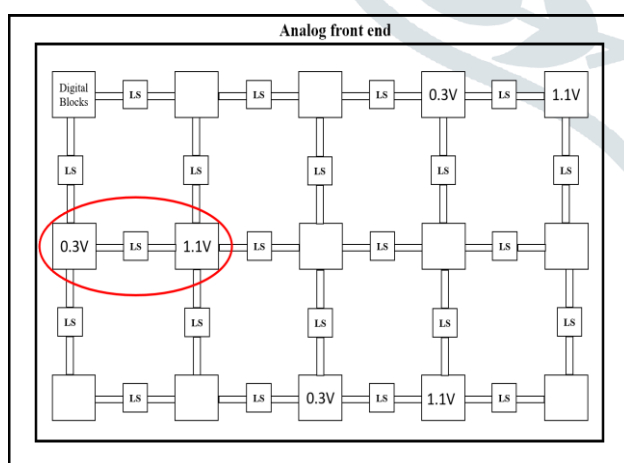


Figure 1.1 Generalised illustration of SoC design

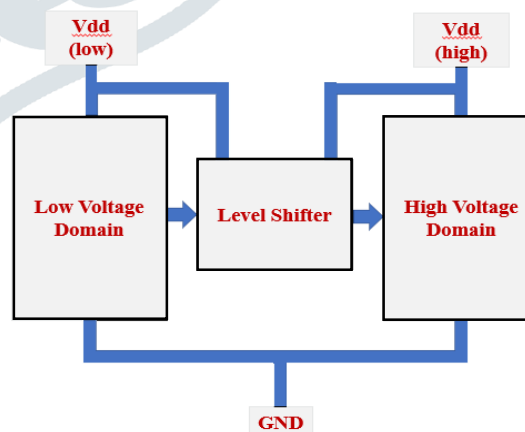


Figure 1.2 Generalised block diagram of a level shifter

Wilson current mirror based level shifter concept is the latest and dual current mirror based level shifter concept is under research. This paper focus on dual current mirror concept. The pull-up section of dual current mirror concept consists of a primary current mirroring circuit and a secondary current mirroring circuit. Currently, this design is widely preferred and it doesn't mean that other designs like DCVS based level shifters, current mirror based level shifters and wilson current mirror based level shifters are not using in modern SoC designs. Some advanced designs of DCVS based level shifters and current mirror based level shifters are also under research.

II. LITERATURE REVIEW

In this section topics related to level shifter designs are included. These provide a sampling of problems appropriate for the application of energy efficient level shifter using dual current mirror. The references are summarized below.

The different level shifter designs include differential cascode voltage switch (DCVS) based, current mirror based and wilson current mirror based. The six-transistor DCVS based level shifter^[2] is the first design to be implemented on an SoC. The circuit diagram for six-transistor DCVS based level shifter is given in figure 1.3. The major drawback of this design is the strong contention current between the pull-up and pull-down networks. To overcome this problem the researchers propose current mirror based level shifter^[3] design, it is given in figure 1.4. In current mirror based level shifter the standby current is extremely high.

To eliminate the extreme high standby current, a feedback transistor is added to current mirror based level shifter, this is wilson current mirror based level shifter^[4] design. The circuit diagram for wilson current mirror based level shifter is given in figure 1.5. When the static current cut off, the voltage swing at the feedback node is reduced. This creates a floating voltage on the feedback node, it causes large static current in the output inverter. To eradicate all these problems an energy efficient level shifter using dual current mirror is proposed in this paper.

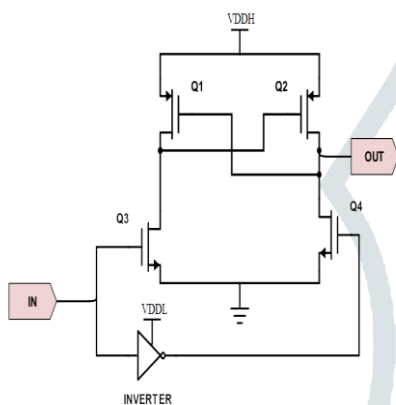


Figure 1.3 Six-transistor DCVS based level shifter

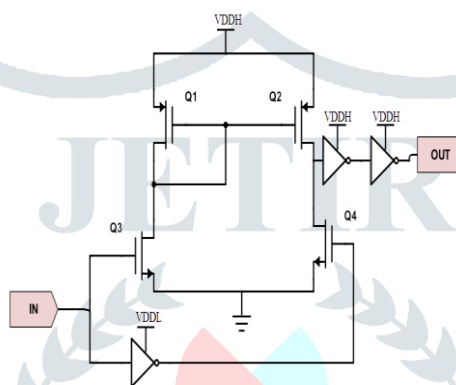


Figure 1.4 Current mirror based level shifter

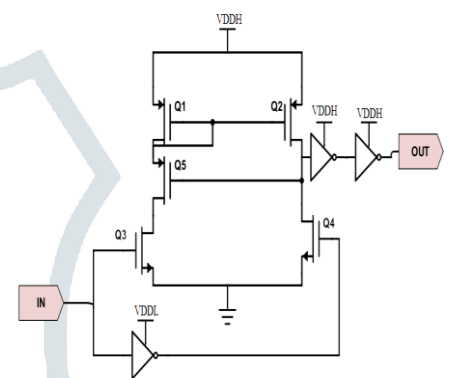


Figure 1.5 Wilson current mirror based level shifter

III. DESIGN OVERVIEW

The energy efficient level shifter using dual current mirror composed of four sections. A pull-up network using two current mirrors, a pull-down network using NMOS logic, input and output sections using simple CMOS inverter. The two current mirror circuits used in pull-up network are a virtual current mirror and an auxiliary current mirror. The block diagram for energy efficient level shifter using dual current mirror is given in figure 1.6.

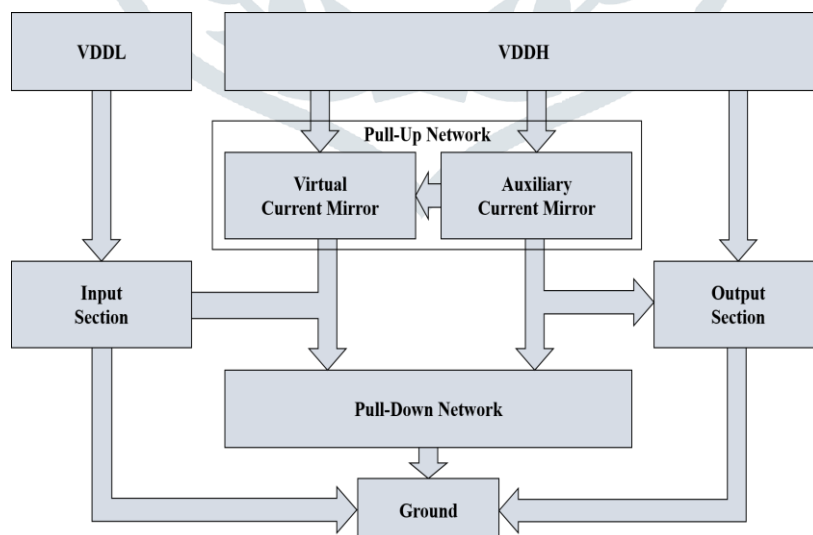


Figure 1.6 Energy efficient level shifter using dual current mirror

The virtual current mirror is built using a modified wilson current mirror and auxiliary current mirror is built using cascoded current mirror. The energy efficient level shifter using dual current mirror also use input signal and it's complimentary signal, and a dual supply system (VDDH and VDDL) ensures the proper working of the circuit. The circuit diagram of energy efficient level shifter using dual current mirror is given in figure 1.7.

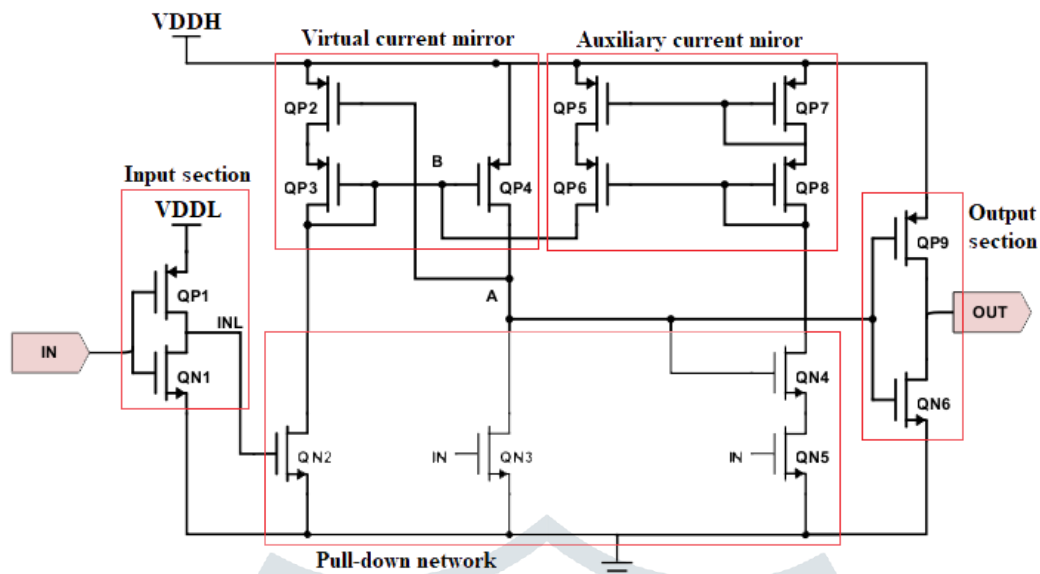


Figure 1.7 Circuit diagram of energy efficient level shifter using dual current mirror

As the name indicates the virtual current mirror acts as a virtual supply in pull-up network. The virtual current mirror section composed of a modified wilson current mirror. Literature review points that the major drawback of wilson current mirror based level shifter is the floating voltage or voltage drop at the feedback node. The revised PMOS transistor feedback control used in virtual current mirror section can successfully eliminate the voltage drop issue and reduce the static power significantly. Circuit diagram for the modified wilson current mirror is given in figure 1.8.

The auxiliary current mirror section is actually designed to assist the discharging process and to ensures the correctness and robustness of the level shifter circuit. The auxiliary current mirror is constructed using a cascoded current mirror circuit. Wilson current mirror uses a negative feedback system, but in the case of cascoded current mirror a feedback system is not present. This makes the discharging process faster and smooth. Cascode current mirror can suppress the effect of channel length modulation and increases the output resistance of a current source. A PMOS cascode current mirror is used here and the current flows from input node to outer node. Circuit diagram for cascode current mirror is given in figure 1.9.

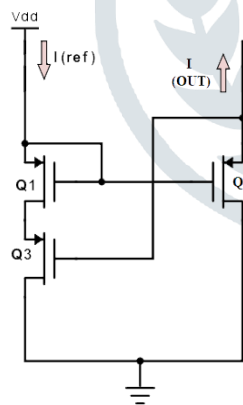


Figure 1.8 Virtual current mirror

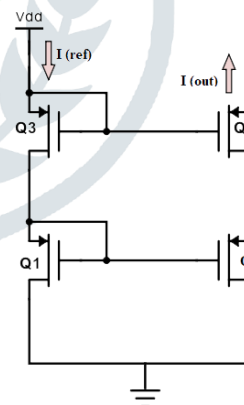


Figure 1.9 Auxiliary current mirror

A. High-to-low Transition

The figure 1.10 explains a high-to-low transition. When the input signal (IN) goes from high-to-low, the voltage level at node A stays at the ground level at first. Transistor QN3 is turned OFF by IN, while the differential signal INL provided by input section inverter turns ON the transistor QN2. Since the voltage at node A resides at '0', the transistor QP2 is in strong inversion region. As a result, the internal node C remains at VDDH and can be seen as a virtual supply voltage, which forms the virtual current mirror between transistor QP3 and transistor QP4. The source current passing through transistor QP3 and transistor QN2 is intended to provide mirror current through transistor QP4 to charge node A. As the voltage at node A increases, the transistor QP2 gradually enters into the weak inversion region, which means that the voltage at node C starts to decrease as along with the voltage at node B. On the other hand, the voltage drop at node B will continue to maintain sufficient pull-up current to charge node A. In the end, the voltage at node A reaches VDDH, while the voltage at node B can be discharged to ground level. Since the voltage at node A is VDDH, the transistor QP2 can be turned OFF and the standby current is eliminated.

B. Low-to-high Transition

The figure 1.11 explains a low-to-high transition. A low-to-high transition occurs at IN with initialized low voltage at node B, whereas node A remains at VDDH. The differential INL is '0', which turns OFF the transistor QN2. During this state, the IN is charged to the '0', and attempts to discharge node A through weak inversion device transistor QN3. However, due to the ground voltage level at node B, the transistor QP4 resides in the strong inversion region and a pull-up current flows through transistor QP4 to charge node A. The contention current in the pull-up network could possibly maintain node A at '1' and compromise the correctness and robustness of the proposed design. Under this circumstance, the auxiliary current mirror is expected to work. Because the voltage at node A and IN remains in '1', the source current path from transistors QP7, QP8, QN4 and QN5 in auxiliary current mirror is turned ON, allowing the mirror current through transistor QP6 to charge node B. Since the INL is '0', the mirror current through transistor QP6 could charge node B rapidly. After that, transistor QP4 is turned OFF, and transistor QN3 could discharge node A to ground level so that the output reaches VDDH or '1'.

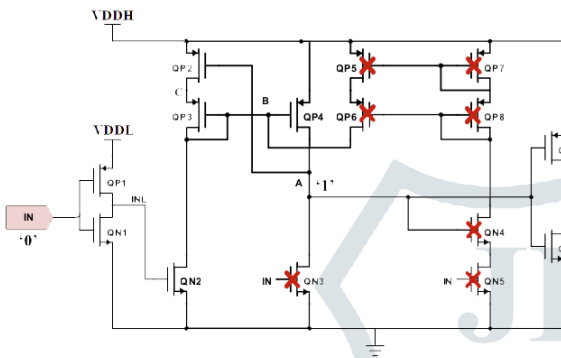


Figure 1.10 High-to-low transition diagram

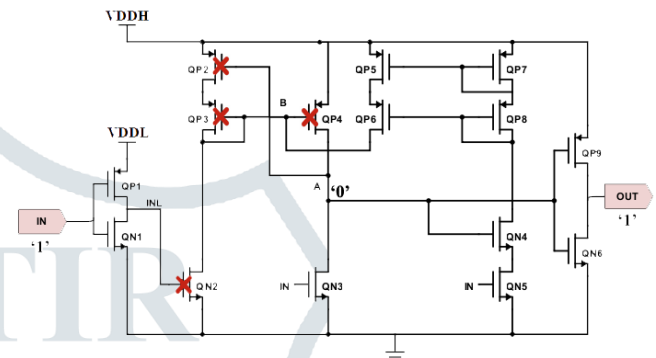


Figure 1.11 Low-to-high transition diagram

Thus the design of energy efficient level shifter using dual current mirror is completed. Next step is the design optimization. In this paper, the power dissipation of energy efficient level shifter using dual current mirror is optimized. There are many techniques available to optimize power dissipation of VLSI circuits, but the most suitable techniques for each circuit will be different. In this thesis work, mainly three power reduction techniques are utilised, while designing an efficient dual current mirror based level shifter. The power reduction techniques used are listed below:

- a) Transistor stacking technique is used at the input section (transistor QN3) to reduce static power dissipation.
- b) Added a single sink PMOS transistor (QP9) between virtual current mirror section and pull-down network to avoid the direct path between supply and ground.
- c) Transistor sleep approach (transistor QN1) is used to reduce the total power dissipation.

The circuit diagram for optimized energy efficient level shifter using dual current mirror is given in figure 1.12. The schematic diagram for the same is given in figure 1.13.

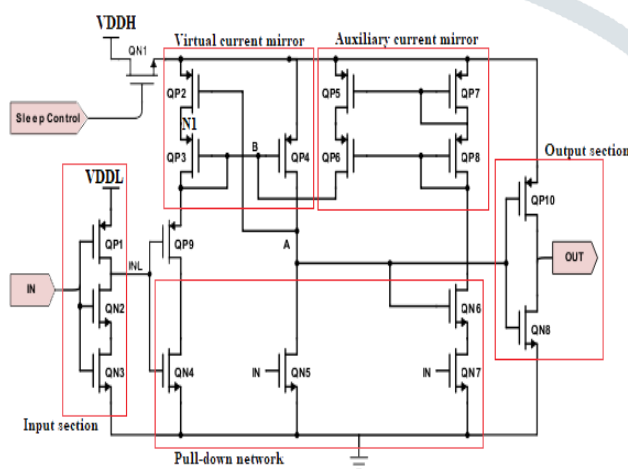


Figure 1.12 Optimized circuit diagram of energy efficient level shifter using dual current mirror

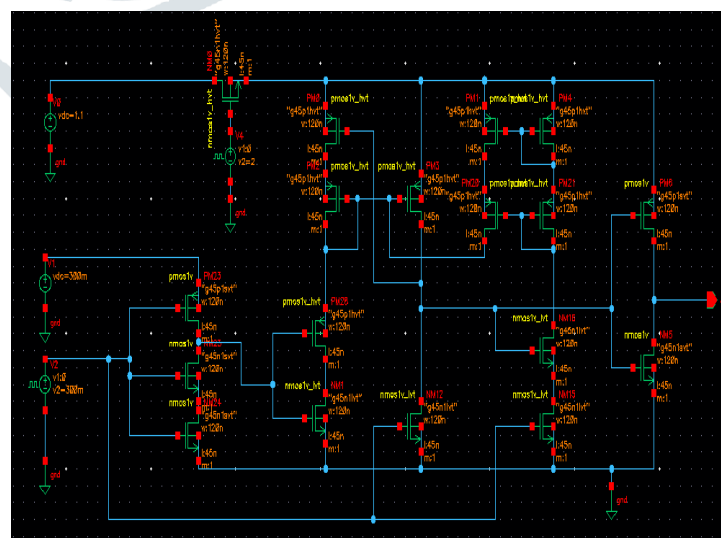


Figure 1.13 Schematic diagram of optimized energy efficient level shifter using dual current mirror

IV. SIMULATION RESULTS

The transient response of energy efficient level shifter using dual current mirror in 45nm CMOS technology is given in figure 1.14. It is evident that the voltage shifting level of optimized design is 0.3V to 1.1V. The DC response for the energy efficient level shifter using dual current mirror in 45nm CMOS technology after optimization is given in figure 1.15.

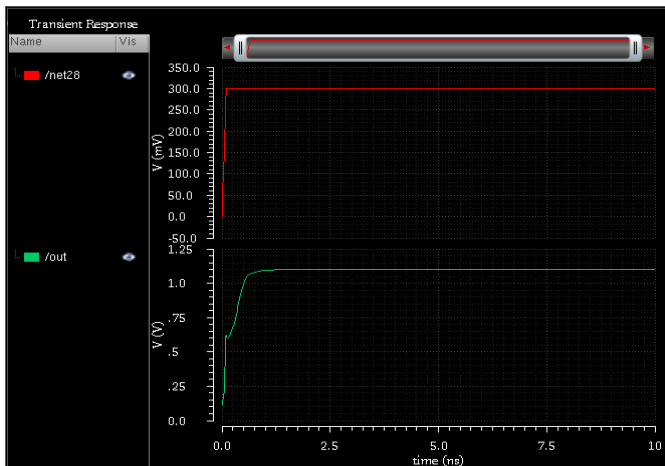


Figure 1.14 Transient response of optimized energy efficient level shifter using dual current mirror

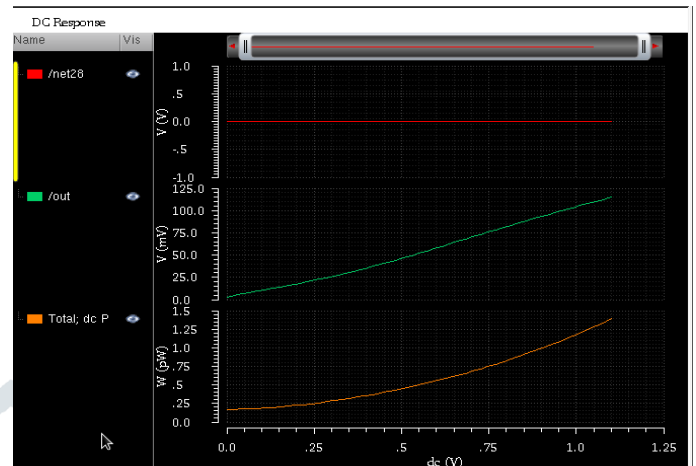


Figure 1.15 DC response of optimized energy efficient level shifter using dual current mirror

The power dissipation and propagation delay of energy efficient level shifter using dual current mirror in 45nm CMOS technology after optimization obtained during the analysis is 1.4 pW and 34.6 pS respectively, given in figure 1.16. and 1.17.

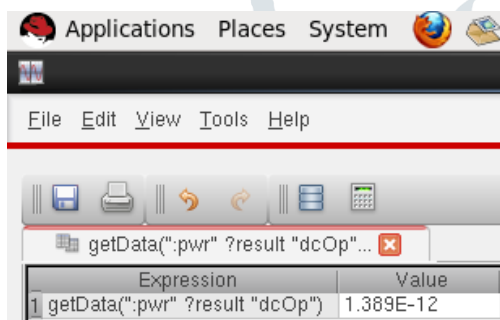


Figure 1.16 Power dissipation of optimized energy efficient level shifter using dual current mirror

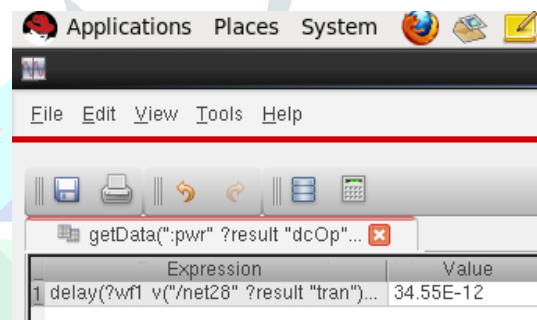


Figure 1.17 Delay of optimized energy efficient level shifter using dual current mirror

Thus the pre-layout simulations are completed and next step is the post-layout simulations. The layout of energy efficient level shifter using dual current mirror is given in figure 1.18. The design rule check and layout versus schematic checks also completed.

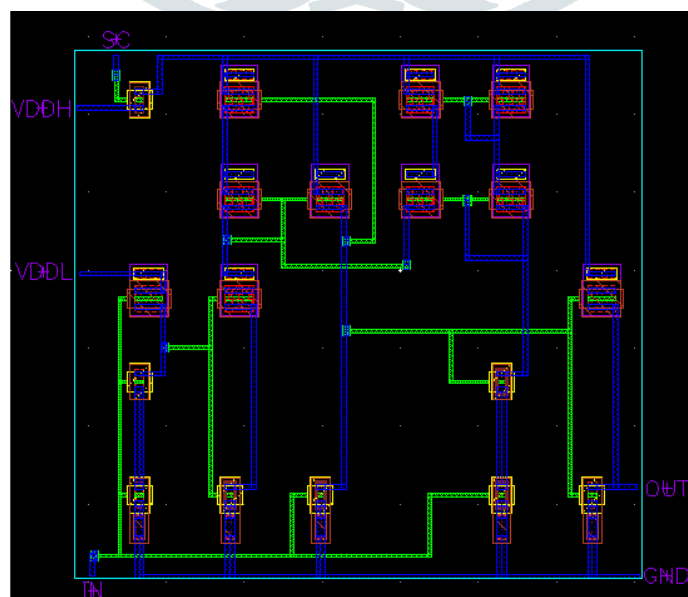


Figure 1.18 Layout of energy efficient level shifter using dual current mirror

V. RESULT ANALYSIS

| Reference | Technology | Design | Voltage Shifting Level | Power Dissipation | Total Delay |
|-----------------|-------------|---|------------------------|-------------------|----------------|
| [2] | 45nm | Six-transistor DCVS level shifter | 0.3V to 0.7V | 545.8 pW | 23.8 pS |
| [3] | 45nm | Current mirror based level shifter | 0.3V to 1.1V | 4.4 nW | 165 pS |
| [4] | 45nm | Wilson current mirror based level shifter | 0.3V to 1.1V | 50.2 pW | 265 pS |
| Proposed | 45nm | Energy efficient level shifter using dual current mirror | 0.3V to 1.1V | 1.4 pW | 34.6 pS |

VI. CONCLUSION

The design of energy efficient and wide range voltage level shifter using dual current mirror concept in 45nm CMOS technology is successfully completed. From transient analysis, it is observed that the energy efficient level shifter using dual current mirror in 45nm CMOS technology can shift voltages from 0.3V to 1.1V. The calculated power dissipation and propagation delay for the energy efficient level shifter using dual current mirror in 45nm CMOS technology is 1.4 pW and 34.6 pS respectively. It is evident that the energy efficient level shifter using dual current mirror in 45nm CMOS technology has a wide voltage conversion range, low power dissipation and smaller propagation delay comparing to the conventional level shifter designs.

The layout design for the energy efficient level shifter using dual current mirror in 45nm CMOS technology in 45nm CMOS technology is also completed successfully. The total area of the proposed design is about 49.3 μm^2 . The layout passes the design rule check and layout versus schematic check successfully. Hence, the layout of proposed energy efficient level shifter using dual current mirror design is ready for RC-extraction and fabrication.

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