COST EFFECTIVE DIGITAL CIRCUITS BASED ON CARBON NANOTUBES FOR LOW POWER APPLICATIONS

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Abstract : This paper deals with basic logic circuits using the carbon nanotube field effect transistor (CNTFET). Due to various beneficial properties of carbon nanotubes, that are more efficient than Metal Oxide Field Effect Transistor (MOSFETs). The parameters like power, delay and power delay product of CNTFET are compared with CMOS technologies. Both the simulations are performed in HSPICE software. The CNT based circuits provides more power reduction, delay reduction and PDP reduction when compared with CMOS technologies

IndexTerms **- Carbon nanotube (CNT), CNT field-effect transistor (CNTFET), Metal Oxide Field Effect Transistor (MOSFETs)**

I. INTRODUCTION

As per Moore's law, the number of transistors that are placed in an integrated circuit increases exponentially by almost doubling every two years. Continuously reducing the size of transistor i.e. scaling of MOSFET technology has been carried continuously in order to meet the density and sustain the IC predicted by Moore's law. Since in year 2006, the gate length of a MOSFET device has entered the deep submicron/nano regime at 65-nm feature size. Now a days, 45-nm technology is a reality used, and in the near future 32-nm has been predicted to be the feature size[2]. As the physical gate length is reduced to below 65-nm, several device-level effects, such as short channel effect, large parametric variations and exponential increase in leakage current, have substantially affected the I-V characteristics of traditional MOSFETs.

Due to this results are major concerns for scaling down the feature size of these devices. To meet the challenges of nanoscale CMOS,and achieve similar performance like CMOS, CNTFET is explored. This CNTFET is consist of utilizing new circuit techniques together with alternative technologies to replace conventional silicon and the current MOSFET-based technology[3]

II. CARBON NANOTUBES (CNTS)

Carbon is the 4th most abundant element in the Universe by mass after (Hydrogen Helium and Oxygen) having atomic number of 6. It forms almost 10 million

pure organic compounds with any other element. Carbon Nanotubes are long, thin cylinders of carbon, were discovered in 1991 by SumioIijima of NEC Crop in Tokyo[2]. He proposed the new type of carbon structure which was needle like tubes of diameter varying from 4-30 nm. By survey of applications regarding to the transistors the channel of traditional MOSFET will replace by CNT. These are large that are unique for their size, shape, and remarkable physical properties. Carbon Nanotubes (CNTs) have attraction of researchers worldwide in recent years because of its small dimensions and unique architecture properties. For passive or active elements in post-CMOS Nano- electronics carbon Nanotubes are the best replacement device[3].

III. CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNTFET)

In the era of Nano scale, Carbon Nanotube Field Effect Transistor (CNTFET) is a promising device for future integrated circuits because of its tremendous properties like ballistic electron transport, high carrier mobility. In 1998, the first carbon nanotube field-effect transistors (CNTFETs) were reported. Which is one of the most promising alternatives to the MOSFET is the CNTFET. The most important and significant attribute of CNTFET is its spectacular ability in current carrying or current driving, and experiments have shown that CNTFET is the best for this purpose. CNTFET can operate five times faster than CMOS in the best case without any extra power overhead.[3]

CNFETs are one of the molecular devices that avoid most fundamental silicon transistor restriction and have ballistic or near ballistic transport in their channel. Therefore a semiconductor carbon nanotube seems to be appropriate to be used as the channel of field effect transistors. Applied voltage to the gate can control the electrical conductance of the CNT by changing electron density in the channel.[4] By using appropriate diameter suitable threshold voltage for CNFET can be achieved. The threshold voltage of the CNFET is proportional to the inverse of the diameter of CNT and can be expressed as:

$$V_{th} = \frac{0.42}{D_{CNT}(nm)} \qquad \text{(i)}$$

For a CNT with *(n, m)* as chirality and *a=0.249* as lattice (that is carbon to carbon atom distance) the diameter is :

$$D_{CNT=} \frac{a\sqrt{n^2+mn^2+m^2}}{\pi} \qquad \text{(ii)}$$

As mentioned above, CNTs are used in CNFETs as channel and depending on the connections between source and drain with channel (CNTs) there are two main CNFETs. It works on the principle of direct tunnelling through a Schottky barrier at the source–channel junction; therefore, these transistors are called Schottky Barrier CNFET (SB-CNFET). SB-CNFET shows ambipolar behavior and constrain usage of these transistors in conventional CMOS-like logic families. Schottky barrier restricts the transconductance in the ON state, and thus Ion/Ioff ratio becomes rather low. Second device is MOSFET-like CNFET which is doped in un-gated portions and has similar behaviour to CMOS transistors and it presents unipolar behaviour. The semiconductor junction will eliminate schottky barrier and therefore there is higher ON current unlike SB-CNFETs. Other advantages of MOSFET-like CNFETs are high on- off ratio and their scalability compared to their schottky barrier counterparts. In this paper we utilized MOSFET-like CNFETs for designing the logic gates.[7]

IV. SPICE COMPATIBLE MODEL FOR CNTFET

CNTs are used in the channel region of the CNTFET. Different types of CNTFET have been demonstrated in the literature. There are mainly two types of CNTFET: Schottky barrier CNTFET (SB-CNTFET) and MOSFET-like CNTFET as shown Fig. 1. In SB-CNTFET the channel is made of intrinsic semiconducting CNT and direct contacts of the metal with the semiconducting nanotubes are made for source and drain regions. The device works on the principle of direct tunneling through the Schottky barrier (SB) at the source-channel junction. The barrier-width is modulated by the application of gate voltage, and thus, the transconductance of the device is controlled by the gate voltage. In MOSFET-like CNTFET doped CNTs are used for the source and drain regions and channel is made of intrinsic semiconducting CNT. A tunable CNTFET with electrical doping is also proposed. It works on the principle of barrier-height modulation by the application of gate potential.

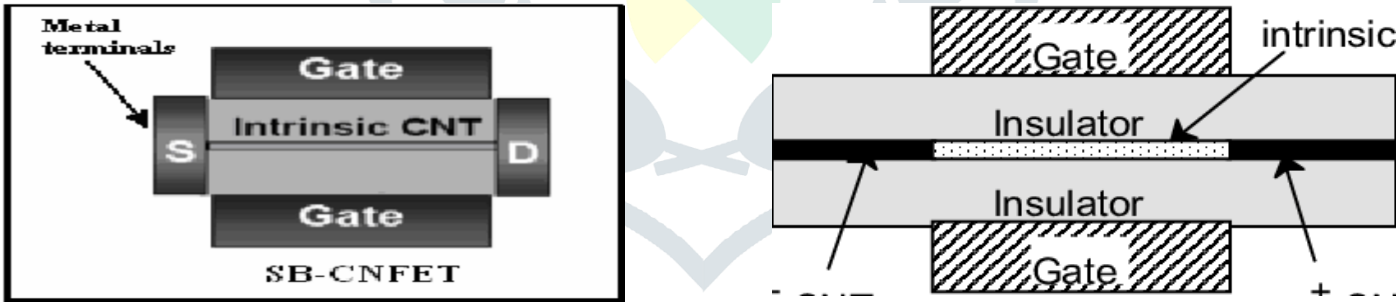

Fig. 1. Different types of CNTFETs: (a) Schottky barrier (SB) CNTFET (b) MOSFET-like CNTFET.[7]

V. ANALYSIS OF LOGIC GATES

We have designed the different digital logic gates and demonstrate the simulation of these logic gates by using HSPICE software. After simulation, we have analysed their average power, delay and PDP (Power delay product).The schematic design and simulation waveform is shown in this section. In fig. 2(a) shows the CNTFET inverter which is the fundamental logic gate for digital circuit design. The circuit consist pull-up networks that is P-type and pull-down network that is N-type which is placed in series between high voltage Vdd and ground. Fig.3(a), Fig.4(a) and Fig.5(a) which shows implmentation of two input NAND, two input NOR logic and two input OR logic gate. In Fig.6 which shows combination circuit of using OR gate and NOT gate.

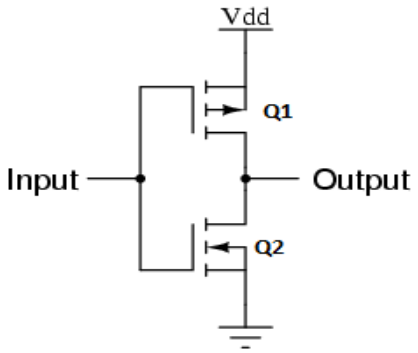

Fig2(a)

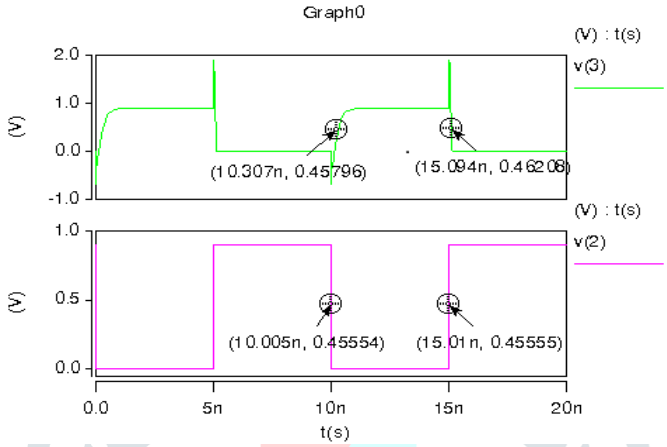

Fig.2((b)

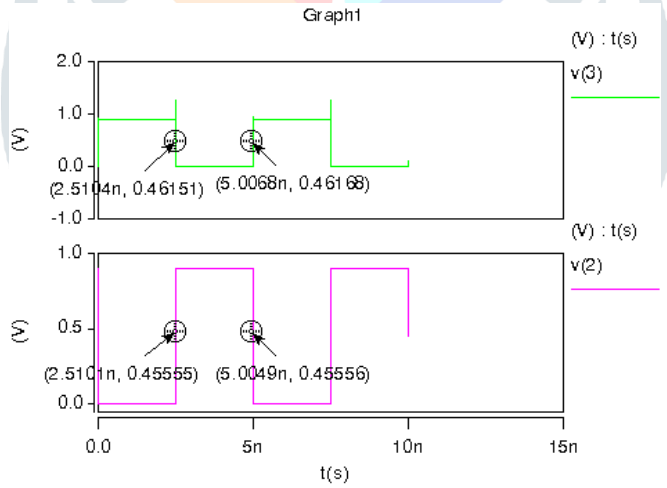

Fig.2((c)

Fig.2. (a) Design of Inverter (b) Transient response of inverter using CMOS and (c)CNTFET

In above figures it shows that inverter using CMOS model which gives more delayed output than that of CNTFET model. It also uses more power and PDP product. Like this design of NAND, NOR, and OR gate using CMOS model give more power,delay and PDP product than that of CNTFET model.

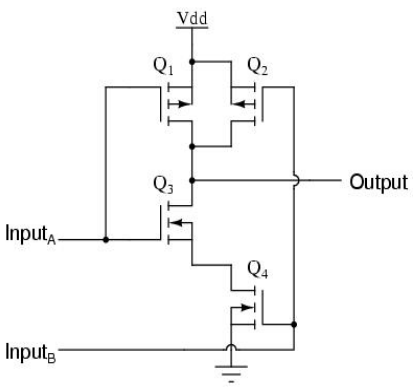

Fig.3(a)

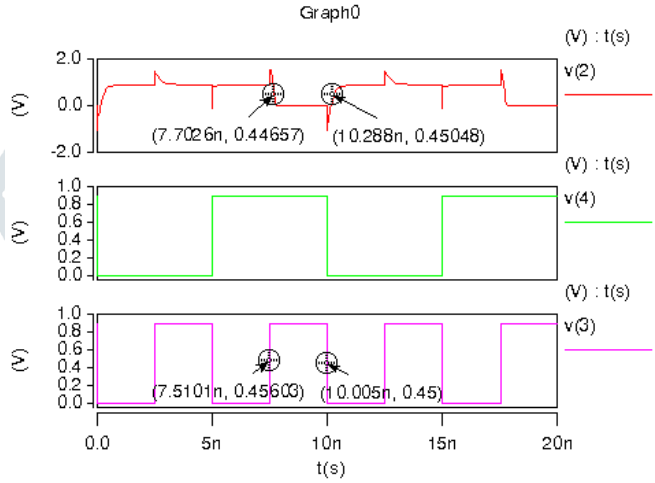

Fig.3(b)

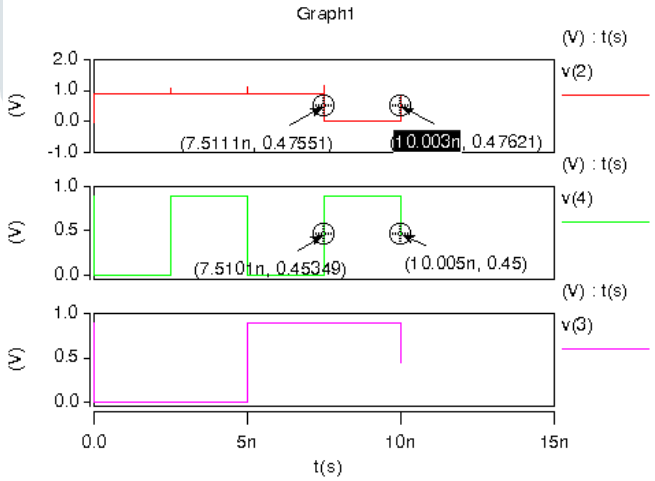

Fig.3(c)

Fig.3 (a) Design of Nand logic gate (b) Transient response of Nand using CMOS and (c) CNTFET

The above design of NAND logic gate shows that transient response using CNTFET model gives more power

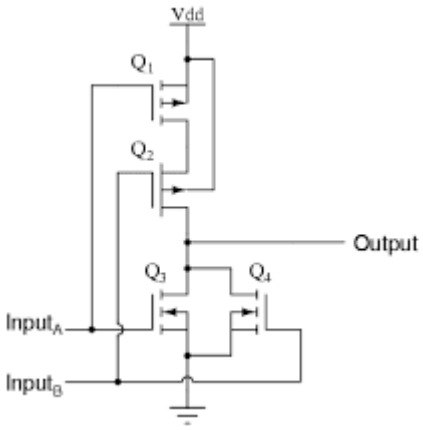

Fig.4(a)

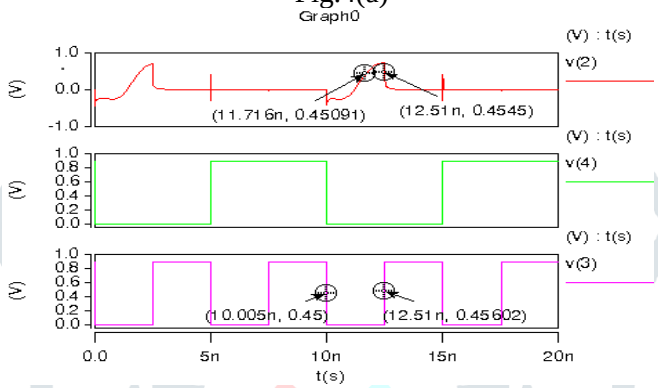

Fig.4(b)

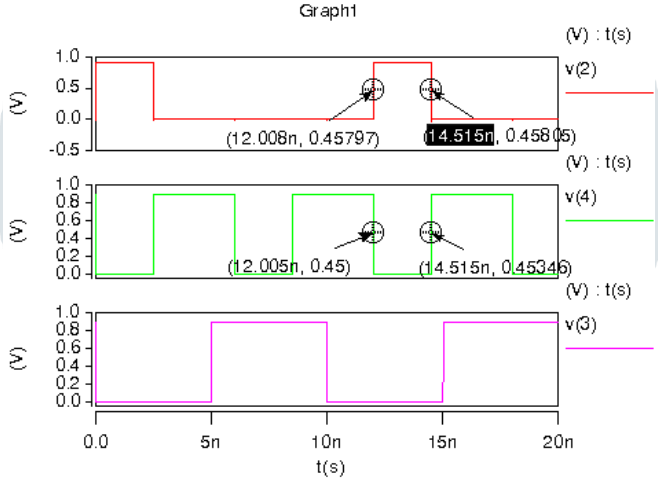

Fig.4(c)

Fig.4 (a)Design of NOR logic gate (b) Transient response of NOR using CMOS and (c)CNTFET

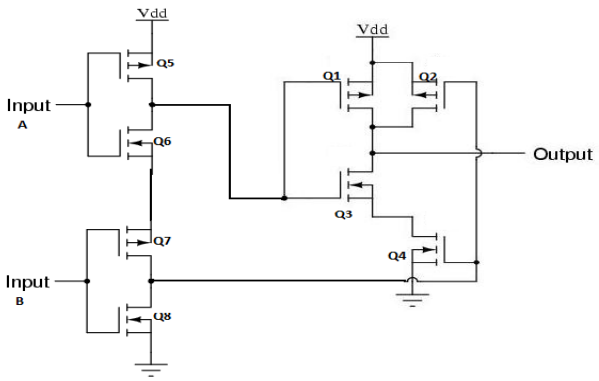

Fig.5(a)

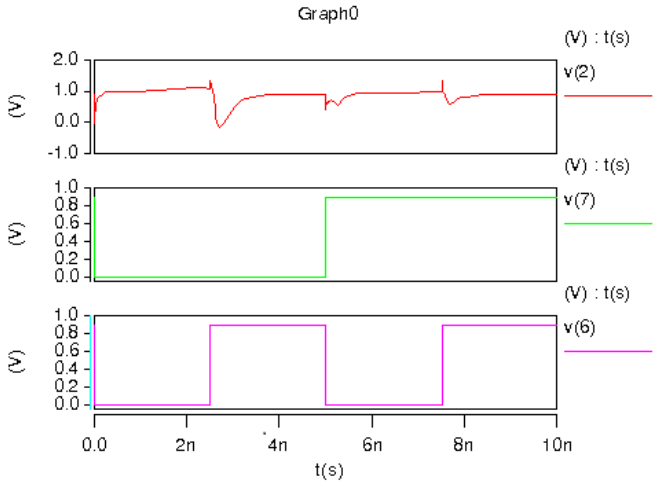

Fig.5(b)

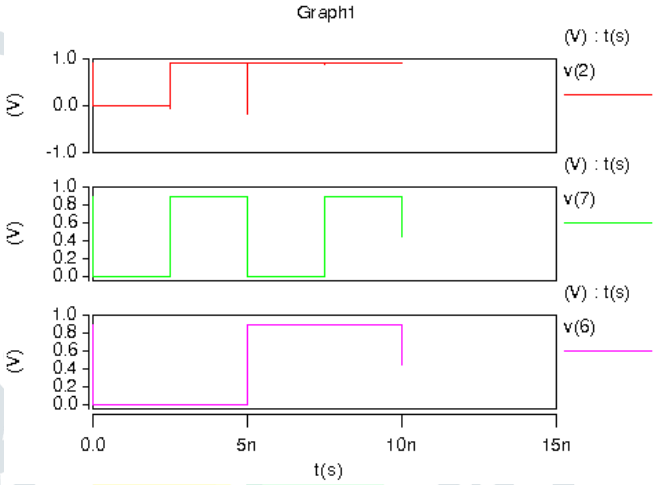

Fig.5(c)

Fig.5 (a)Design of OR logic gate (b) Transient response of OR using CMOS and (c)CNTFET

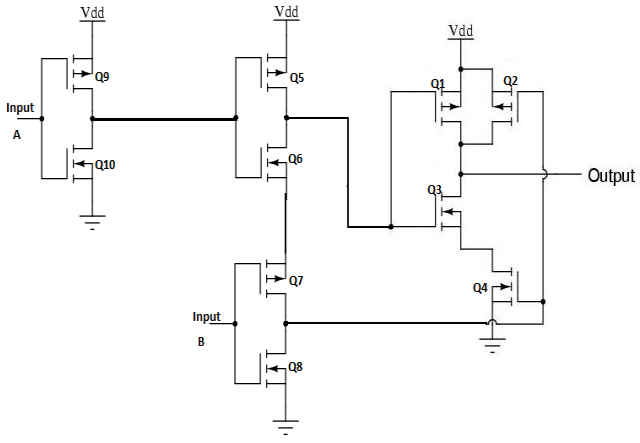

Fig.6(a)

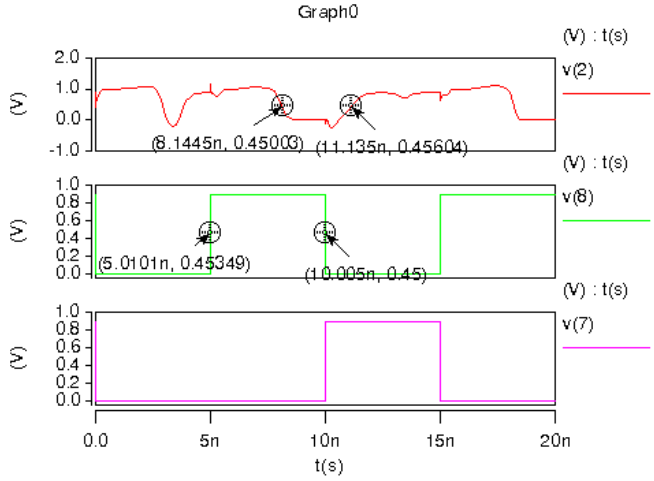

Fig.6(b)

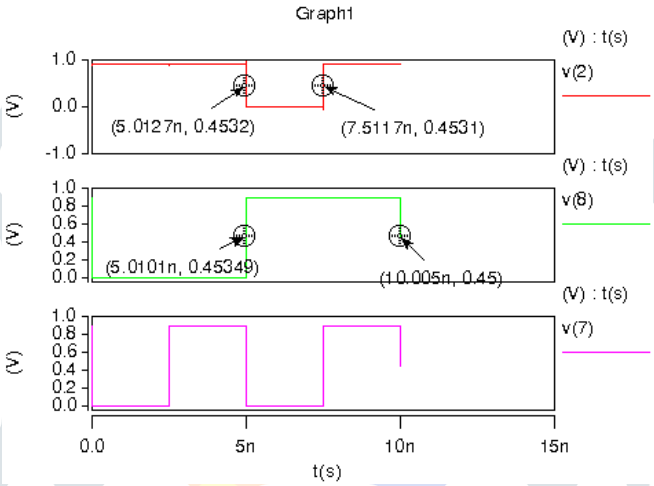

Fig.6(c)

Fig.6 (a)Design of Combination circuit (b) Transient response using CMOS and (c)CNTFET

The above designs are simulated in HSPICE software. The voltage transfer characteristic (VTC) curve of above gates using CMOS 32nm technology and CNTFET 32nm technology shown in fig.2 (b), fig.3 (b), fig.4 (b) and fig.5 (b).

TABLE I : Performance Analysis of CMOS logic gates at VDD=0.9V

Designs using logic gates	P (W)	D (W)	PDP (J)
	CMOS		
INVERTER	4.0385E-05	0.386E-09	1.5588E-14
NAND	2.7968E-05	0.4755E-09	1.3298E-14
NOR	1.0185E-04	1.711E-09	1.7426E-13
OR	6.7714E-04		
Combinational Circuit (Y= $\bar{A}+B$)	8.0823E-04	4.2644E-09	34.466E-13

TABLE II : Performance Analysis of CNTFET logic gates at VDD=0.9V

Designs using logic gates	P (W)	D (W)	PDP (J)
	CNTFET		
INVERTER	4.0243E-09	0.0022E-09	8.8534E-21
NAND	9.2441E-09	0.0029E-09	2.6807E-20
NOR	8.1697E-09	0.003E-09	2.4509E-20
OR	2.4703E-09		
Combinational Circuit (Y= $\bar{A}+B$)	7.1956E-08	2.495E-09	1.7953E-16

Conclusions:

- Simulations are performed on HSPICE, which shows that the proposed CNTFET device is more preferable than silicon based device in terms of performance.
- The CNTFET based circuits provides more power reduction, delay reduction, and Power Delay Product (PDP) reduction when compared with CMOS technologies.
- CNTFET is more Efficient than CMOS in terms of power, delay and PDP. CNTFET gives fast output, improved transient response than CMOS.
- From delay table, reduction in delay. From result discussion, give concluding remark of power consumption, power delay product improvement

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