Area efficient mixed mode scan chain design for systematic testing

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Abstract

Today the stipulation for system on chip (SOC) for high performance applications like communications, digital signal processing etc is leading growth in present digital world. There are some requirements for high performance like reducing the area, or reducing the delay or reducing the power as area, power and delay are the important concerns in VLSI. To meet these requirements the use of smallest possible logical depth is used. As these parameters plays a major role in VLSI design ,when we consider he scan chain path in testing the flip-flops which are used for passing data are added with extra multiplexers which creates the more critical path delay. This may cause the performance degradation of the circuit. The multiplexers which are causing more delay are removed and the logic is replaced and generates randomness for data. This may produce some better effect in mixed mode random testing (serial and random mode). The proposed work takes advantage of scan flip-flops which presents better delay are used to design mixed mode logic by random scan chain. The random access scan flip flop controlling logic for both serial mode and random mode. This architecture of mixed mode is area efficient design.

Keywords: Scan flip-flop, Serial scan test, Random access scan test, Mixed mode scan test, Low power test, Test application time, Test data volume

I. Introduction

As digital world techniques improving the demand for more particularity on master and every flip-flop is major concern. To have a constant look over flip-flop the memory elements are modified to muxed D flipflop mean inputs are given through multiplixers. The architecture caused by this architecture is called as scan chains and these are controlled by test modes so that they form a chain by shifting the data. The chain of flip-flops are under control of test mode enable access. As we are having multiplexers here they add two gates path delay towards clock path during this scan chain architecture, and thus shrinkthe functional speed. To improve the capacity load one more output is added called fan-out load. The clock delay gets high [3] because of can chains. So this may affect the performance of scan chains, the full scan chains are redesigned partially for improving the performance. Partial-scan provides a trade-off between the ease of testing and the cost associated with the scan design by selecting a subset of the flip-flops for inclusion in the scan chain. Subsist partial-scan techniques are: based on architecture [4]–[8], testability measures based [9]– [13], and test-generation based [14]–[18]. Flip-flops with poor controllability measures are selected for scan. The effectiveness of this method entirely depends upon testability measures.

The BIST implementation makes advantages like a) Cost efficiency by reducing the external pattern genetrator like ATP b) as particular logic which reduces the fault occurrence is designed c) If we want to test designs parallel less number of BISTs are used of 4) easy to present for consumer 5) Out of electrical testing test equipment usage can be reduced. The last advantage mentioned can actually allow the consumers themselves to test the chips prior to mounting or even after these are in the application boards.

BIST supports testing not only for single designs for multiple designs also–for example system on chip: to start testing the chip sends the signals to test circuit which enable the test circuit. The outputs from the design under test are given back to the BIST and it checks the output result and if there are any errorsit indicates the design is faulty. This test all the embed designs, system on chips.testing one design by assigning or passing inputs data takes more time also testing some hundreds of designs individuallymay consume more time. The external hardware usage of testing can be eliminated. This testing based on BIST makes less time consumption for testing.

II. Existing work

Serial scan testing indicates passing data serially through the scan chains which is efficient but facing some drawbacks like a. Test data volume. b. Test application time c. test power consumption. From the drawbacks the performance overhead is due to scan multiplexers.These scan multiplexers adds 2 gates delay which effects more in reducing speed. From figure 1 we can observe the critical path between two flip-flops by using this there is possibility to calculate the delay effecting the designing. So for scan insertion in testing also follows the same scam multiplexers which create delay effects in design.along with this also adds extra fan-out in output. This effects the speed of testing by creating more critical path delay , hence reduces functional clock speed by 5% to 10%.So many research works are followed to reduce or to eliminate this delay effects in designs. Usage of partial scan chain in place of serial scan chain is one of the solutions. Here the set of flip-flops are replaced by scan flip-flops. This doesn't include critical path based flip-flops so that there is performance development.

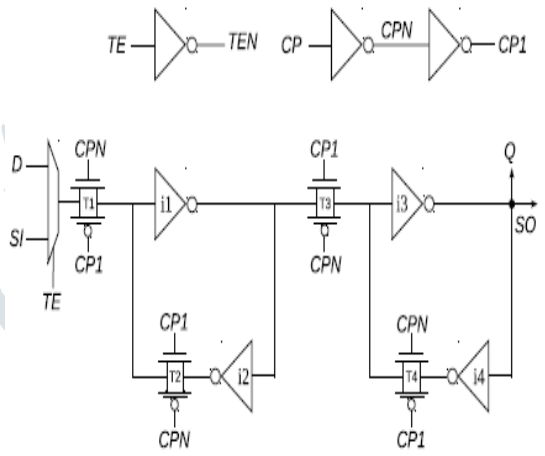

Figure 1.A traditionaldesign of scan flip-flop

As we are having different modes of operation of scan flip-flop, here in this brief we are dealing the mode of operations of scan flip-flop. Let we have a look at figure 1 shows the design of scan flip-flop. In conventional we observed the usage of mux rather than that mux another logic which gives the same operation is implemented and given as input to master flop and slave flop. The dynamic slave flop is utilized to move the input test vector to functional mode.so the slave flop drives Q to input based on controlling pins. In new modified scan chain design the master flop is designed to utilize transmission gates and two inverter , and also associated with transmission gate2 .similarly the slave flop is also designed with more two transmission gates and inverters. To build the test mode some transmission gates like t4, t5, t6 along with inverter are cascaded to master flip-flop. It ought to be noticed that the additional gates added to the master to shape the test mode input way are not on the utilitarian way. In the period of functional mode this extra added hardware stays conditionally,now scan flop works as a ordinary flip-flop.so these master and slave flop are controlled by signal CPN and CP1 which in turn controlled by CP. SCN and SC! Are the signal controlled by SCK

but they are used for controlling the functional mode operations.SCK signal and TE are proportional, in any case, as opposed to the ordinary output plan in which TE is an absolutely combinational flag, SCK is a low frequency or semi successive flag.SCK signal used not only for test performance but also for checking data. The activity is run in low frequency, regularly at 10MHz to 50MHz, contrasted with the framework or practical clock frequency.

The short discussion about the working of functional mode state, here the output flip-flop mechanisms infunctional mode flip-flop.SCK signal should be high. For high state of SCK the transmission gates T1, T2 will be on working mode. This doesn't involvesthe test mode input way from the master structure and the output flip-flop works as an ordinary flip-flop. The SCK signal state high indicates or presents the functional mode working.Along with this T7 transmission gate always enables.This keeps the dynamic slave latch constantly straightforward amid the practical mode and makes the scan yield (SO) master time at whatever point there is an adjustment in master latch state. In any case, that isn't of any worry the extent that the functional mode task is concerned on the grounds that the scan yield (SO) drives just the output way which bolsters the scan input (SI) of the progressive scan flip-flop.

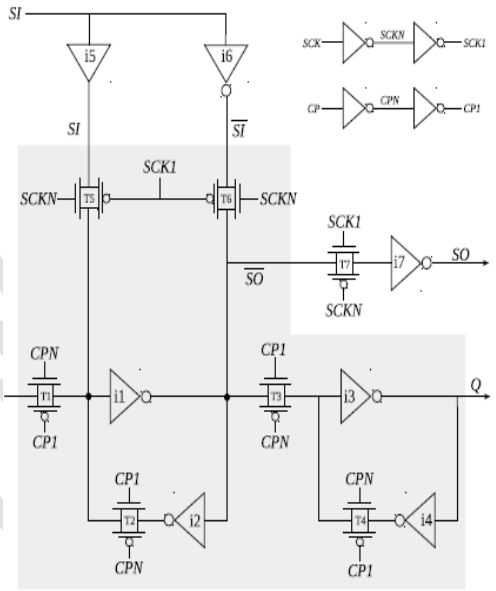

Figure 2: scan flip-flop design

The scan input way stays atmaster structure amid the useful method of activity. The high enabling of the so signal makes data to flip over the output of scan cells.As a process at any point in scan design at functional mode gives Q to be enabled, Likewise, in traditional scan cell, the output multiplexer which falls in the output way would disseminate repetitive power in both the modes. In functional mode, the master latch of proposed examine cell gets its contribution from the utilitarian information input D.At the point when clock CP is low, the estimation of utilitarian info D engenders into the useful mater latch. Now check the conditions for test mode, CP signal which maintains high state gives back to back utilization of output clock SCK presents proposed scan chains.Because of Cp signal state in high makes T1 gate to be on state in testmode. This master the practical info D from the master latch.During test mode, the master latch gets its contribution from output input SI. Because of changing states of SCK signal the load of data in scan chains occur. As it tends to be seen in Figure, when SCK gets to rationale low (0), T5 and T6 get empowered, and the estimation of SI is composed into the master latchalong these lines to memory compose activity.

III. Proposed Work

Mixed Mode Scan Design

In a mixed scan design, a portion of the flip-flops are utilized to frame sequential output and rest of the flip-flops structure RAS architecture. Both sequential scan test engineering and RAS test design are worked simultaneously [20]. But here the partial mode working of scan chains are also replaced and worked with RAS cells.The sequential scan chain is implemented for serial data transfer in mixed mode.

and the flip-flops that are incorporated into RAS architecture are supplanted by RAS cell. Clock should be in active state for entire operation. Thus, the sequential output part can't be worked in simultaneous to RAS utilizing the traditional sequential scan cell. The proposed output cell conquers this issue by utilizing test control motion as a moderate frequency filter clock and permits to work both sequential and RAS configuration in parallel.

The proposed scan design disposes of the requirement for two separate scan cell libraries for executing sequential scan part and RAS part. It gives a typical scan cell that can be utilized both as a sequential output cell just as a RAS cell. Schematic structure of region and execution proficient, dynamic irregular access filter cell RAS and sequential part individually. The initial phase in mixed mode check design usage is isolation of all the flip-flops into two gatherings. One gathering of the flip-flops is doled out to sequential part and the flip-flops from the second gathering go into RAS part.

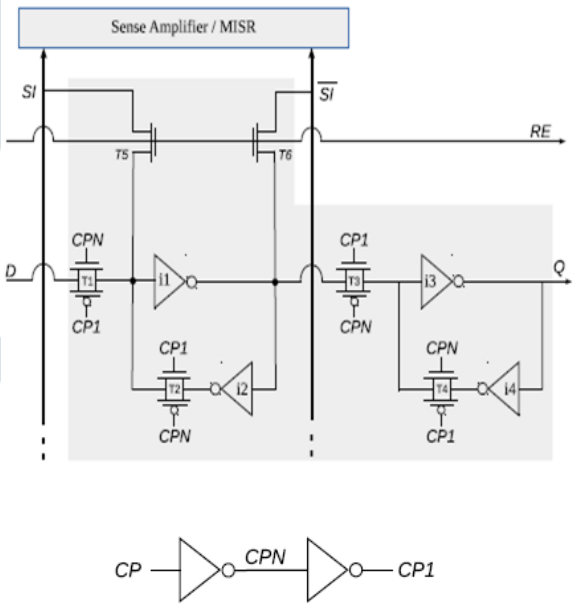

Figure 3. Random Access Scan (PRAS) Cell

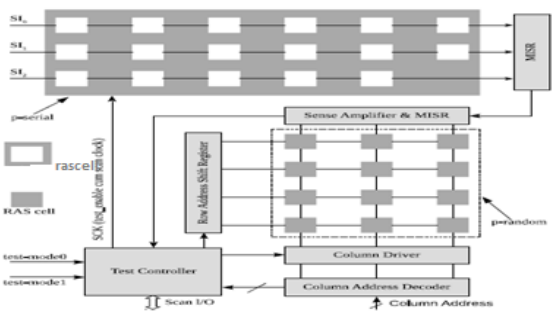

Figure 4 . Mixed mode scan design architecture

The isolation of scan cells among sequential part and RAS part is exceptionally critical for test time, test information volume, test control scattering, and zone overhead. For the present work, we have utilized a straightforward measure dependent on test design care bits. The scan cells for which a large portion of the examples are determined with consideration bits are incorporated into sequential output part. While those scan cells for which a large portion of the test designs have unspecified or couldn't care less bits are incorporated into RAS part.

The usefulness of the circuit is constrained by the two test mode control signals test-mode0 and test-mode1. Contingent on the conditions of the test control flags the circuit can work in four modes. At the point when the two signs are 0, the circuit works in ordinary practical mode. The staying three states are mixed mode (01), p-arbitrary mode (10), and p-sequential mode (11). The test procedure begins with mixed mode with p-sequential and p-irregular stacking/emptying the test boosts/reaction simultaneously. The move activity in p-serial which is mixed utilizing the read/compose task in p-arbitrary is completed in two stages. Note that the read/compose task in RAS compares to stacking/emptying of test improvements/reaction. To begin with, the line empower flag is declared to peruse the current condition of the RAS cells. The read task is performed push by column utilizing the sense amplifier.

IV. Results and discussion

The mixed mode test design is likewise assessed for test information volume and test application time for stuck to blame test. The ATPG was performed for stuck-at faults Static compaction was utilized for test design compaction during ATPG. For reasonable examination, the quantity of accessible test pins was kept steady for all the three structures. Test time and test information volume are processed utilizing a similar measure. The exploratory outcomes displayed.

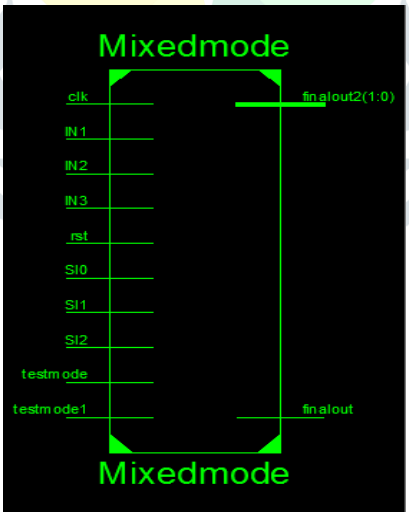

Figure 5. Block diagram

Here in figure 5 clk,rst, are control inputs. IN1,In2,IN3 are user data. SI0,Si1,SI2 are scan data. Below figure 6 is the RTL schematic figure of mixed mode architecture.

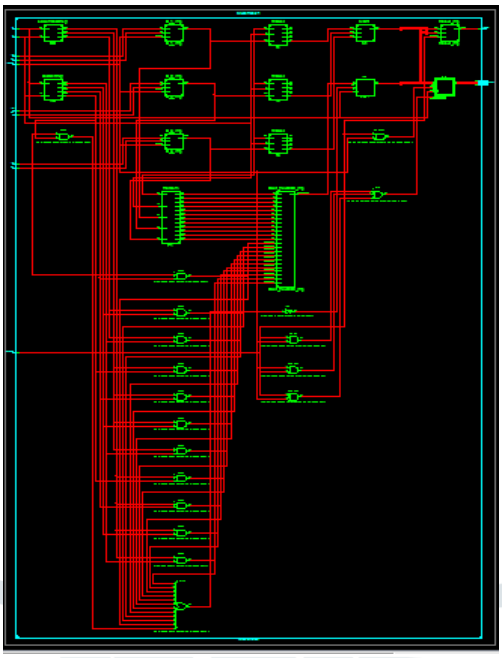

Figure 6. Mixed mode RTL schematic

Output wave form results are shown below

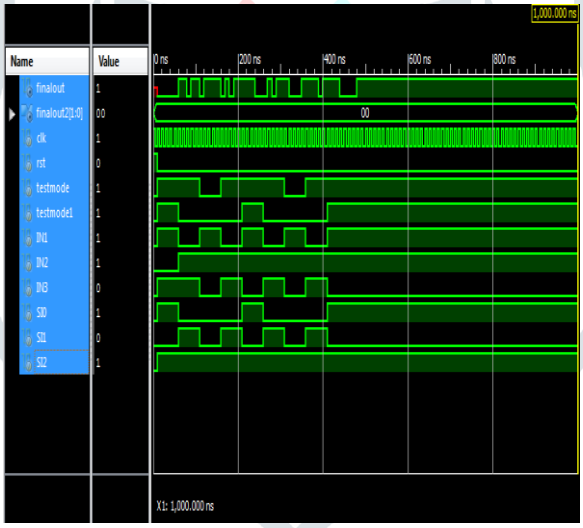

Figure 6.Output waveform result.

Area , delay and power are the major parameters of any vlsi design that to be compared, for the mixed mode architecture which is designed with both serial mode and ras scan chain is compared with proposed work of mixed mode architecture designed using less control input based ras cell. The comparison table is shown in table 1.

Parameters	**Mixed mode proposed**	**Mixed mode extension**

Area	132 LUT's	89 LUT's
delay	4.905ns	4.905ns

Table 1. Comparison table

V. Conclusion

The area efficient design for scan chain is proposed that which overcome the low performance due to critical path and high usage of multiplexers in design and replacing random scan architecture for mixed mode design. The new proposed design of mixed mode works for all conventional and test flow. Furthermore, the proposed scan flip-flop can be used both as a serial scan cell as well as a RAS cell, in the mixed mode scan test.

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